

A Blueprint for Inverting Buck-Boost Compensation

Designing a voltage-loop compensator is critical for buck-boost converters that generate negative voltage rails.

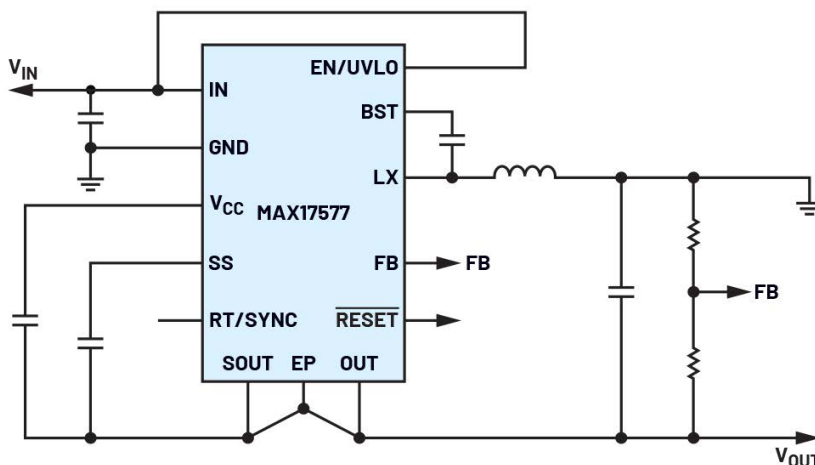
Many electronic systems require one or more [negative supply rails](#), typically implemented alongside corresponding positive rails to form symmetrical power supplies. These negative voltages are essential for proper biasing, signal swing, and device operation in various applications, including [gate-driver circuits](#) for [EV power electronics](#). This enables efficient switching of wide-bandgap semiconductors such as gallium-nitride (GaN) FETs and silicon-carbide (SiC) MOSFETs in onboard chargers (OBCs) and traction inverters.

Precision [analog front ends \(AFE\)](#)s, including high-resolution [analog-to-digital converters \(ADCs\)](#) and digital-to-analog converters (DACs), require negative rails to deliver a full dynamic range and linearity in industrial and medical equipment. [Rail-to-rail op amps](#) used in many of the same signal chains need negative supply voltages for the same reason. Medical imaging equipment depends on

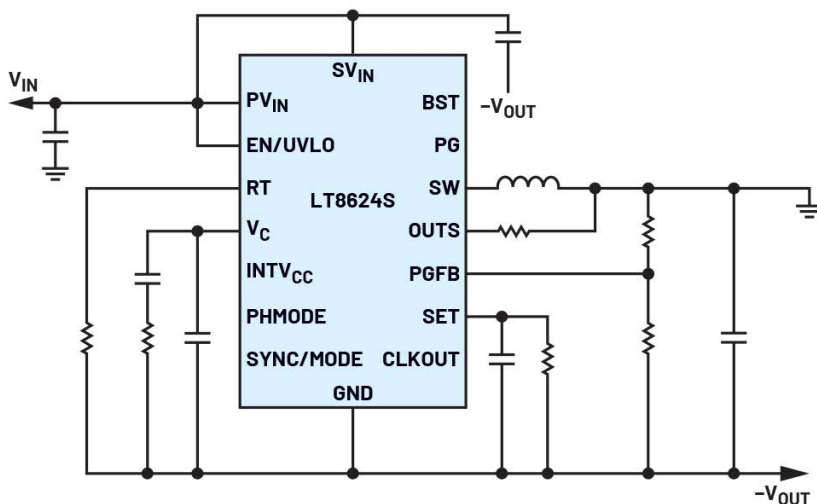
negative voltages for detector bias and signal conditioning.

In data centers, [optical transceivers](#) apply negative bias voltages to [photodiodes](#), which take light signals shooting through fiber-optic cables and translate them into electrical signals for servers and [switches](#). The negative bias voltage helps them achieve high-speed response and low-noise operation. In consumer electronics, negative voltages are also used to control pixels and adjust contrast in high-resolution LCD displays.

These negative rails are typically generated using the inverting buck-boost (IBB) topology. In these cases, engineers can use a buck-boost regulator specifically designed for negative-output operation. Alternatively, a standard buck regulator could be reconfigured for inverting operation by rerouting the power stage. The differences between these approaches are outlined in *Figure 1*, which shows a dedicated IBB solution, and *Figure 2*, which illustrates a buck regulator configured to output negative voltages.



1. The MAX17577 inverted buck-boost circuit. (Credit: Analog Devices)



2. The LT8624S configured as an inverting buck-boost converter. (Credit: Analog Devices)

Since there are tradeoffs with each approach, a practical design example can help illustrate their pros and cons. The process starts with power-stage design considerations based on a set of electrical requirements and then discusses how to develop the small-signal control-to-output transfer function for peak current-mode control operating in continuous conduction mode (CCM). The design requirements, including small-signal linear operation around the steady-state operating point, are in *Table 1*.

Using the model, a voltage-loop compensator can be developed for the power stage to improve loop stability and transient response. The analysis assumes a peak current-mode controlled converter with internal slope compensation and a high-bandwidth inner current loop, allowing the outer voltage loop to be modeled with a Type-II (two-pole, one-zero) compensator. For devices with internal [compensation](#),

designers should follow the recommendations provided in the respective datasheets.

Step-By-Step Process for Power-Stage Design

Here's the step-by-step procedure for designing the power stage.

1. For an IBB converter, the ideal duty cycle is calculated using the magnitude of the output voltage:

$$D = \frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|} \quad (1)$$

2. The average current through the inductor is determined as:

$$I_L = I_{OUT} \left(1 + \frac{|V_{OUT}|}{V_{IN} \times \eta} \right) \text{ A} \quad (2)$$

3. The peak inductor current can be calculated using the following expression, assuming an AC ripple current of 30% of the average inductor current (represented by 0.3):

$$I_{L,peak} = I_L + \frac{\Delta I_L}{2} \text{ A} \quad (3)$$

where:

$$\Delta I_L = 0.3 \times I_L \text{ A} \quad (4)$$

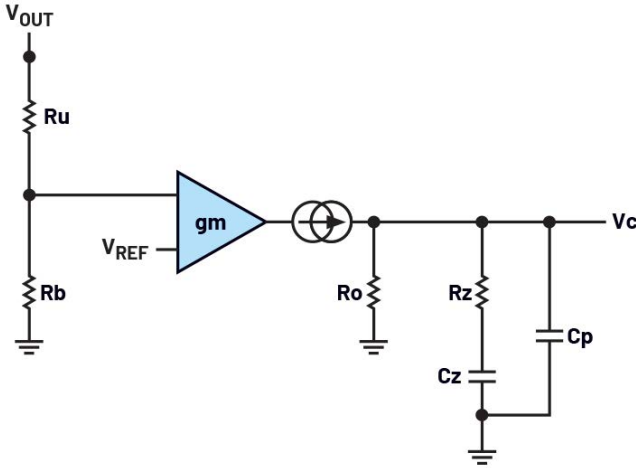
4. The inductor to be selected should have an I RMS rating greater than I_L , and I_{SAT} rating greater than $I_{L,peak}$. The inductance required is determined as:

$$L = \frac{V_{IN} \times D}{\Delta I_L \times f_{sw}} \text{ H} \quad (5)$$

For buck-converter ICs configured in IBB mode with a duty cycle greater than 50%, the selected inductance must exceed the minimum required inductance L_{min} , as specified in the respective product datasheet. The example formula from the LT8624S is as follows:

Table 1: Design Requirements

Parameter	Value
Input voltage, V_{IN}	5 V
Output voltage, V_{OUT}	–5 V
Load current, I_{OUT}	1 A
Switching frequency, f_{sw}	3.3 MHz
Efficiency, η	90%
Upper feedback resistor, R_u	454 k Ω
Upper feedback resistor, R_b	49.9 k Ω
Load resistor, R	5 Ω
Power block transconductance, G_m	6 S
Transconductance of error amplifier, g_m	12 ms



3. A voltage-loop compensator to pair with the buck-boost converter. (Credit: Analog Devices)

$$L_{min} = \frac{V_{IN} \times (2 \times D - 1)}{2.5 \times f_{sw}} \text{ H} \quad (6)$$

When applying the L_{min} formula for the IBB configuration, replace V_{IN} with $V_{IN} + |V_{OUT}|$, and use the duty cycle D , calculated in Step 1. The resulting formula is:

$$L_{min_IBB} = \frac{(V_{IN} + |V_{OUT}|) \times (2 \times D - 1)}{2.5 \times f_{sw}} \text{ H} \quad (7)$$

5. The right-half-plane (RHP) zero is determined by the following equation:

$$f_{rhp} = \frac{|V_{OUT}| \times (1 - D)^2}{2 \times \pi \times L \times D \times I_{OUT}} \text{ Hz} \quad (8)$$

Since the V_{OUT} is negative, the absolute value of the same is considered.

6. The target crossover frequency, f_{cr} , is at a range of $0.1 \times f_{rhp}$ to $0.3 \times f_{rhp}$. Selecting $f_{cr} = 0.3 \times f_{rhp}$ Hz.

7. Considering a step load current, $I_{STEP} = 0.5 \times I_{OUT}$ for a 3% V_{OUT} ripple ($\Delta V_{OUT} = 0.03 \times V_{OUT}$), the output capacitance is calculated as:

$$C_{OUT} = \frac{I_{STEP}}{2 \times \pi \times f_c \times \Delta V_{OUT}} \text{ F} \quad (9)$$

Note that the C_{OUT} value calculated is derated to V_{OUT} .

8. The slope compensation, S_E , is determined from Equation 7, which is the denominator, that is $2.5 \times f_{sw}$ A/s.

9. The current-sense resistance, R_i , can be approximated by:

$$R_i = \frac{1}{G_m} \Omega \quad (10)$$

Generally, the slope and the current-sense information aren't made directly available in the datasheet.

10. Evaluate the inductor current slope S_N as:

$$S_N = \frac{V_{IN}}{L} \text{ A/s} \quad (11)$$

11. The power stage output-to-control transfer function can be calculated with:

$$G_{VCI}(s) = K_{VCI} \times \frac{\left(1 - \frac{s}{\omega_{rhp}}\right) \times \left(1 + \frac{s}{\omega_{esr}}\right)}{\left(1 + \frac{s}{\omega_{pl}}\right) \times \left(1 + \frac{s}{Q_p \times \omega_n} + \frac{s^2}{\omega_n^2}\right)} \quad (12)$$

where:

$$K_{VCI} = \left(\frac{(1 - D) \times R}{R_i}\right) \times \frac{1}{1 + \left(\frac{(1 - D)^3 \times R \times T_S \times (m_c - 0.5)}{(1 + D) \times L}\right)} \quad (13)$$

$$\omega_{rhp} = 2 \times \pi \times f_{RHP} \text{ rad/s} \quad (14)$$

$$\omega_{esr} = \frac{1}{R_c \times C_{OUT}} \text{ rad/s} \quad (15)$$

The value, R_c , is the ESR of the output capacitor in Ω .

$$\omega_{pl} = \frac{1 + D}{R \times C_{OUT}} + \frac{T_S \times (1 - D)^3 \times (m_c - 0.5)}{L \times C_{OUT}} \text{ rad/s} \quad (16)$$

$$Q_p = \frac{1}{\pi \times (m_c \times (1 - D) - 0.5)} \quad (17)$$

$$\omega_n = \pi \times f_{sw} \text{ rad/s} \quad (18)$$

$$m_c = 1 + \frac{S_E}{S_N} \quad (19)$$

[The parameters of the power supply are shown in Table 2.

Completing the Buck-Boost Converter with a Compensator

Figure 3 represents a two-pole, one-zero voltage Type-II voltage-loop compensator. The transfer function of the component can be calculated as:

$$\frac{K_v}{s} \times \frac{\left(1 + \frac{s}{\omega_{zc}}\right)}{\left(1 + \frac{s}{\omega_{pc}}\right)} \quad (20)$$

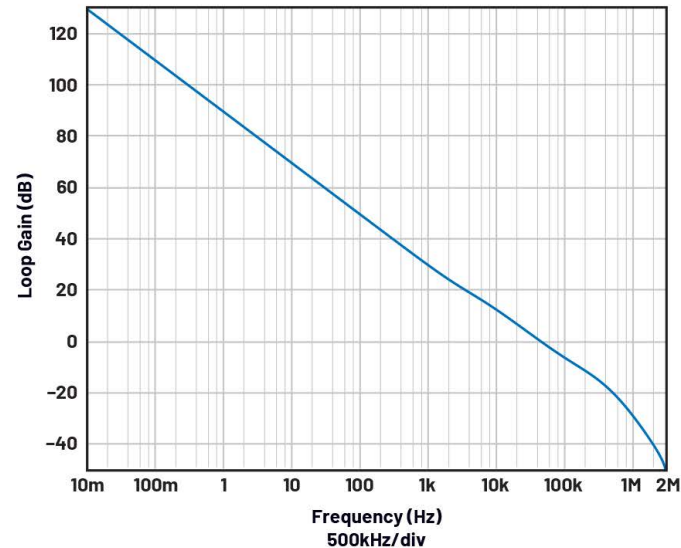
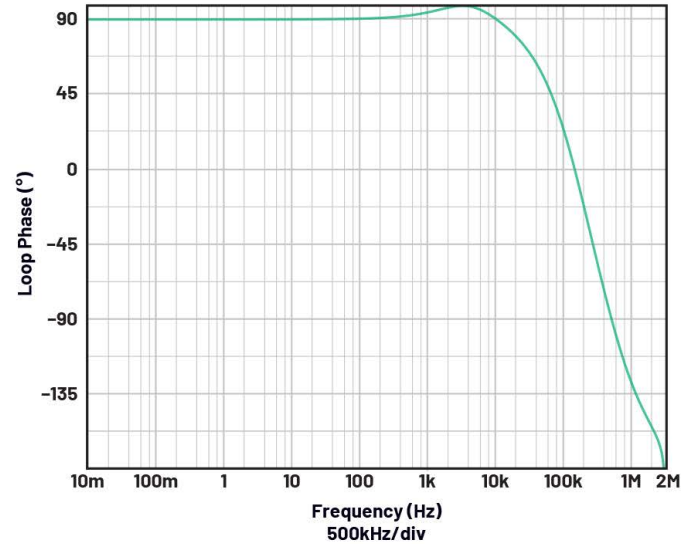
Table 2: Power Stage Parameters

D	0.5	C_{OUT} (F)	11.79 μ
L (H)	2.7 μ	K_{VCI}	12.18
f_{rhp} (Hz)	147.365k	ω_{rhp} (rad/s)	925.925k
f_{cr} (Hz)	45k	ω_{pl} (rad/s)	31.343k

The combination of the control to output transfer function and the output voltage feedback provides insight into designing the compensator transfer function. From there, you can follow these step-by-step guidelines:

1. The additional gain required for the loop transfer function to obtain the required bandwidth:

$$G_{req} = \frac{\omega_{cr}}{H \times K_{VCI} \times \omega_{pl}} \quad (21)$$



— Loop Phase
Phase Margin = 59.07667°
— Loop Gain
Gain Margin = 8.9096311dB
Gain Crossover Frequency = 46.265389kHz

4. The Bode plot of the buck-boost converter operating at full load. (Credit: Analog Devices)

where:

$$H = \frac{R_b}{R_u + R_b} \quad (22)$$

$$\omega_{cr} = 2 \times \pi \times f_{cr} \text{ rad/s} \quad (23)$$

[2. The phase shift of the power-stage transfer function is represented:

$$PS = -\tan^{-1} \frac{\omega_{cr}}{\omega_{rhp}} + \tan^{-1} \frac{\omega_{cr}}{\omega_{esr}} - \tan^{-1} \frac{\omega_{cr}}{\omega_{pl}} - \quad (24)$$

$$\tan^{-1} \frac{\omega_{cr}}{Q_p \times \omega_n} \text{ deg, } (\omega_n \gg \omega_{cr})$$

3. For a buck-boost converter, a good phase margin is above 45°. Selecting a PM of 60°, the phase boost required is:

$$Boost = PM - PS - 90^\circ \quad (25)$$

4. The factor k is evaluated as:

$$k = \tan \left(\frac{Boost}{2} + 45 \right) \quad (26)$$

5. The compensator pole ω_{pc} and compensator zero ω_{zc} are obtained as:

$$\omega_{pc} = \omega_{cr} \times k \text{ rad/s} \quad (27)$$

$$\omega_{zc} = \frac{\omega_{cr}}{k} \text{ rad/s} \quad (28)$$

6. The integrator gain is obtained as:

$$K_v = G_{req} \times \omega_{zc} \quad (29)$$

7. The components for the above compensator are designed as:

$$R_z = \frac{G_{req}}{g_m} \Omega \quad (30)$$

$$C_z = \frac{g_m}{K_v} \text{ F} \quad (31)$$

$$C_p = \frac{1}{R_z \times \omega_{pc}} \text{ F, } (C_p \ll C_z) \quad (32)$$

Table 3 shows the compensator designed for the power stage.

Table 3. Compensator Parameters

ω_{pc} (rad/s)	3.696M	C_p (F)	433.954p
ω_{zc} (rad/s)	21.625k	C_z (F)	74.184n
K_v (s/rad)	161.758k	R_z (Ω)	623.345

Simulating the Circuit and Testing Its Performance

The simulation of the IBB stage, configured with the parameters derived in *Table 3*, is shown in *Figure 4*.

At a crossover frequency of 46.269 kHz, the loop exhibits a gain margin (GM) of 8.90 dB and a PM of 59.07°; GM is expected to be greater than 10 dB. This can be improved by tuning the compensator pole. In this design, transient response was prioritized over gain margin, resulting in a measured GM of 8.9 dB, which is acceptable for the intended operating range.

During the load step, the transient waveform exhibits an output-voltage excursion of roughly 2.88%, indicating the

converter's dynamic response characteristics (*Fig. 5*).

Given all that, it's evident that the selection of the inductor, L , directly influences the location of the RHP zero and, consequently, limits the maximum achievable crossover frequency of the IBB converter. The choice of output capacitance, C_{OUT} , not only determines the output-voltage excursion during load transients, but together with its equivalent series resistance (ESR) and inductor L also shapes the dominant power-stage pole.

These parameters collectively dictate the required loop gain and phase boost during compensator design, ultimately determining the resulting phase margin of the system.

This checklist outlines the essential design requirements:

- High RHP zero for adequate bandwidth (via inductance selection).
- Phase margin (PM) > 45°.
- GM ≥ 10 dB is recommended; however, slightly lower GM may be acceptable when transient performance is prioritized.
- Output voltage deviation ≤ 3% during load transients.

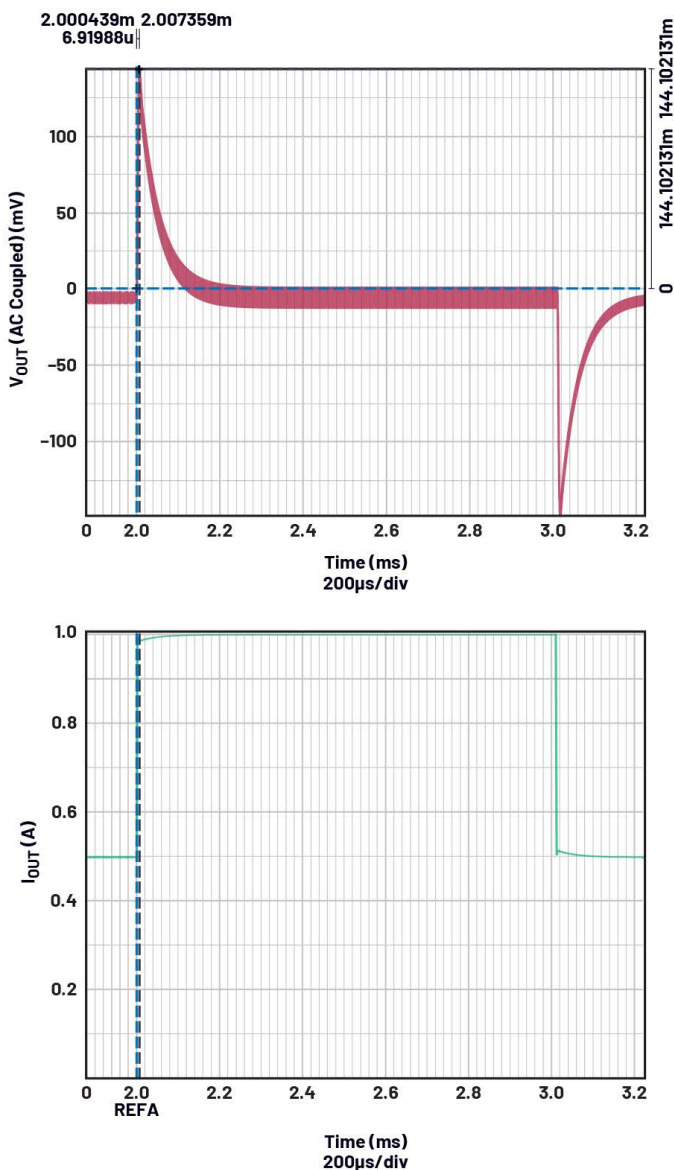
Conclusion

This step-by-step guide gives engineers a systematic approach to compensator design for IBB converters. By deriving the small-signal power-stage model and explicitly accounting for the RHP zero, designers can select an appropriate loop bandwidth and compensation network. The [LTspice](#) simulations can be used to confirm that the proposed method achieves stable operation and fast transient response, making it suitable for a wide range of negative-rail-generation applications.

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References

- Basso, Christophe P. *Switch-Mode Power Supplies*, Second Edition. McGraw-Hill Professional, February 2008.
- Lamp, Erik. "[Fast-Transient Negative Voltage Rail for Noise-Sensitive Applications](#)." Analog Devices, July 2024.
- Lamp, Erik and Randyco Prasetyo. "[Generating Negative Voltages from a Positive Voltage Supply: Market Requirements and Solutions](#)." Analog Devices, September 2024.
- Mitra, Dipankar. "[How to Use the MAX17501 and MAX17502 for Negative Output Voltage Applications](#)." Analog Devices, April 2014.
- Nelson, Carl. "[AN19—LT1070 Design Manual](#)." Linear Technology, June 1986.
- Ridley, Raymond B. "[A New Small-Signal Model for Current-Mode Control](#)." Ridley Engineering, 1999.



5. The transient waveform with a 0.5- to 1-A load step with 0.5-A/μs slew rate.