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A compendium of articles from *Electronic Design*

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How Rad-Hard GaN Is Powering the New Space Race

A technician wearing a white cleanroom suit and mask is holding a large, circular, mesh-like substrate, likely a GaN wafer, in a cleanroom environment. The substrate has a dark outer ring and a fine grid pattern in the center. In the top right corner, the text "GaN" is enclosed in a green circle.

GaN

Pioneering GaN technology in space

For over 50 years, Infineon IR HiRel has made history by powering countless space missions that unlock the secrets of our universe and advance critical climate research on our planet.

Continuing this proud tradition of innovation, Infineon IR HiRel recently launched the industry's first rad hard Gallium Nitride (GaN) transistor, manufactured in our own fabrication facility, achieving the highest Qualified Manufacturers List (QML) standards for space and defense applications, as defined by the Defense Logistics Agency (DLA). Our 100 V GaN device has undergone the most rigorous testing and certification process in the industry, ensuring consistent quality and reliability in extreme environment applications.

Explore our portfolio of rad hard products and design with complete confidence, knowing you are using the best radiation hardened power, RF, and memory products available, all backed by a global technology leader.



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How Rad-Hard GaN Is Powering the New Space Race



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The New Space Race: What's Happened, What Hasn't, and What's Coming Next

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THE NEW SPACE RACE is imposing complex demands on power system designers. Space-based systems already operate under strict power limits imposed by tight mass and volume budgets. Now a new generation of compact satellites—some as small as a shoebox—is swarming into orbit, equipped with advanced sensors, processors, and connectivity for commercial and military missions. Power demand is rising sharply, along with the difficulty of delivering a reliable, uninterrupted supply.

Power subsystems already occupy a disproportionate share of a satellite's mass and volume. This imbalance comes at a steep cost given the resources required to launch a spacecraft against the pull of gravity into orbit.

As a result, engineers are under constant pressure to deliver more power in smaller, lighter form factors. Innovations in high-efficiency solar cells and high-density lithium-ion (Li-ion) batteries are helping close the gap on the supply side. Equally important, though, is the efficient conversion and distribution of all that power under the hood. Driving up the power density and efficiency while withstanding the rigors of space are key deliverables when designing the next generation of space-based power systems

GaN is rapidly becoming a key technology helping to break through these constraints. Already reshaping everything from consumer fast chargers to power supplies in AI data centers, GaN is now moving into orbit. GaN power FETs run at higher frequencies than silicon with lower switching and conduction losses. Faster switching shrinks bulky magnetics and other passives. Higher efficiencies help ease thermal management in tightly packed satellites, where dissipating heat into the void of space is difficult.

Space adds another challenge: radiation. Electronic systems in space are exposed to intense radiation and harsh temperatures for extended periods. The unique physical properties of GaN grant radiation tolerance. But GaN power devices can also be “radiation hardened” to add robustness. These rad-hard devices are designed to deliver uninterrupted power for years in satellites launched into LEO and MEO and for decades in spacecraft deployed in geostationary (GEO) orbits or deep space.

This technical series examines the design challenges facing power electronics in space—from power density to efficiency and reliability—and highlights how space-grade GaN is helping overcome them.



James Morra,
Lead Reporter
Electronic Design



Credit: NASA/Desiree Stove

CHAPTER 1:

How Do You Counter the High-Radiation Environment of Space?

PAUL MORRIS, VP of the RF and Communications Business Unit, *EnSilica*

This article examines the mitigation techniques that allow space equipment to cope with ionizing solar radiation.

It's an understatement to say that launching equipment into space isn't cheap. Even with costs dropping in recent years, the cost of a satellite and its launch can still be anywhere between \$10 and \$400 million. Indeed, a geomagnetic storm in February is estimated to have caused approximately \$50 million of damage to SpaceX's low-Earth-orbit (LEO) communication satellites. Weather-monitoring satellites cost approximately \$290 million.

And that's before maintenance costs, with component failure requiring either in-space repair or causing the entire system to be written off. In short, all equipment must incredibly reliable and be able to withstand the extreme environment.

There are essentially three key differences faced by chip and system engineers when creating orbit-based rather than ground-based equipment.

The first is temperature, with equipment needing to be protected from extreme (150°C) fluctuations and an operational level maintained. The second is the vacuum.

Collectively these create a different cooling effect than on the ground, relying solely on thermal radiation rather than air convection. This requires slightly different calculations for heat dissipation. It also creates issues with moisture, which gets into the package on the ground and then seeps out of the package once in orbit, potentially delaminating the package from the board. Thus, a separate qualification is required to make sure that you don't have trapped moisture in the package before launch.

These two issues are relatively straightforward to mitigate through packaging and insulation. The third (and arguably more challenging) difference encountered by electronic components in space is radiation.

Radiation Encountered

The magnetosphere of the Earth concentrates particles into two main belts (**Fig. 1**). The

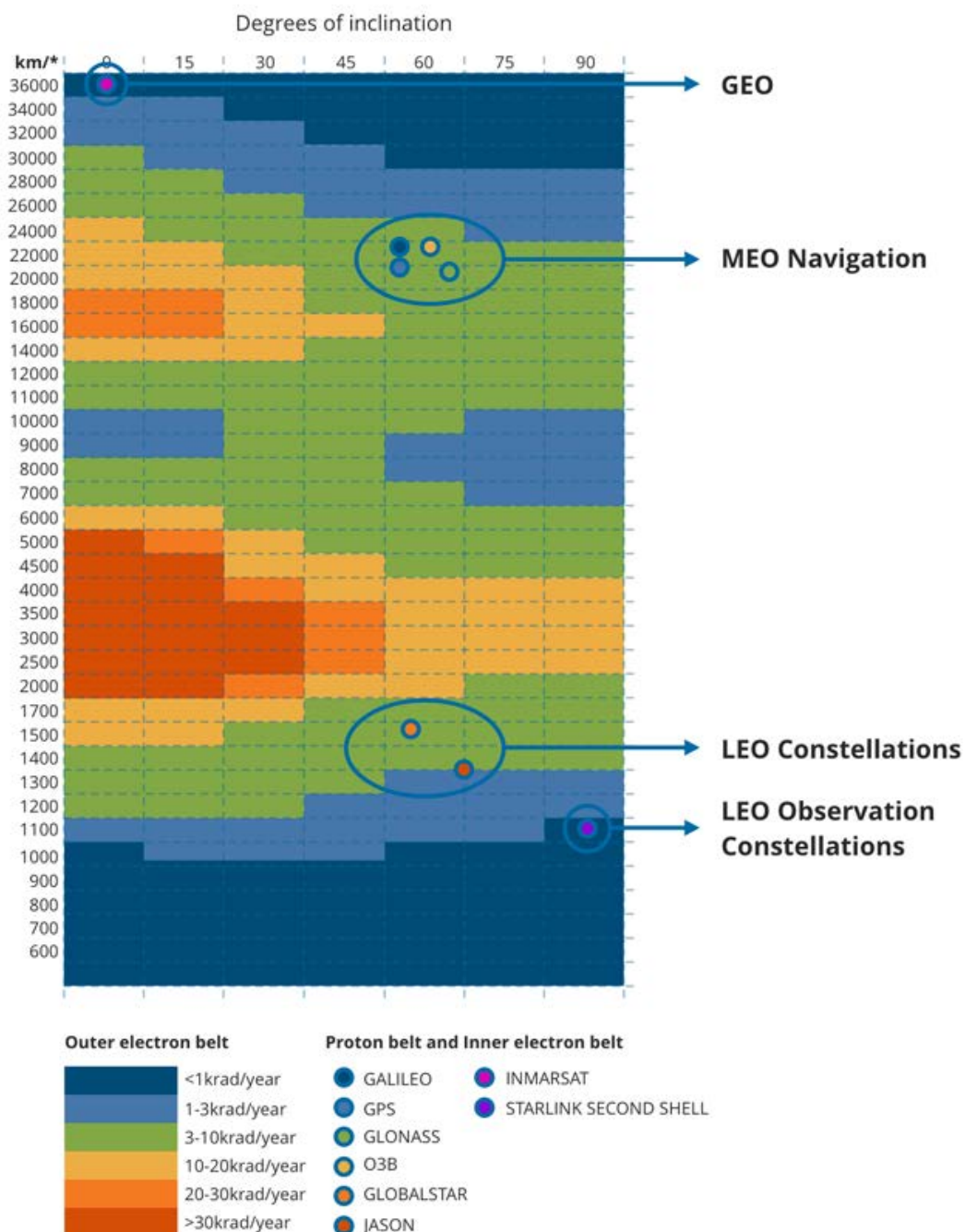
lower belts mostly consist of protons, and the upper belts being mostly electrons, with most of these particles coming from the sun via solar wind / solar flares. Any remaining particles come from cosmic radiation from other galaxies.

While it's difficult to replicate the full test environments on Earth—to generate some of these particles would require in the region of giga electron volts—these belts are at least very well understood and were being studied by NASA since the start of its space programs.

1. Van Allen belts in the earth's magnetosphere, adapted from European Space Agency (ESA) data. The Y axis is orbit height to 36,000 km (geostationary satellite); the X axis is angle of inclination of the orbits (0-90 degrees).

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AE8 Max/AP8 Min - Circular Orbits



Depending on the equipment's orbit, it will pass through these belts at different rates.

Anything that's operating in a polar orbit, such as a spy satellite, will be crossing through the concentrated radiation belts on a regular basis and need protection from a higher radiation dose. Whereas LEO satellites operate at 1,000 to 1,500 km and thus undergo lower levels of radiation.

So, depending on these factors, a satellite can absorb between 1 and 10 kilorads per year. Therefore, we need to calculate the dose a satellite will receive during its lifetime.

Effect of Radiation

Effect of Radiation

In addition to dose, we need to look at the types of radiation and the damage they cause.

Let's first look at ionizing radiation (non-ionizing radiation is discussed toward the end of the article), which can come from protons or electrons. These particles strike the gate oxide of the semiconductor and cause damage through a build-up of charged particles in the MOSFET gates (Fig. 2).

In a PMOS transistor, this increases the threshold voltage and makes it more difficult to turn on. Conversely, in an NMOS transistor, the opposite is true, making it turn on at a lower threshold.

And the probability of this happening is proportional to the size of the gate. Consequently, older process nodes tend to have a higher probability of radiation damage to the gate oxide.

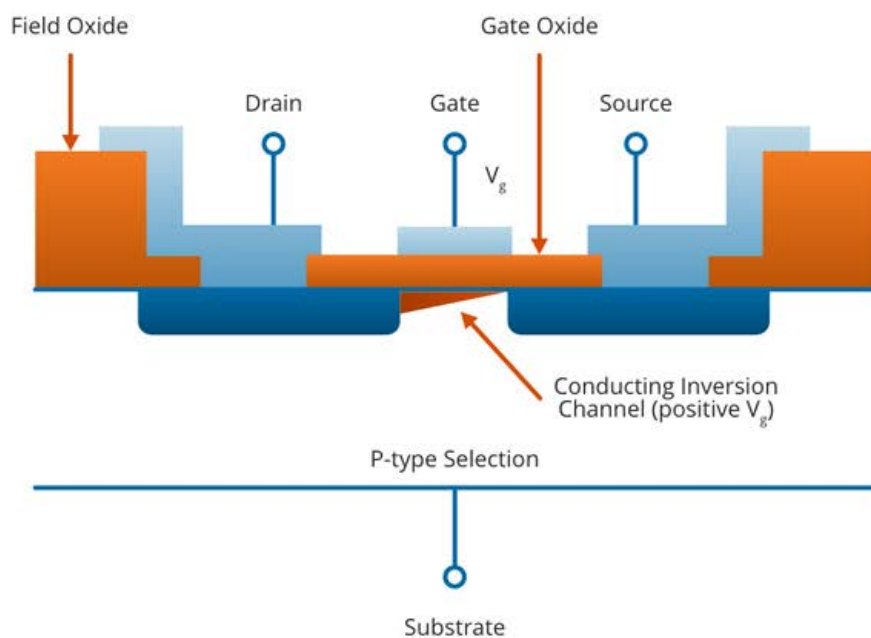
In addition, in an analog design, you can get bandgap shifts, changes in bias current leakage side effects, and an increase in the $1/f$ noise.

Types of Events

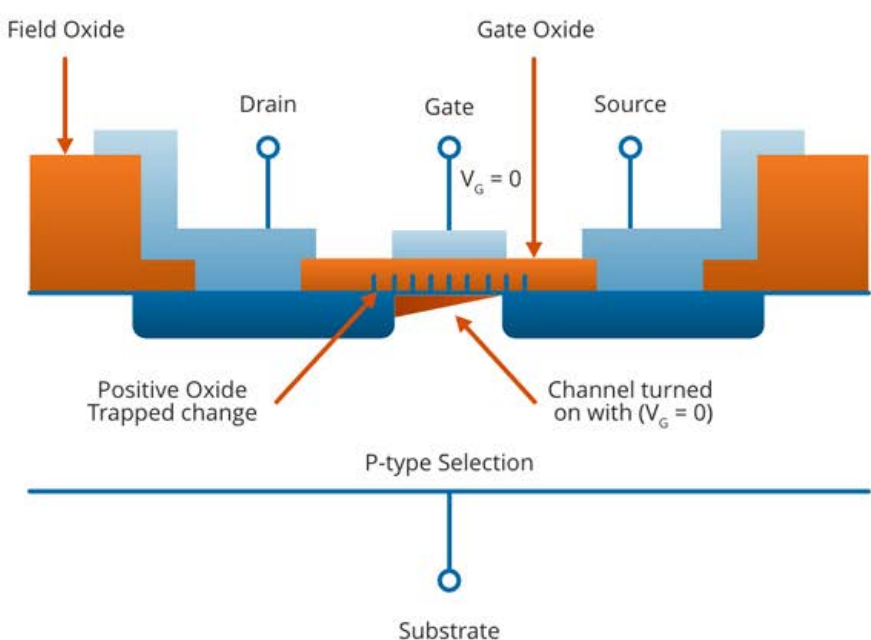
There are two possible outcomes following an impact: a non-destructive or destructive event (Fig. 3). A non-destructive event might be a single-event upset in a storage element, a soft error where the radiation causes a noise spike and changes a memory location from a zero to a one.

A destructive event might be a single-event

(A) MDS Transistor - Normal Operation



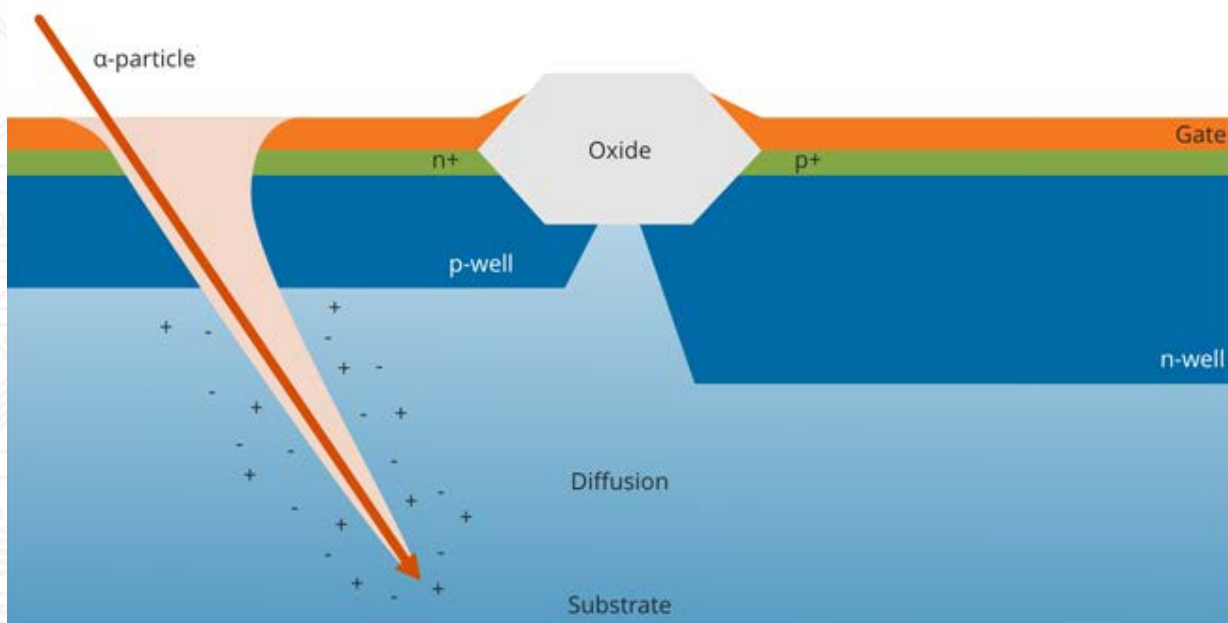
(B) MDS Transistor - Post Irradiation



2. Shown is a standard (top) and damaged NPN transistor (bottom) with the two junctions and its gates in the sensor. The damaged transistor has a positive charge build up on the gates. EnSilica

3. A simplified view of a semiconductor device following a particle impact with a conduction path created across the device.

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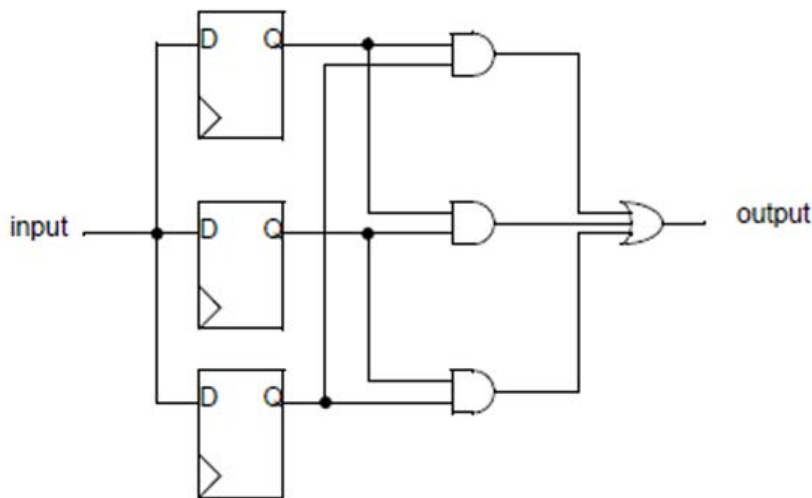
gate rupture, which mostly affects power devices. Or, if the particle impact energy is high enough, it also can cause a single-event latch-up, which results in a device turning on permanently until a power cycle is undertaken. And depending on the device, this can be catastrophic.

Thus, you need to detect and protect the equipment against these events. We've looked at these single end events and their effects tend to come more from the heavier particles, creating electron hole pairs and a transient conduction path; flipping memory locations and flip-flops is a concern, too. And that tends to be how most of these things are tested: Placing a large memory on a device, radiating it, and then measuring the number of errors across the megabits of memory.

Latch-up is a separate test and you need to put in protections to detect power surges and read the ability to reset critical devices.

4. The triple-redundancy flip-flop has been used by the aerospace industry to mitigate against single-event upsets. It offers the best protection, but there are disadvantages.

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Mitigation Techniques

First is gate selection. For example, with a power transistor, which must not switch on by accident, it's better to use PMOS than an NMOS.

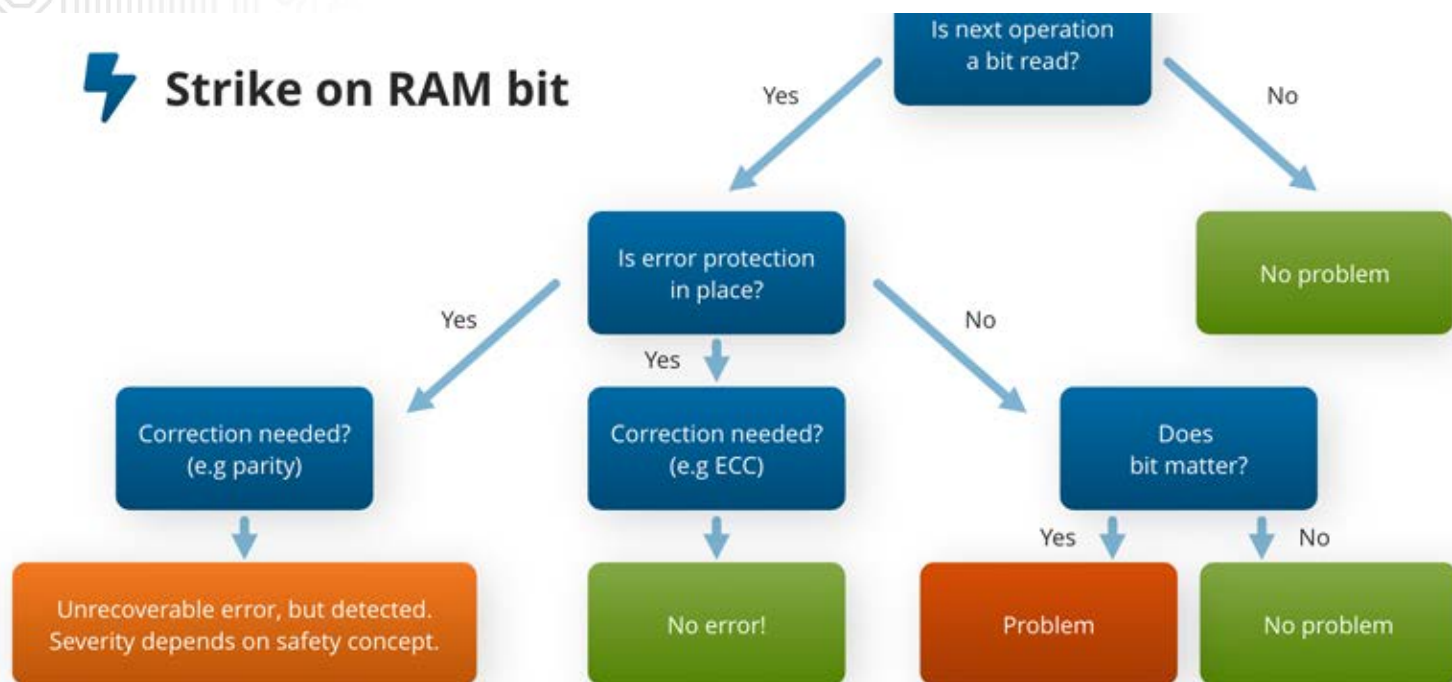
In addition, because the probability increases with size, there's some advantage in going to smaller process nodes, but that that does bring in other risks as well.

And there are specific design mitigation techniques such as avoiding gates with many inputs.

Beyond these basic steps, a host of other specific mitigation techniques target both single-event upsets and single-event latches.

Noteworthy among these is the triple-redundancy flip-flop (Fig. 4). This (and its multiple variants) often

⚡ Strike on RAM bit



5. Error detection and classification following a strike on RAM. EnSilica

has been used in the aerospace industry, as it offers the best possible protection against single-event upsets.

But there are disadvantages that prevent the triple-redundancy flip-flop from being used throughout the design: It's going to triple the size of your solution and increase power demands from the whole system. But they should be deployed in critical areas where you've got key decisions being made.

To avoid a glitch on a clock causing the same error to propagate through, it's also possible to jitter or defer the clocks to each of the flip-flops so that they're all completely independent. The downside for this method is that it doubles the safe faults rate.

Finally, you could have a fully redundant system with separate microprocessors where the results are compared. And only when there's a majority of votes is the output allowed to be used to decide. Again, this is an expensive solution.

In short, the mitigation technique employed will depend on the criticality of the component and the likelihood of a destructive event affecting it.

Predicting and Fixing Software Errors

After an incoming particle strikes RAM, the problem depends on where the next step is read or write. If you're going to be reading that data, you've got a problem. And if the next operation is a write, then the error is going to be cleared. So how do you predict what's going to happen?

It's completely interdependent to the software operation of the system. And, of course, you can put in memory refresh strategies to try to keep your memory clean.

Taking this a few steps further, for some functions—where the data isn't critical to the function—you can ignore it and carry on.

For more critical elements, you could deploy error-correction code (ECC) to give you error protection, with the ECC built into the memory (**Fig. 5**). It should be stated that you

will not always have enough correction parity to fix every error. However, even in this case, such an approach will still be able to detect an error, alerting you to a problem and preventing you from proceeding with certain actions or functions at critical stages.

Additional steps that can be taken include the implementation of cyclic redundancy checks into communication channels; or setting the state machines' Hamming distance to be greater than 1, which will avoid accidental flipping into another state.

Beyond that, it's possible to run software self-test procedures, as well as have the hardware check on the software and the software check on the hardware. Of course, there are external watchdogs, too, as we have in embedded systems. Finally, a remote-control-based internal clock monitor or safety clock can be recovered from a PC.

Coping with Non-Ionizing Radiation

As alluded to above, there are also effects from non-ionizing radiation. Displacement damage leads to more gradual effects, with bits of the silicone structure becoming damaged over time and leakage that causes decreased gain in bipolar transistors.

This effect has been documented in satellites, notably with CMOS imaging sensors becoming damaged over time. In this case, the component might need replacement at some point, or the use of larger devices to create spare pixels and extend the life of the satellite.

Characterization	Class A	Class B	Class C	Class D
Priority (Criticality to agency Strategic Plan)	High priority	High priority	Medium priority	Low priority
National significance	Very high	High	Medium	Low to medium
Complexity	Very high to high	High to medium	Medium to low	Medium to low
Mission Lifetime (Primary Baseline Mission)	Long, >5 years	Medium, 2-5 years	Short, <2 years	Short, <2 years
Cost	High	High to medium	Medium to low	Low
Launch Constraints	Critical	Medium	Few	Few to none
In-Flight Maintenance	N/A	Not feasible or difficult	May be feasible	May be feasible and planned
Alternative Research Opportunities or Re-flight Opportunities	No alternative or re-flight opportunities	Few or no alternative or re-flight opportunities	Some or few alternative or re-flight opportunities	Significant alternative or re-flight opportunities
Examples	HST, Cassini, JIMO, JWST	MER, MRO, Discovery payloads, ISS Facility Class Payloads, Attached ISS payloads	ESSP, Explorer payloads, MIDEX, ISS complex subrack payloads	SPARTAN, GAS Can, technology demonstrators, simple ISS, express middeck and subrack payloads, SMEX

6. Is your component space-qualified? EnSilica

Again, a host of mitigation techniques can be deployed, including the incorporation of some form of redundancy or ECC into the system. On the analog side, it's advisable to monitor the voltage and current carefully—if there's a latch-up, you can more easily detect it and shut things down quickly.

And silicon layout plays a crucial role. Here on Earth, there's always a push to put the metal tracks closer and closer together with each generation, with designs taking them to the absolute limits of what the technology can support. However, for electronics designed for use in space, it's advisable to increase the separation of the critical node to give greater protection.

So, is Your Chip Space-Qualified?

Can you use something off the shelf? It's a little (lot) more difficult than that, and the answer, of course, is "it depends." NASA has tried to define four classes: A,B,C, and D (**Fig. 6**). These depend on the mission and its lifetime. For example, the James Webb Space Telescope is Class A (*see opening image*).

Conclusion

The ionizing radiation that electronic components will undergo in space can cause significant damage if it's not considered from the beginning of their design.

Several mitigation techniques can be deployed. However, cost and size limitations prevent them being used throughout a system. Thus, careful cost vs. risk analyses must be performed when developing the system as a whole.

**The opening image of the James Webb Space Telescope is credited to [NASA/Desiree Stover](#).*

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CHAPTER 2:

Credit: Nmedia

New Radiation-Hardened GaN HEMT for Next-Generation Space Missions

INTERNATIONAL RECTIFIER

The demand for greater communication bandwidth on a global scale is insatiable and undeniable. As a result, next-gen satellites must deliver higher data throughput for digital payloads. Among in-orbit configuration, edge-computing, and other advanced needs, current FPGAs and ASICs call for greater and more innovative power requirements. The shift to digital payloads requires engineers to reassess key design parameters, such as material needs, operational factors, and radiation robustness, to ensure optimal performance in their space power systems.

For generations, silicon (Si) has been the industry's material of choice in power applications, but in recent years, gallium nitride (GaN) has shown real promise offering a multitude of advantages in applications where reaching high switching speeds and efficiency are just as important as minimizing the size and weight of a power system. Continue reading to learn more about GaN for space applications, the benefits of using a wide band gap semiconductor to optimize operations, and its performance as a radiation-hardened (rad-hard) High Electron Mobility Transistor (HEMT). Discover the industry's

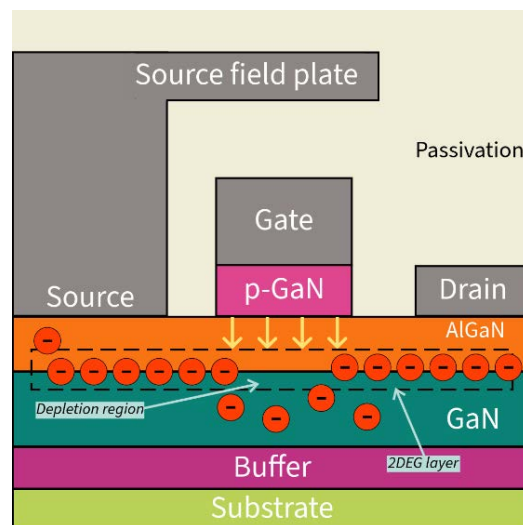


Figure 1: Cross-sectional material of GaN HEMT (Infineon IR HiRel)

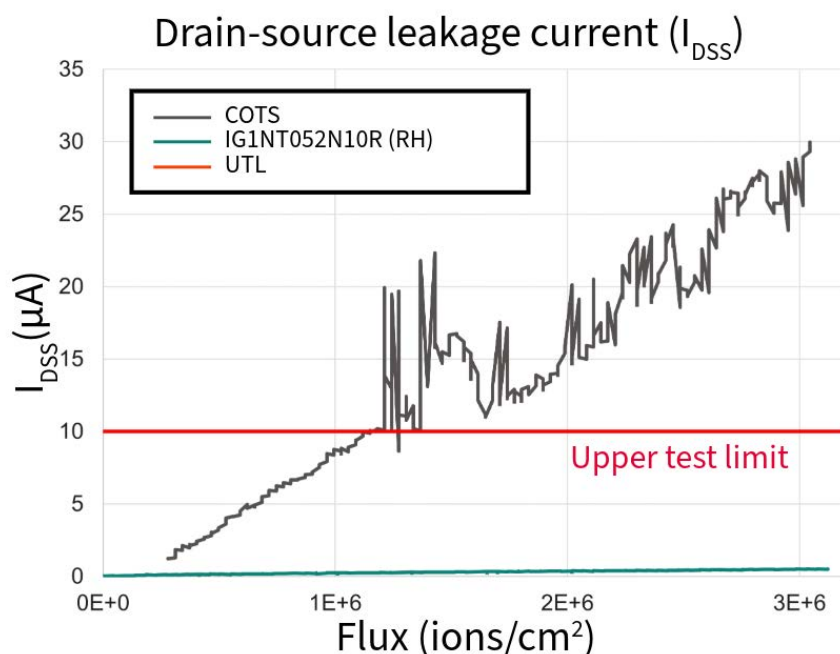


Figure 2: SEE Flux radiation vs Drain-source leakage current (Infineon IR HiRel)

first internally manufactured [rad-hard GaN transistor](#) with Joint Army Navy Space (JANS) qualification from Infineon IR HiRel.

Technological Architecture of GaN

GaN holds a wide bandgap energy of ~3.4 eV. In comparison, legacy technology, such as Si, has a wide bandgap energy of ~1.1 eV. The material properties of wide bandgap semiconductors such as GaN make the technology attractive as power transistors. **Figure 1** illustrates the general design of Infineon IR HiRel's lateral GaN HEMT, [IG1NT052N10R](#). Electrons move from source to drain through a “2-dimensional electron gas” (2DEG) layer formed at the AlGaN and GaN epi heterojunction layer. This is a result of a piezoelectric effect that occurs at the interface between the two layers. A layer of positively doped GaN, p-GaN, is integrated between the gate and AlGaN layer to produce a depletion region. The inclusion of a p-GaN layer allows the transistor to face a low, positive threshold voltage and perform as an

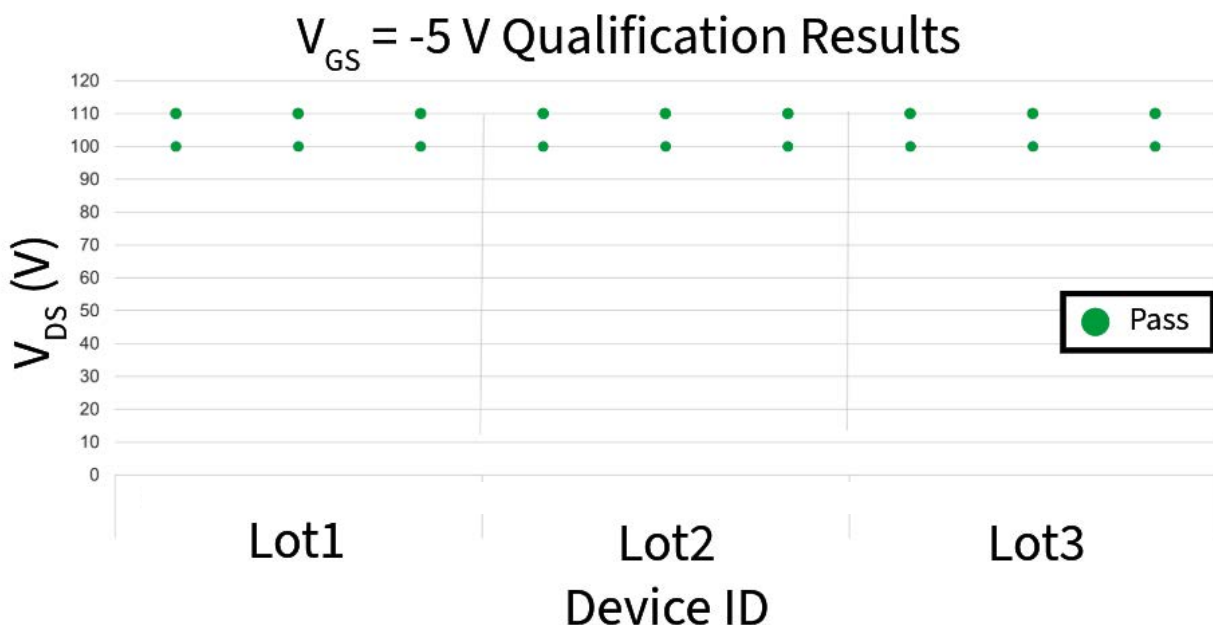
enhancement-mode device. This structure plays a role in the benefits of GaN as a power transistor technology. The source field plate contributes to the improved breakdown voltage as it reduces the peak electric fields found on the gate. The 2DEG layer allows high mobility of electrons with minimal drain-source resistance ($R_{DS(on)}$), a key parameter to account for in power transistors. Low V_{th} , such as 1.5 V for IG1NT052N10R, results in higher switching speeds. The structure of a lateral GaN HEMT also lacks a gate oxide that is typically observed in Si MOSFETs. As a result, GaN has a slight robustness to radiation inherent to its design. Rad hard by design is still applicable to GaN as there are some parameters that need to be mitigated under radiation.

Optimized Radiation and Power Performance

There is some inherent robustness to GaN under various radiation effects due to the absence of a gate oxide. GaN faces no trapped charge nor $V_{GS(th)}$ shift under Total Ionizing Dose (TID) radiation and does not suffer from Single Event Gate Rupture (SEGR) under Single Event Effect (SEE). Even though GaN boasts inherent radiation resistance, there is still an advantage to choosing radiation hardened solutions over commercial-off-the-shelf (COTS) parts for space applications. **Figure 2** demonstrates the importance of creating a GaN transistor radiation hardened by design. Comparing a COTS-graded GaN to a rad hard GaN, we see the COTS device significantly drift while the rad hard GaN remains relatively stable over the entire duration. Rad hard by design will almost always ensure the reliability required in extreme environment applications.

Despite the benefits GaN's technological set up has over Si, it is still crucial for engineers to design the device to perform efficiently under radiation. **Figure 3** highlights the radiation robustness of GaN under SEE for 3 different lots tested up to Au. In addition to

Figure 3: SEE SOA for IFX IR HiRel 100 V rad-hard GaN HEMT (Infineon IR HiRel)



how the GaN device under testing does not require derating when subjected to LET of 70 MeV*cm²/mg (the LET Si equivalent to 86.5 MeV*cm²/mg), the electrical operation of the device is up to standard with the industry's leading rad hard transistor standards. To make sure the device is suitable for power architectures in space systems, Infineon IR HiRel created a new package specifically for [GaN](#), called the PowIR-SMD.

Best-in-class Packaging

Innovative semiconductor technology requires optimal packaging to perform at its best. Infineon IR HiRel developed a new surface mount package to ensure utmost reliability and robust operations for its rad hard GaN device.

Minimizing parasitic inductance is imperative in system design, especially because GaN is a fast-switching technology. With this in mind, we developed the PowIR-SMD to be a bond-wire-free SMD package that has an extremely low inductance value of 0.1 nH. Additionally, this package allows a kelvin-source connection to decouple the gate drive from the power stage, lowering the common-source inductance of the device. Another factor to address is the CTE mismatch between the packaged device and the PCB. Occasionally, ceramics

such as Alumina are developed into hermetic packaging to address such mismatches. This is seen with Si MOSFETs where the devices are large enough to dissipate the heat generated. The high density of GaN allows the technology to perform efficiently within a smaller form factor compared to Si MOSFETs.



Figure 4: A three-dimensional representation of the PowIR-SMD, a new space-grade, hermetic package dedicated for GaN design

Consequently, packages dedicated to GaN would benefit from developing a package consisting of Aluminum nitride, AlN. The higher thermal conductivity of AlN compared to alumina, 150 W/m²K versus 12 W/m²K respectively, allows the device to dissipate heat more effectively. The size of GaN, in this case, is small enough to mitigate the thermal cycling mechanical stress concern that is considered when using AlN. The inclusion of AlN holds an additional benefit as it lessens the accumulation of free charges from environmental radiation, preventing system damage and contributing to inherent radiation robustness. **Figure 4** illustrates the surface mount packaging dedicated to addressing GaN usage in space.

Conclusion

The increasing demand for higher processing power in satellites has led to a growing need for advanced technologies that can efficiently handle complex tasks such as artificial intelligence, in-orbit reconfiguration, and more. High-power FPGAs and ASICs are being driven to their limits, and as a result, improved efficiency and reduction in size and weight are critical factors to consider in satellite design.

Infineon IR HiRel's [rad hard GaN HEMT](#) brings top-of-the-line radiation performance and electrical robustness to the high reliability market. Our 100 V rad hard GaN HEMT, now available under MIL-PRF-19500 JANS qualification, has been designed to optimize higher performances in power systems.

To learn more about Infineon Technologies IR HiRel (IFX IR HiRI)'s rad hard GaN product, please visit <https://www.infineon.com/products/high-reliability/space/power/rad-hard-gan>.

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CHAPTER 3:

Rad-Hard-by-Design: GaN Semis for Next-Gen Space and Defense Systems

STEVE TARANOVICH, Freelance Technical Writer, *Phoenix Information Communication LLC*

Enter the realm of radiation hardness and space-qualified power system designs that employ gallium-nitride power semiconductors.

Spacecraft must have [radiation-hardened \(rad-hard\) electronics on board](#) simply because radiation can cause electronic equipment to malfunction. Thus, power-management devices are critical for powering all of the electronics on board satellites and spacecraft, especially when astronauts are present within the spacecraft. For instance, deep-space missions will likely encounter [neutrons from background radiation](#) or radioisotope thermal generators (RTGs), as well as other harmful nuclear sources (**Fig. 1**). And terrestrial and atmospheric environments may be exposed to galactic cosmic rays (GCRs) along with secondary emissions.

Moreover, long-term radiation effects in space can affect astronauts and spacecraft electronics. [Total ionizing dose \(TID\) levels](#), which will be received at the component die level, are calculated for active parts while taking into account the spacecraft's defensive shielding. Protons and electrons will typically lead to a cumulation of long-term damage in space.

Called displacement damage (DD), it will cause extensive non-ionizing damage (this is usually not applicable to CMOS microelectronics). Transient effects can be affected by single-charged particle effects (single-event effects or SEEs) along with hard (destructive) or soft errors.

Why “Radiation-Hardened by Design” is Important

Designers can combat such damage with a radiation-hardened by design (RHBD) method, which will help meet performance, cost, and availability needs. Consequently, demand is great for high-performance semiconductors in real-time imaging applications among the space and defense sectors. However, the availability of components is quite limited,

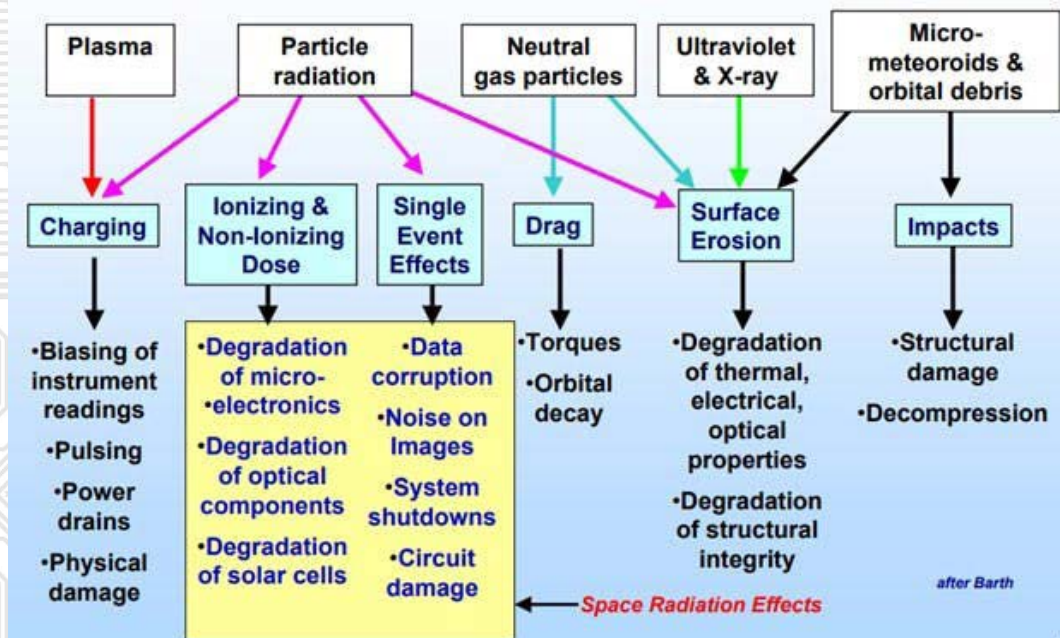
creating challenges within the RHBD industry.

This, coupled with high radiation-tolerant electronics larger than 1 milligray (mGy), a unit of absorbed radiation equivalent to one thousandth of a gray, or 0.1 rad for nuclear fusion and small modular reactors (SMRs), is restricted due to performance and limited availability.

There are now two solutions to utilize electronic components in harsh (radiation-filled) environments:

- Upscreening of commercial off-the-shelf (COTS) components.

- [Use of space-grade radiation-hardened electronics.](#)



1. The space environment induces an array of harsh effects. NASA

RHBD is a door-opener to applications that require extremely high-dose-tolerant ICs and meet the demanding reliability and electronic performance guidelines of the space and military industries.

Rad-Hard GaN Wide-Bandgap Power Semiconductors

Some people think that wide-bandgap (WBG) semiconductors are naturally radiation-hard. However, the “inherent” radiation hardness of WBG semiconductors typically refers to their tolerance of total

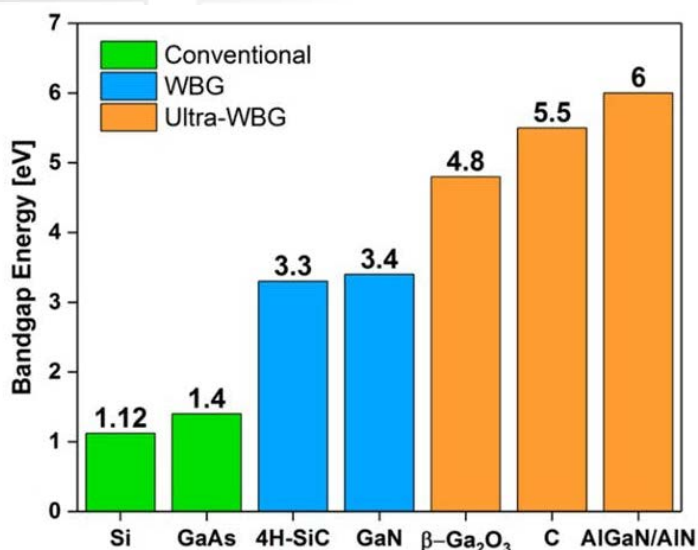
dose. The total dose for WBG semiconductors (**Fig. 2**) refers to their tolerance to radiation, specifically their ability to withstand ionizing radiation without significant degradation.

Radiation hardness assurance (RHA) is defined as the activities undertaken to ensure that the electronics and materials in a space system can perform to the design specifications after exposure to the natural space radiation environment.

Spacecraft, along with some key avionic power systems, include lunar and planetary surface power, Mars transport and lunar gateway, small fission reactors, small satellites, and electric aircraft. Scientific payloads and instruments, such as LiDAR and mass spectrometers (**Fig. 3**), are also included.

GaN WBG Technology: Size, Weight, and Power (SWaP)

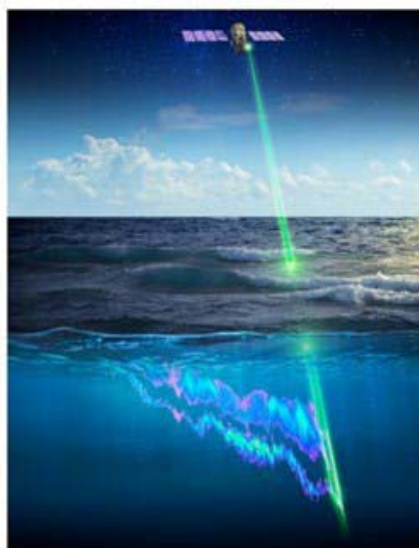
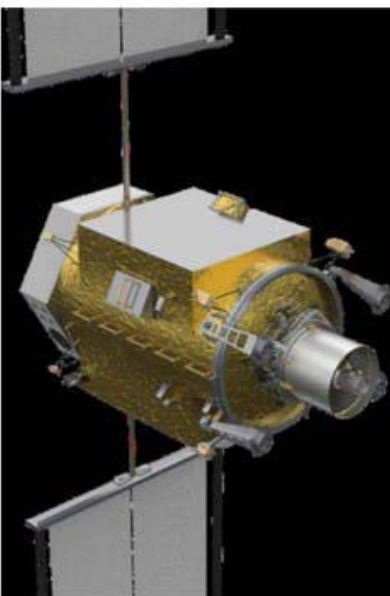
GaN has a fast-switching superjunction technology with voltages under 650 V. The GaN high electron mobility transistor (HEMT) structure (**Fig. 4**) enables a two-dimensional route for



2. An overview of WBG technology, highlighting properties associated with Bandgap Energy. NASA

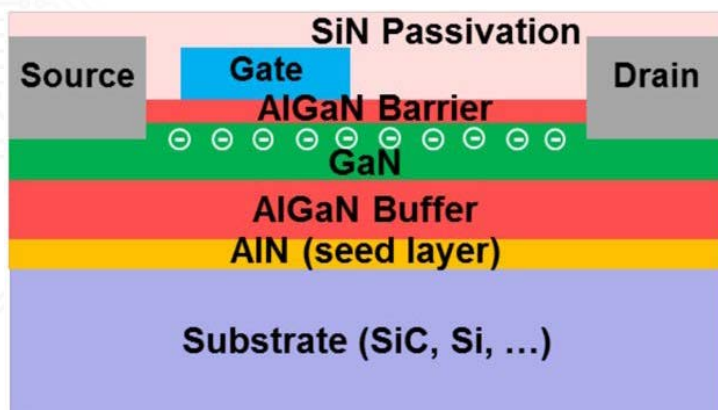
the flow of electrons. Charge polarization and lattice strain are between the AlGaIn barrier and the GaN layer.

WBG semiconductors exhibit “inherent” rad-hard tolerance of total dose. The threshold energy, along with the ionization energy for defect formation, i.e., the atomic bond strength, exceeds that of a silicon device. WBG devices are capable of operating at high temperatures, which may help mitigate radiation dose effects. Early WBG devices didn’t have gate oxides.



3. Shown are aerospace drivers for WBG RHA. NASA GSFC

4. A GaN HEMT has high mobility, which is achieved without the need for doping.
NASA GSFC



GaN HEMT’s High Mobility is Achieved Without Doping

Designers must beware of SEEs. WBG devices are vulnerable to heavy-ion-induced catastrophic single-event burnout in both SiC and GaN power devices. Higher energy for charge ionization will not provide immunity to SEEs. GaN HEMT SEEs exhibit single-event burnout (SEB), leakage current degradation, and single-event dielectric rupture (SEDR).

The *table* shows an example of analysis requirements that depend on SEE sensitivity. Heavy ion- and proton-induced SEE rates can be calculated in the presence of quiet and under solar event conditions.

GaN HEMT Displacement Damage Dose effects

Displacement damage dose (DDD) parameter degradation in GaN HEMTs will happen at DDD levels higher than those for typical space applications.

- DDD effects in GaN HEMTs:
- A threshold voltage shift (typically positive)
- Decreased drain current
- Decreased mobility and transconductance
- DDD susceptibility becomes greater when:
- Component parts are biased during irradiation
- Parts have had prior hot-carrier stress

IMPACT OF DIFFERENT DESIGN AND TECHNOLOGY PARAMETERS ON ESD ROBUSTNESS, FAILURE MECHANISM, AND FAILURE LOCATION IN GAN HEMTS						
ESD Test Structure	MESA	Gate	V_{Trig}	I_{t2}	Failure Spot	Failure Mechanism
w/o MESA & w/o Gate	No	No	Low	Low	At Source/Drain corners	Crack formation in AlGaIn barrier near source/drain contact corners & metal diffusion via cracks
w/ MESA & w/o Gate	Yes	No	Improved	Improved	In channel region	Crack formation in AlGaIn barrier & channel and metal diffusion via cracks
w/ MESA & Floating gate	Yes	Floating	Improved	Improved	At MESA edge under the gate	MESA Schottky turn-ON due to C_{gd} coupling
w/ MESA & grounded gate	Yes	Grounded	High	High	At Gate finger	Gate finger blows-off due to mechanical strain near gate edge
w/ MESA & Surface Passivation	Yes	Grounded	High	High	At Gate finger	Gate metal finger blew-off due to mechanical strain between gate and drain
p-GaN Cap Gate (commercial) HEMT	NA	Grounded	High	High	In Gate Region	Gate bus bar blew-off due to mechanical strain between drain and gate

Distinct failure modes of AlGaIn/GaN HEMTs under ESD conditions. IEEE Transactions on Electron Devices 2020

GaN HEMT Total Ionizing Dose

GaN FETs in power applications open the door to new technology trends in the cold void of outer space. Demand is great for an easy-to-use pulse-width modulation (PWM) controller, with a high-reliability integrated circuit (IC), which will be able to directly drive GaN power FETs.

In previous research, COTS GaN power transistors were exposed to TID effects via 10-keV X-rays. Such GaN HEMTs were tested in both on- and off-state bias conditions. These GaN switching tests were conducted before, during, and after irradiation, and the devices were characterized at temperatures ranging from -50 to $+75^{\circ}\text{C}$. The results indicate that GaN technology, with a bandgap of 3.4 eV, is a promising candidate for use in harsh environments.

HEMT devices have heterojunctions, in which electrons are confined to a quantum well, thereby avoiding impurity scattering. These devices are also known as two-dimensional electron gas field-effect transistors (TEGFETs).

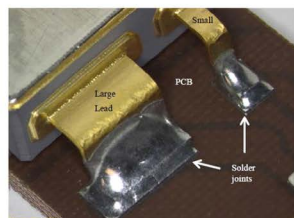
Summary

GaN devices exhibit significantly higher radiation hardness than their Si and GaAs counterparts, primarily due to the high bond strength in III-nitride materials. GaN's response to radiation damage is a function of radiation dose, type, and energy, coupled with carrier and dislocation density, as well as impurity content density.

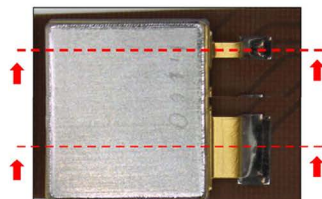
Rad-hard by design makes possible applications requiring a very high-dose tolerance for ICs, while also meeting demanding electronic and reliability performance guidelines in the space and military industries.

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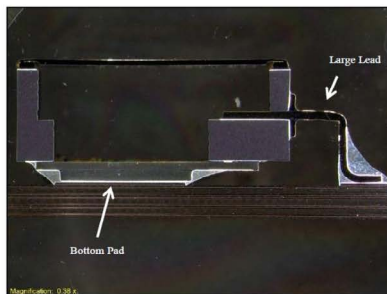
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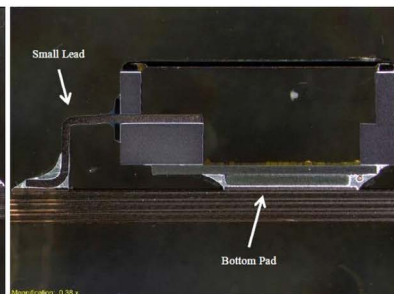
SuplR-SMD close up view of large & small lead solder joints



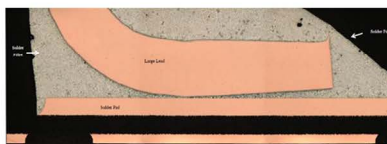
SuplR-SMD cross section plane & direction of cuts, large & small leads



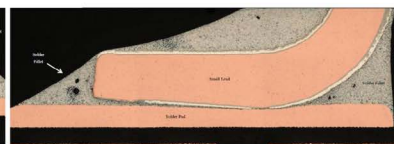
SuplR-SMD package cut view, one side, large lead (0.38x magnification)



SuplR-SMD package cut view, one side, small lead (0.38x magnification)



SuplR-SMD cross section of large lead



SuplR-SMD cross section of small lead

CHAPTER 4:

Board-Level Qualification Testing for Rad-Hard MOSFET Packaging

ANDREW POPP, *Infineon Technologies*

High-reliability rad hard MOSFETs undergo extensive screening and quality conformance testing to ensure that devices perform to specification in the harshest environments.

For Defense Logistics Agency (DLA) QPL qualification, high-reliability rad-hard MOSFETs undergo extensive screening and quality-conformance testing to ensure that devices perform to specification in the harshest environments, sometimes for 15 years and longer. Both the U.S. and European communities have developed specifications detailing quality conformance testing sequence.

In the U.S., DLA's MIL-PRF-19500 and MIL-STD-750 govern the quality conformance testing sequence performed on discrete MOSFET semiconductors manufactured to JANS or JANTXV levels. In Europe, ESA's ESCC 5000 is the standard for discrete semiconductors, hermetically sealed and die.

These tests are performed at the chip or package level, per applicable standards. In real life, rad-hard MOSFETs are mounted to boards for use in subsystems, such as DC-DC converters, intermediate bus converters, motor controllers, and others. Yet PCB-level performance testing is not required by DLA or MIL standard. That's why with our newest package designs, International Rectifier HiRel (IR HiRel) developed a series of board-level qualification tests to provide even greater levels of assurance to our customers.

Packaging for higher reliability

In space-rated power electronics, reliable attachment of surface-mount hermetically-packaged MOSFETs to PCBs has dogged space system designers for years. Material differences, specifically coefficient of thermal expansion (CTE) mismatch of the board and surface mount power package, can make it difficult to maintain reliable solder joints between the PCB and SMD package. CTE mismatch also makes it challenging to preserve the sealed integrity of a hermetically packaged silicon power MOSFET.

IR HiRel developed the SuplR-SMD package as a way to overcome the issue of CTE mismatch between a power semiconductor and PCB. Designed for direct-to-PCB surface mount attach, SuplR-SMD enables the shortest thermal conduction path to help optimize

power system efficiency. Standard qualification for new devices housed in SupIR-SMD is JANS level per MIL-PRF-19500.

Typical applications range from space exploration vehicles to communications, navigation, and observation satellites, and more. These vehicles may fly at low Earth, geostationary, or highly elliptical orbits, or interplanetary, deep space missions. While the flight environments may differ greatly, we know that each space program must be evaluated vis-à-vis its mission profile needs including, but not limited to:

- Reliability
- Radiation tolerance
- Environmental stresses
- Expected mission life cycle

Beyond that, space electronics must withstand tremendous forces from the launch environment itself. Extreme shock and vibration, ESD discharge, vast temperature swings and more...high-reliability electronics are designed to endure much harsher conditions than COTS parts were ever meant to face. IR HiRel's rad-hard silicon power MOSFETs undergo extensive testing at the chip or package level per the applicable standard(s) to ensure performance to specification in the harsh space environment. In this case, it is typically qualified to MIL-PRF-19500 JANS level.

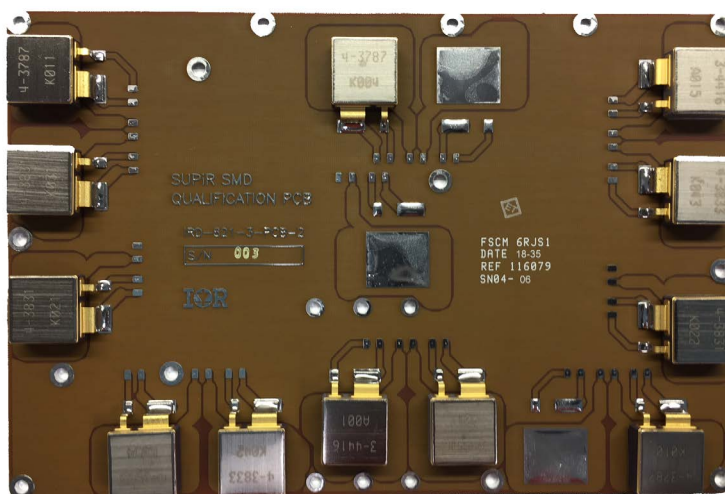
The goal of PCB-level test procedures is to validate the package design integrity through next-level assembly and environmental testing operations. Broadly speaking, these board-level protocols include:

- Random vibration
- Mechanical shock
- Temperature cycling
- Post-test inspection for fine and gross leak, and cross-sectioning of solder joints

Sequential Qualification Tests

For example, to qualify the SupIR-SMD package at the board-level, we mounted several packages in various orientations and positions on a representative PCB. With

polyimide glass fiber as the board material, per IPC 4101/411, the PCB had eight layers and an overall board thickness of 1.8 mm. Using SN63Pb37 solder and RMA flux, we attached components to the PCB. The solder stencil was 8 mils thick, with a 90% ratio of opening to pad size. Prior to testing, we inspected the whole assembly according to



Test characteristics	MIL-STD-883J TM2026 condition 1J	ECSS-Q-ST-70-08* Table 13-3, launcher applications	ECSS-Q-ST-70-08* Table 13-4, non-launcher applications		IPC-TM-650 Test condition F	IR HiRel PCB board-level parameters
			Perpendicular to PCB	Parallel to PCB		
Power spectral density	1.0 g ² /Hz	+3 dB/octave (20 – 60 Hz)	+6 dB/octave (20 – 100 Hz)	+6 dB/octave (20 – 100 Hz)	0.008 g ² /Hz (0 – 10 Hz)	+6 dB/octave (20 – 100 Hz)
		0.27 g ² /Hz (60 – 100 Hz)	1.0 g ² /Hz (100 – 500 Hz)	0.5 g ² /Hz (100 – 800 Hz)	+3 dB/octave (10 – 75 Hz)	1 g ² /Hz (100 – 1000 Hz)
		-6 dB/octave (1000 – 2000 Hz)	-6 dB/octave (500 – 2000 Hz)	-3 dB/octave (800 – 2000 Hz)	0.06 g ² /Hz (75 – 2000 Hz)	-3 dB/octave (1000 – 1500 Hz)
G _{rms}	36.6	20	28.5	27.1	10.9	39.9
Duration	15 minutes/axis	5 minutes/axis	5 minutes/axis		15 minutes/axis	5 minutes/axis

*ECSS-Q-ST-70-38C includes by reference test conditions outlined in ECSS-Q-ST-70-08C, as summarized here.

IPC-J Standard, Space Addendum². Then we subjected the board to random vibration, mechanical shock and temperature cycling. In order to proceed through each stage of mechanical stress tests, the assemblies had to remain failure-free.

Random vibration

The random vibration test simulates spacecraft launch and Grms (root-mean-square acceleration) that the electronics must endure. We tested in accordance with ECSS-Q-ST-70-38C³, with the test level increased to 40 Grms. Note that this standard includes by reference test conditions outlined in ECSS-Q-ST-70-08C⁴. Based on IR HiRel's space power electronics experience and our customer needs, increasing the test conditions more accurately reflects what parts actually face in launch settings. This is also closer to MIL-STD-883J⁵ Test Method 2026, Condition 1J, which requires 36.6 Grms.

Our test setup vibrated the SuplR-SMD board assemblies in three dimensions, up to 40 Grms for five minutes in each dimension, which exceeds the ECSS standard. For comparison, IPC-TM-650⁵ test condition F is the closest equivalent to these ECSS and MIL-STD-883 standards, but far less intense, with a required test level of only 10.9 Grms.

Mechanical shock

The mechanical shock test simulates the sudden and extreme accelerations or decelerations caused by launch sequence engine separations. As a baseline reference, we

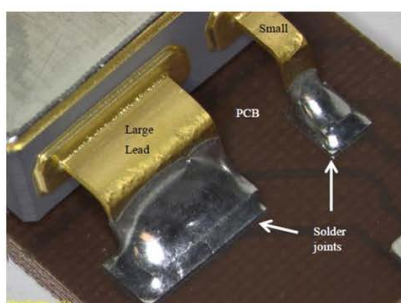
Test characteristics	MIL-STD-883J TM 2002.5 condition B	ECSS-Q-ST-70-38C	IPC-TM-650 TM 3.8 A condition E	IR HiRel PCB board-level parameters
Peak acceleration (G)	1,500	Should “meet the intended mission with margin”	1,000	1,500
Pulse duration (ms)	0.5		0.5	0.3
Shocks/axis	5		3	3
Total shocks	30		18	18

Test characteristics	MIL-STD-750F TM 1051 condition A	ECSS-Q-ST-70-08C*	IPC-9701A Test condition 5 NTC=B	IR HiRel PCB board-level parameters
Temperature range	-55°C – 85°C	-55°C – 100°C	-55°C – 100°C	-55°C – 100°C
Ramp rate	≤ 15°C/minute	≥ 10°C/minute	≥ 20°C/minute	≥ 10°C/minute
Minimum dwell time	10 minutes	15 minutes	10 minutes	15 minutes
# of thermal cycles	Minimum 20, or as specified	200	500	500

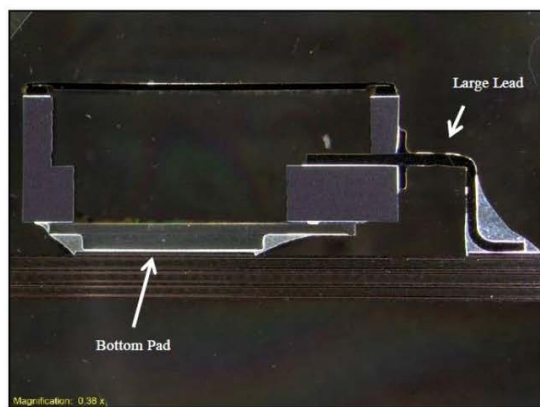
*ECSS-Q-ST-70-38C includes by reference test conditions outlined in ECSS-Q-ST-70-08C, as summarized here.

started with MIL-STD-883J4 Test Method 2002.5, Condition B, which is part of IR HiRel's usual package-level qualification for MOSFETs. We also considered ECSS-Q-ST-70-38C5, which specifies that shock levels should “meet intended mission with margin.” IPC-TM-6506 Test Method 3.8 A, Condition E is similar to the MIL standard, but less intense, specifying a peak acceleration of 1,000 Gs with three shocks in each direction per axis and a pulse duration of 0.5 ms.

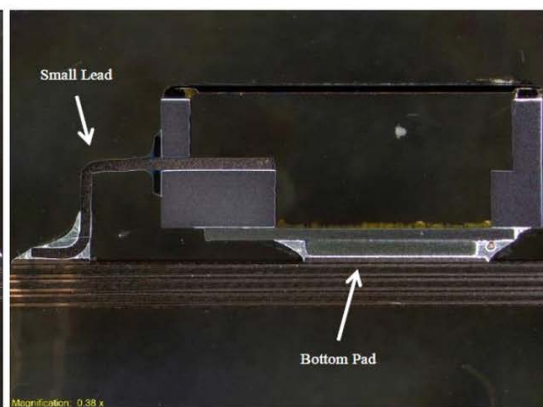
For our PCB-level tests, we subjected the SupIR-SMD assemblies to a minimum of 1,500 Gs peak acceleration for 0.3 ms, shocking them in positive and negative directions each in X1, Y1 and Z1 directions. With six shocks per axis, we performed 18 shocks in total. These test parameters are in line with our global customer requirements for standard space equipment.



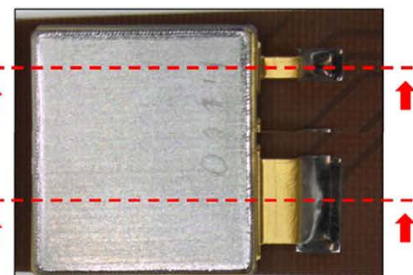
SupIR-SMD close up view of large & small lead solder joints



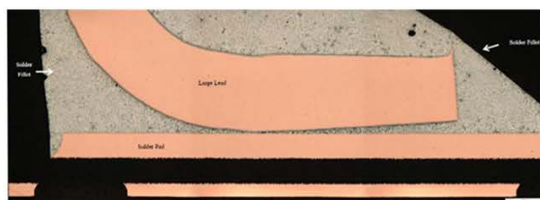
SupIR-SMD package cut view, one side, large lead (0.38x magnification)



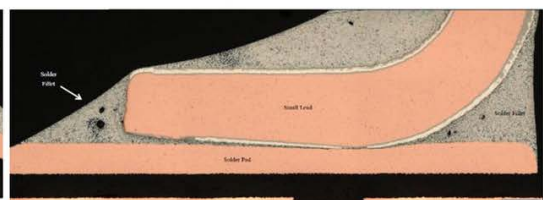
SupIR-SMD package cut view, one side, small lead (0.38x magnification)



SupIR-SMD cross section plane & direction of cuts, large & small leads



SupIR-SMD cross section of large lead



SupIR-SMD cross section of small lead

#	Test	Conditions
1	Random vibration	ECSS-Q-ST-70-38C with test level increased to 40 G _{rms} (MIL-STD-883, Test Method 2026 1J requires 36.6 G _{rms})
2	Mechanical shock	ECSS-Q-ST-70-38C (1,500 G, 0.3 ms) MIL-STD-883, Test Method 2002 3x in positive and negative directions each in X1, Y1 and Z1 directions 6 shocks per axis, 18 shocks total
3	Temperature cycling	ECSS-Q-ST-70-38C (-55°C to +100°C) Ramp not to exceed 10°C/minute Dwell minimum 15 minutes at each extreme 500 cycles
4	Cross-section of solder joints	ECSS-Q-ST-70-38C Cracks in solder shall not exceed 25% of the lap connection in the critical zone

Temperature cycling

This test simulates the extreme operational temperatures space electronics must withstand in flight. We subjected the SupIR-SMD assemblies to the thermal cycling based on ECSS-Q-ST-70-38C (-55°C to 100°C). Specifically for the board assemblies, we applied 500 temperature cycles from -55°C to 100°C with a maximum 10°C/minute ramp and a minimum 15 minute dwell time at each extreme, which is more intensive than specified by the standards for package qualification.

These parameters are similar to IPC-9701A7, but with an increased dwell time and decreased ramp rate. MIL-STD-750F for package qualification isn't directly comparable to either the ECSS or IPC standards which both use a test condition from -55°C to 100°C, whereas MIL-STD-750F specifies -55°C to 85°C. ECSS-Q-ST-70-38C and MIL-STD-750F standards also specify fewer number of cycles, 200 and 20, or as specified, respectively.

Cross-section inspection of solder joints

After completion of these tests, we cross-sectioned the assembly solder joints in accordance with ECSS-Q-ST-70-38C, which specifies requirements for qualification of PCB technology. Pass criterion for this test is that cracks in the solder shall not exceed 25% of the lap connection in the critical zone. There shall also be no cracks in the ceramic. Since the ECSS standard doesn't allow for any ceramic cracks in SMD devices, it is stricter than the MIL-STD-7508 Test Method 2071 and MIL-STD-883 Test Method 2009 alternatives.

Conclusion

Satellite manufacturers worldwide use hi-rel DC-DC converters, and board-level tests subject the power semiconductors to the same rigors expected during space flight lifetime. While there are no mandated industry standards for this type of testing, best-practice board-level protocols should either comply with or exceed the test conditions selected as baselines. We strongly believe this proactive approach and added level of qualification gives a high degree of assurance. Silicon-based technologies remain a trusted choice for use in high-reliability space applications. With its proven heritage, performance, robustness, and well-known screening and reliability standards, pushing to greater levels of test acceptance helps extend that confidence to next-generation silicon platforms.

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CHAPTER 5:

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The 2025 Space Race: What Happened, What Didn't, and What's Coming Next

CABE ATWELL, Technology Editor, *Electronic Design*

A look at how the space race evolved in 2025, key missions that slipped, and why 2026 is looking to be a banner year for lunar and commercial spaceflight.

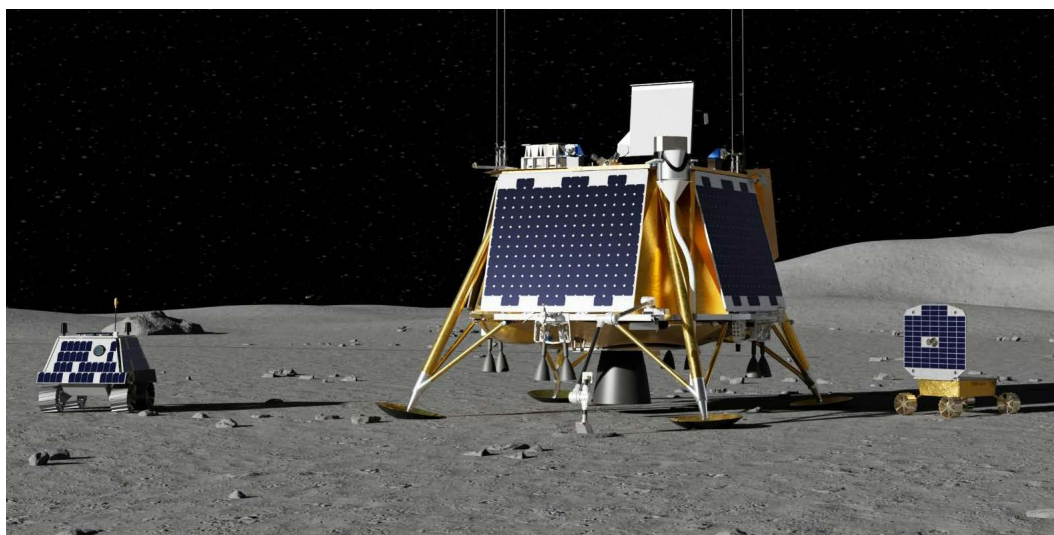
Artimus II was a resounding success. It took humans the furthest away any have ever traveled. First time humans have been anywhere near the Moon since December 19th, 1972. Getting where we are today took countless little steps. The Space Race is back on. Taking a look back, 2025 wasn't defined by a single historic landing or a dramatic first, but rather momentum.

2025 became a transition point, setting up several critical milestones that now spill into 2026. Commercial launch providers dominated activity in orbit throughout the year. SpaceX continued operating at a pace unmatched by any other launch provider, expanding its Starlink constellation via Falcon 9 rockets while refining reusability and operational efficiency.

Redefining Low Earth Orbit

The volume of launches underscored how space access has shifted from rare events to routine deployment. [Low Earth orbit](#) is no longer just a destination for science missions. It's become a working environment supporting communications, defense, and Earth observation on a global scale.

At the same time, competition in heavy-lift launch capability finally became competitive. Blue Origin's [New Glenn](#) rocket made its long-awaited debut, signaling a new contender into a market historically dominated by SpaceX and government-backed vehicles. While New Glenn hasn't matched Falcon Heavy's launch schedule, its arrival introduces redundancy and competition, both key challenges for government and commercial customers looking to diversify launch options heading into the last half of the decade.



1. Firefly Aerospace landed its Ghost Lunar Lander at Mare Crisium near Mons Latreille on the Moon's surface in March 2025. Firefly Aerospace

NASA's Artemis program remained a focal point of the government-led space race, though progress came with familiar caveats. Hardware integration continued with Orion and the Space Launch System, but Artemis II, the first crewed lunar flyby mission, dropped from a late-2025 target into early 2026. The delay cascaded forward, further pushing Artemis III, the mission intended to return humans to the Moon's surface, [beyond its original schedule](#).

These shifts reinforced a growing reality: Deep-space human exploration is advancing, but not on the original timelines due to engineering complexity and political ambition.

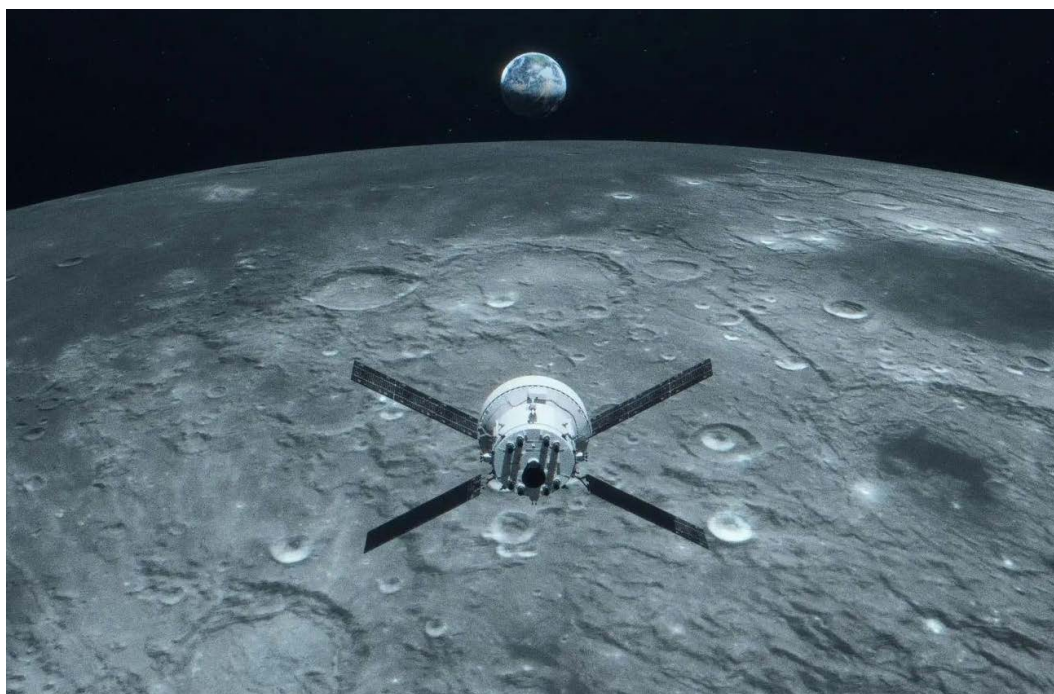
Lunar Landscape

Moon exploration did see meaningful progress via commercial partnerships. Firefly Aerospace successfully landed its [Blue Ghost](#) lunar lander (**Fig. 1**) in early 2025, delivering payloads under NASA's Commercial Lunar Payload Services program.

The mission demonstrated that smaller, private companies can reach the Moon and operate there, even as other efforts, such as ispace's second [Hakuto-R](#) attempt, fell short. The mixed results highlighted both the promise and the risk that comes with commercial lunar exploration, where innovation moves quickly but margins remain thin.

Notably absent in 2025 was a fully operational [Starship](#) system. SpaceX continued flight testing throughout the year, focusing on vehicle design, crew safety, and recovery techniques. While several milestones were achieved, Starship did not yet reach the level of operational readiness required for its role as NASA's lunar human landing system. As a result, Starship remains a central dependency for Artemis III and beyond, tying NASA's lunar ambitions to SpaceX's development timeline.

By the end of 2025, the space race had become less about national prestige and more about infrastructure. Satellites, launch vehicles, lunar landers, and space stations are increasingly viewed as interconnected systems rather than isolated missions. Governments still set strategic goals, but private companies now build and operate much of the hardware that makes those goals achievable.



2. NASA's Artemis II is slated for a lunar flyby by spring of 2026 if schedules hold up. NASA

What are the Expectations for 2026?

Looking ahead to 2026, several long-delayed milestones are expected to converge. NASA is targeting Artemis II for a [crewed lunar flyby](#) (Fig. 2), a mission that would mark humanity's first return to the moon since Apollo. Starship is slated to move closer to operational status, with orbital refueling demonstrations becoming a critical focus. Success in that area would unlock not only lunar missions, but also future Mars-bound advances.

Commercial activity is also expected to intensify. Additional lunar landers are scheduled under [CLPS](#) and international programs, while satellite constellations will further expand. Analysts expect increased focus on space-based infrastructure, including communications, navigation, and Earth monitoring, over symbolic exploration. Even long-term ambitions, such as Mars cargo missions, are increasingly thought of as engineering validation exercises rather than headline-grabbing events.

In retrospect, 2025 will be remembered as a year where the modern space race matured. The technology advanced, the business models stabilized, and the limitations became clearer. The dramatic moments may have been delayed, but the groundwork was laid.

If 2026 delivers on even a portion of what's now scheduled, it could mark the moment when years of incremental progress finally turn into visible, historic achievements that go beyond Earth's orbit.

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