Electronic Design

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Apply Tee Networks to Broaden TIA Required Solutions (Part 2): Loop Gain Plot, Noise, and Single-Supply Operation

Part 2 shows the impact of adding the tee to the op-amp loop gain plot. Mapping that back to the design algebra then reveals the impact the tee has on output noise.

The tee network algebra of Part 1 can be illustrated by adjusting the terms in the loop gain (LG) plot. It gives a visual interpretation of what the tee network is doing.

This article discusses the effect the tee network has on the different output spots and then assesses the integrated noise terms. The required circuit modifications to operate the TIA with the tee network using a single supply are shown. Test-ing the tee in adapting a very demanding 50 MΩ TIA design is then executed, raising the required feedback C_f to equal a typical 0.2 pF parasitic value.

Modifying the LG Plot with the Tee Network

One way to approach the compensation solution for this tee network idea is to adjust each part of the original LG plot of Figure 2 in Part 1, including the effect of that inside-the-loop tee network. The adjustments to get the plot of *Figure 1* include:

- The low frequency noise gain shifts up to $20\log(A_t)$.
- The Z_1 frequency will move out in frequency by A_t as well.
- The inside of the loop tee divider has effectively shifted the amplifier's A_{ol} curve down by that amount. The entire A_{ol} curve shifts down by $20\log(A_t)$.
- Since Z_1 has shifted up the same amount as the gain bandwidth product (GBP) has shifted down, the F_o frequency remains the same.
- Staying with the Butterworth target of setting $P_1 = 0.707 \times F_o$, that frequency hasn't moved with the addition of the tee. Hence, using that lower R_f value, now that we have some tee gain, will shift the required C_f up — maybe into a realizable range for particularly challenging designs.
- The higher frequency noise gain (NG) set by $1+ C_s/C_f$ has moved down by the A_t gain, which, along with the amplifier A_{ol} curve shifting down by A_t, places the F_c frequency at the same place as the design without the tee.

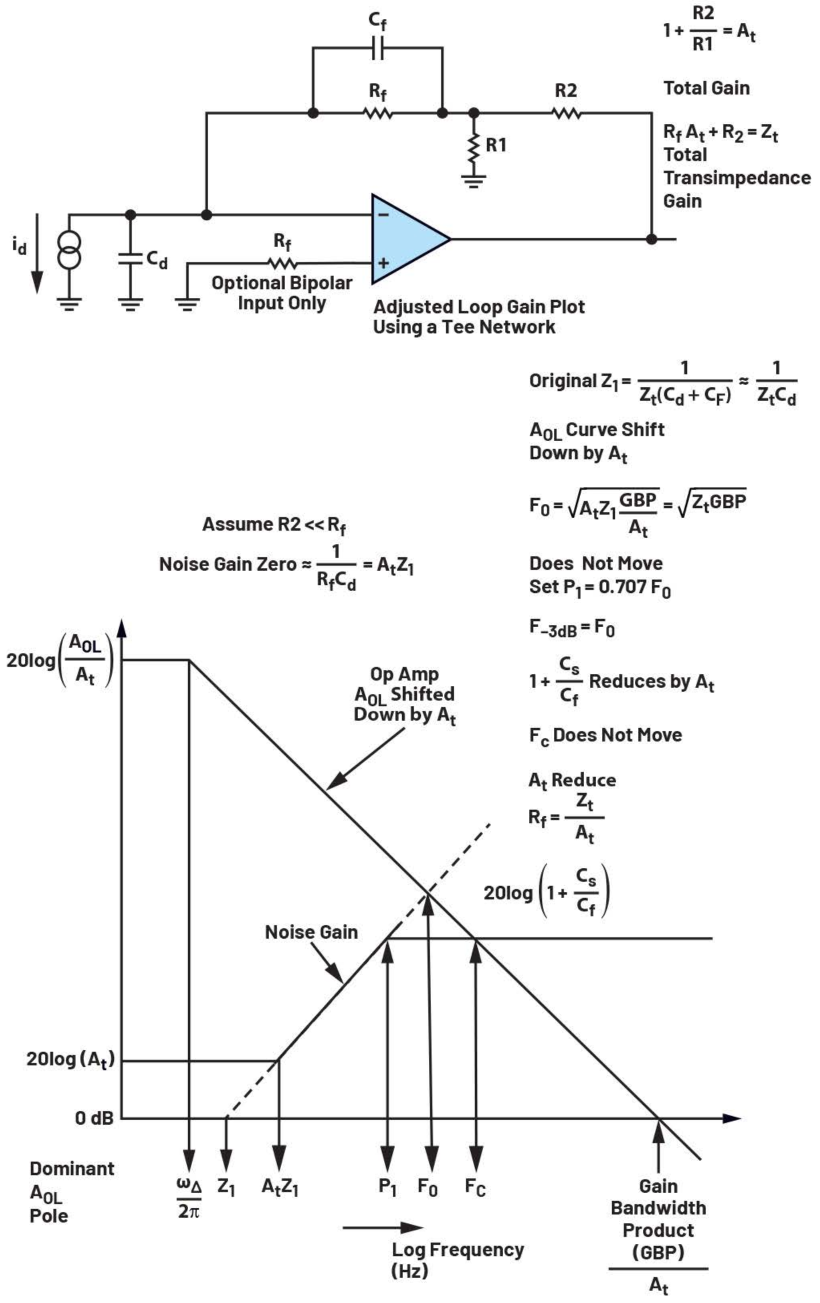
Applying these LG curve modifications to the example of Figure 5 in Part 1 using a tee gain of 2.78 adjusts the key elements on the LG curve to:

- Low-frequency noise gain goes up to 20log(2.78) = 8.9 dB.
- Z_1 ($1/2\pi R_f C_s$) shifts out to 1.63 MHz (from a no tee 556 kHz, 2.78×).
- The effective GBP shifts down to 1.3 GHz/2.78 = 467 MHz.
- The geometric mean of Z1 and GBP (F_o) stays the same at $\sqrt{1.63\text{ MHz} \times 467\text{ MHz}} = 27.6$ MHz.
- Set the feedback pole at the same $0.707 \times F_o = 0.707 \times 27.6\text{ MHz} = 19.5$ MHz.
- The higher C_f value reduces the higher-frequency NG to 1 + 14.3 pF/1.2 pF = 13. That then intersects the lower GBP curve at the same F_c frequency, F_c = 467 MHz/13 = 35.9 MHz. The tee gain has also shifted the minimum stable gain down to 10/2.78 = 3.6, where the new NG2 = 13 comfortably exceeds that.

Total Output Integrated Noise Using the Tee Network

The gains for each of the noise terms will be changed when going to the tee network, except for the op amps' input current noise, which, by definition, will have the same resistive gain using the tee. The input spot voltage noise gets to the output × the noise gain curve, then is band-limited either at the F_c frequency or by a lower bandwidth noise power bandwidth (NPBW) limiting postfilter.

The tee will increase from a gain of 1 to a gain of A_t from



1. Modified LG plot including an inside-the-loop tee network.

low frequencies to the new noise gain zero frequency that's shifted up from the no tee location by the A_t gain. That will be an increased contribution using the tee, but this part of the output integrated noise is usually a very small part of the total and doesn't increase the total by more than 0.5%.

The rising portion of the NG curve will add an equivalent spot noise for integration through P_1 that's identical to the original no tee design. If the NPBW is higher than the P_1 frequency (where the NG goes flat at the now reduced higher-frequency NG set by $1 + C_s / C_f$), it's then gained up by the tee gain to be at the same output level and has the same flat span from P_1 to F_c.

The more significant part of the output integrated noise that's automatically increased by the tee network is the Johnson noise for the feedback resistor. Analyzing that term's spot noise with just the simple R_f resistor and then the solution using a tee network shows that it increases by a $\sqrt{A_t}$ factor. Looking at the original spot noise voltage term, due to the R_f noise, will give:

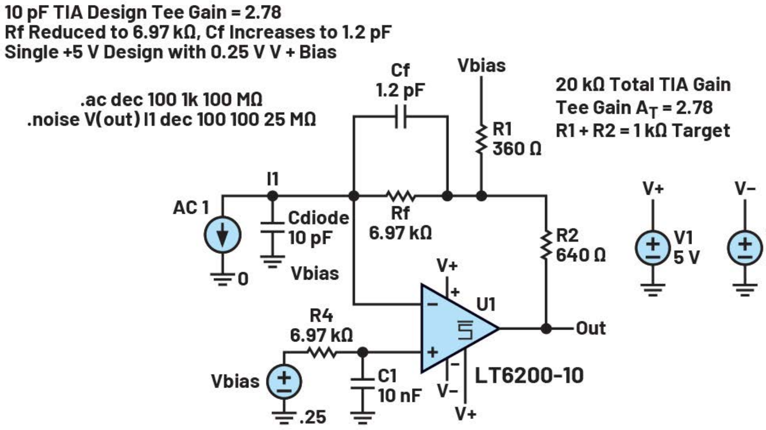
$$e_{o\_R_f} = \sqrt{4kTR_f} \qquad (1)$$

Output spot noise due to the R_f Johnson noise (no tee) will give:

$$e_{o\_R_f} = \sqrt{4kT\frac{R_f}{A_t}} \times A_t = \sqrt{4kTR_fA_t} \qquad (2)$$

Neglecting the small R2 term in the gain and output noise, going to the tee network reduces R_f by A_t. However, it then multiplies that spot noise by a linear A_t value. That adjustment is shown here: R_f' is the reduced R_f value by A_t neglecting the small effect R2 has on the TIA gain and output noise.

From a spot noise perspective at the op amp output, the contribution of the original R_f Johnson noise has been increased by $\sqrt{A_t}$. Often, the resistor noise part of the total equivalent integrated output V_o RMS is a small part of the total. If so, this adjustment will increase the total inte-



2. Adjusting the design to a single 5-V supply.

grated noise only slightly. The R_f in these equations is the original desired gain.

In the example design (Figure 5, Part 1) with NPBW set to 20 MHz, the "no tee" design is dominated by the input current noise × the R_f gain as 86% of the total output noise power. With the tee design, targeting C_f = 1.2 pF increases the simulated integrated noise over 20 MHz from 330 µV RMS with no tee to 351 µV rms (only 6%). The R_f noise contribution increases from 6% of the total to 15% with that $\sqrt{A_t}$ multiplier in its spot noise to the output.

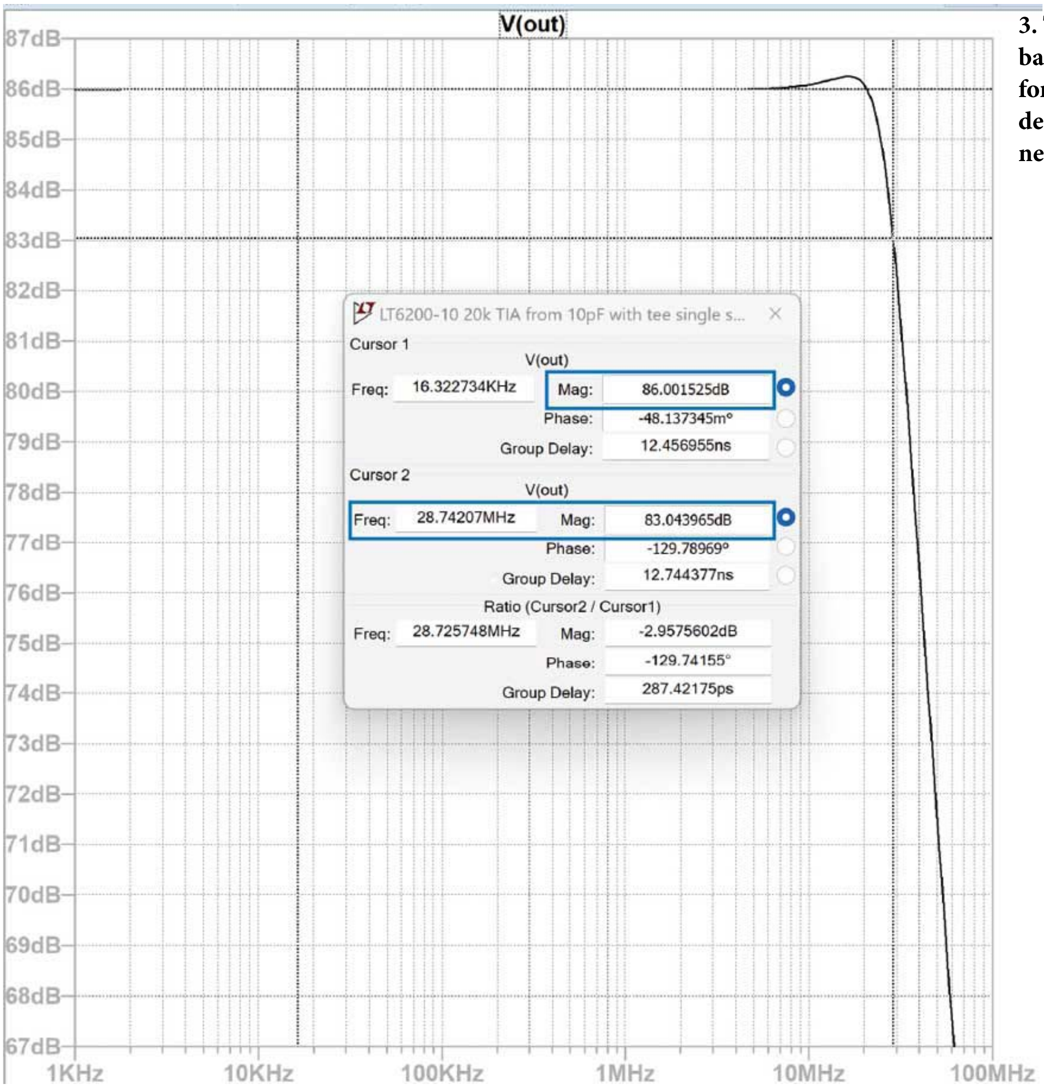
Modifying the Design to a Single Supply

Most TIA designs operate from a unipolar output diode where the op amp is operating with a single supply, and the zero input output voltage is set just above the negative supply rail to keep the output stage out of saturation for a faster, more linear response. The easiest way to operate with an actual ground on the V+ input (part of the diode bias voltage) is to provide a small negative supply (such as –0.25 V) to give adequate headroom to the output stage for typical RR_{OUT} devices like the LT6200-10.

Lacking that negative supply, *Figure 2* shows the design modified to a single 5-V supply with the inputs and output biased to approximately 0.25 V with no diode input current. With that offset on the V+ input, that same voltage will need to be applied to the bottom of the R1 resistor in the tee network to remove it as an output offset term.

This nominal simulation shows 0.236 output DC bias. The V_{BIAS} source into R1 must show a low broadband output impedance with low noise for good broadband TIA performance. Consider buffering V_{BIAS} into R1 using the ADA4899-1.

The small signal AC response of *Figure 3* operating with a single +5-V supply has peaked at a very slight 0.25 dB and



LT6200-10 20k TIA from 10pF with tee single s...

Cursor 1

V(out)

Freq: 16.322734KHz Mag: 86.001525dB ●

Phase: -48.137345m° ○

Group Delay: 12.456955ns ○

Cursor 2

V(out)

Freq: 28.74207MHz Mag: 83.043965dB ●

Phase: -129.78969° ○

Group Delay: 12.744377ns ○

Ratio (Cursor2 / Cursor1)

Freq: 28.725748MHz Mag: -2.9575602dB

Phase: -129.74155°

Group Delay: 287.42175ps

3. The small signal bandwidth (SSBW) for the single-supply design of the tee network.

rolled off at 28.8 MHz — a very slight shift from the supply-centered response using split ±2.5-V supplies of Figure 6 in Part 1. This slight closed-loop response peaking over the balanced supply case is likely due to small shifts in the internal A_{ol} curve. That 0.25-dB peaking maps to a closed-loop Q = 0.8, where a nominal 9% step overshoot should be expected.

Producing a 0.25- to 2.25-V output square wave at 2 MHz is shown in the waveform of *Figure 4*. This overshoots the expected 9% and reveals a good reason to have a little extra headroom on the negative side to keep any overshoot from clipping into the negative supply.

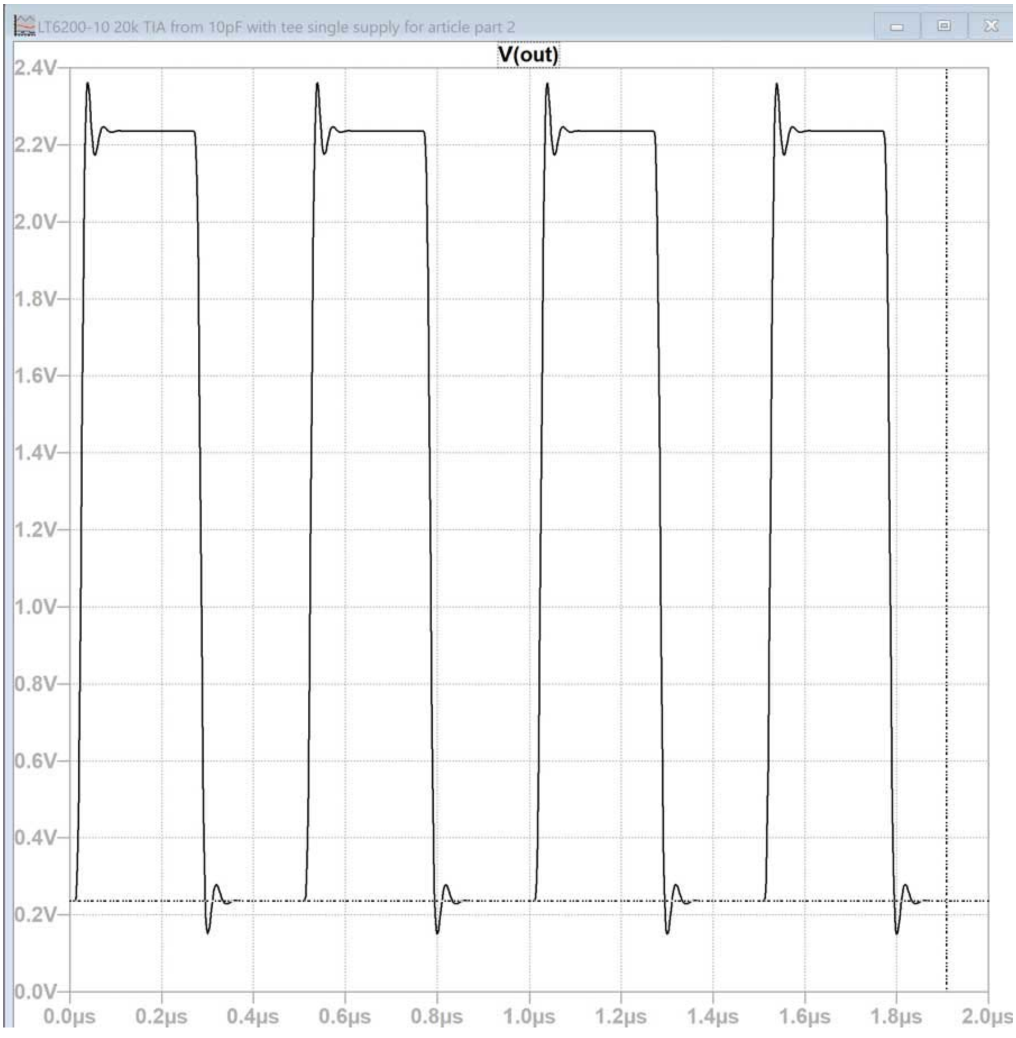
Adjusting the C_f up slightly can be used to reduce this overshoot. Any kind of post-NPBW filter can also be used to reduce this overshoot and should be considered in these designs to control the integrated noise.

Applying the Tee Network Using a JFET Input Device

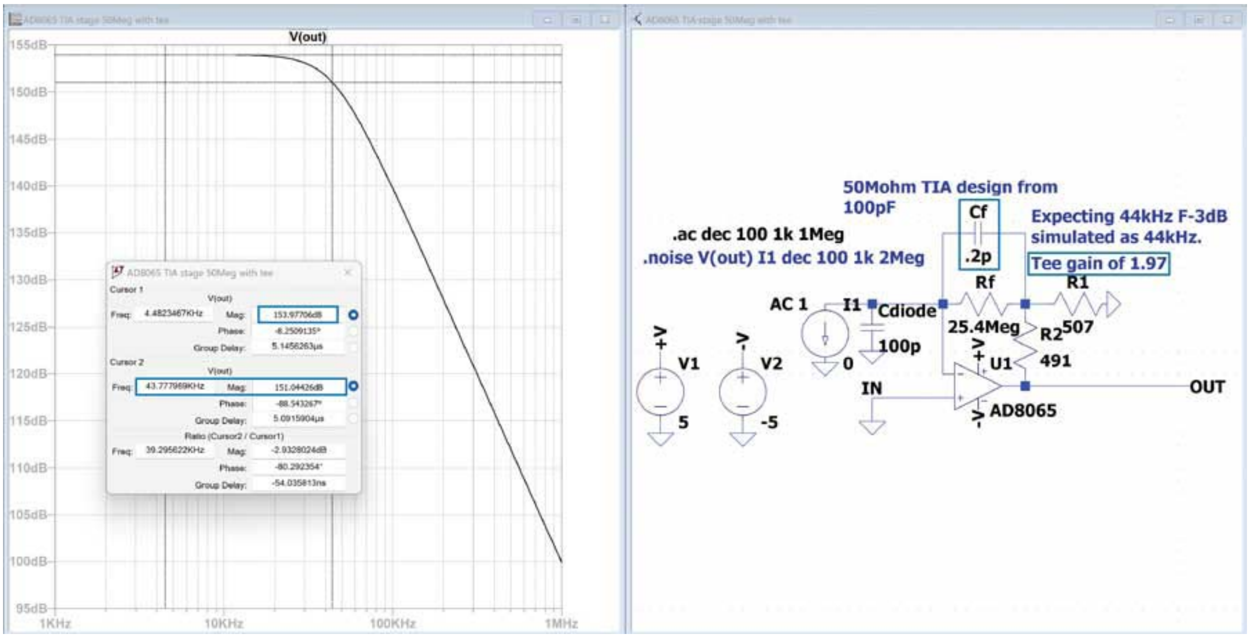
To illustrate how useful this tee network technique might be, implement a 50-MΩ design from a 100-pF detector using the unity-gain stable AD8065 JFET input FastFET device. The design equations shown here apply equally as well to this unity-gain stable, 67-MHz GBP, very low input bias-current device.

For very high TIA gains, JFET or CMOS inputs are preferred to remove the output DC offset due to the input bias current through that feedback resistor. The simple design required a 0.1-pF C_f, too low for implementation. Targeting a 0.2-pF parasitic in the R_f resistor requires the tee design of *Figure 5*, where the R_f element has been reduced from 50 MΩ to 25.4 MΩ, and relatively low-valued R1 and R2 elements provide 1.97 A_t gain. The expected F_{-3dB} in a Butterworth response was verified in this test simulation at the expected 44 kHz.

Note that there's no matching resistor on the V+ input to ground, as this JFET input device doesn't have matching input bias currents. The maximum 6-pA input bias current



4. A 2-MHz, 0- to 100-µA input square wave through a 20-kΩ TIA gain using a tee network.



AD8065 TIA stage 50Meg with tee

Cursor 1

V(out)

Freq: 4.4823467KHz Mag: 153.97706dB

Phase: -8.2509135°

Group Delay: 5.1456263µs

Cursor 2

V(out)

Freq: 43.777969KHz Mag: 151.04426dB

Phase: -88.543267°

Group Delay: 5.0915904µs

Ratio (Cursor2 / Cursor1)

Freq: 39.295622KHz Mag: -2.9328024dB

Phase: -80.292354°

Group Delay: -54.035813ns

4. A 2-MHz, 0- to 100-µA input square wave through a 20-kΩ TIA gain using a tee network.

(25°C) adds only 6 pA × 50 MΩ = 0.3 mV to the output offset error. The 25°C max input offset voltage of 1.5 mV now adds 1.97 × 1.5 mV = 2.96 mV output offset error.

Simulating the total output integrated noise through 30 kHz for the simple design shows 732 µV RMS (input-referred 14.7 pA RMS), where the tee design increases to 743 µV RMS. This is only a very slight increase since, in this design, the dominant noise term is the peaking NG × the 7-nV input voltage noise for the AD8065, which adds terms that don't really change going to the tee design.

Conclusion

When a TIA design asks for a possibly unrealizable low C_f value in the simple TIA design flow, using a resistive tee network is one simple option to raise the required C_f. Furthermore, it provides the same gain and SSBW at the possible cost of a small increase in output integrated noise.

This simple approach can also be used more generally to move the required C_f exactly onto standard C values for easier implementation. Be sure to account for the typical 0.20-pF parasitic on resistors. The tee network will reduce the input common-mode voltage shift, too, due to a bias-current cancellation resistor on the V+ input used for bipolar input op-amp solutions. Be sure to add a noise band-limiting cap for the resistor into the V+ input if that bias-current balancing resistor is used.

Starting in 1985 with the original current feedback company (Comlinear Corp.), Michael Steffes meandered through 40 years of high-speed amplifier developments across six different companies, defining and introducing over 140 high-speed amplifier products. En route, through constant applications support, new product launches, and customer interactions, he has published over 150 articles and application notes — all in the high-speed signal path area.