

Achieving Megawatt-Scale AI with SiC JFET Technology

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The rapid evolution of artificial intelligence (AI) is revolutionizing the architecture and demands of modern data centers. With the proliferation of generative AI (GenAI) models such as ChatGPT, Llama, Gemini, and DeepSeek, data centers are under pressure to deliver unprecedented computational power, energy efficiency, and thermal management. These demands are driving a shift toward high-voltage, high-density power architectures, where silicon-carbide (SiC) technology is emerging as a key enabler.

As AI data centers scale to meet these requirements, the need for efficient, reliable, and cost-effective power delivery becomes increasingly critical. SiC cascode JFETs (CJFETs) are engineered to enhance power-conversion efficiency in server power supply units (PSUs), while normally-on SiC JFETs and SiC combo JFETs provide robust protection for high-voltage hot-swaps and eFuse/ORing applications.

This article explores the latest market trends and system requirements of AI data centers, along with how to leverage the technical advantages of SiC JFET families in enabling efficient, reliable, and scalable AI data center infrastructure.

AI Data Center Market Trends and System Purpose

AI data centers are specialized facilities designed to support the intensive computational demands of AI workloads. These centers host thousands of servers equipped with GPUs, AI-specific ASICs, and high-speed networking components.

The International Energy Agency (IEA) estimates that data centers consumed about 415 terawatt-hours (TWh) of electricity in 2024, accounting for around 1.5% of global electricity use. The consumption is expected to more than double to around 945 TWh, increasing to about 3% share by 2030.

As AI models grow in complexity and size, the power requirements of these systems have surged. Current server rack power levels range from 30 to 120 kW. However, leading computing companies are actively developing technologies to push this threshold to 1 MW, which is 10X the present capacity, driving the need for significant innovations in power conversion and distribution. Traditional 48- to 54-V rack-level power distribution can no longer meet the needs of today's megawatt-scale AI infrastructure.

Most AI racks still rely on 48 V DC delivered via heavy copper busbars from power shelves to compute trays. But, once rack power surpasses 200 kW, 48-V DC distribution encounters critical limitations. It consumes excessive space — up to 64U per rack for power shelves in systems like NVIDIA's GB200/GB300 NVL72 — leaving no room for computing hardware.

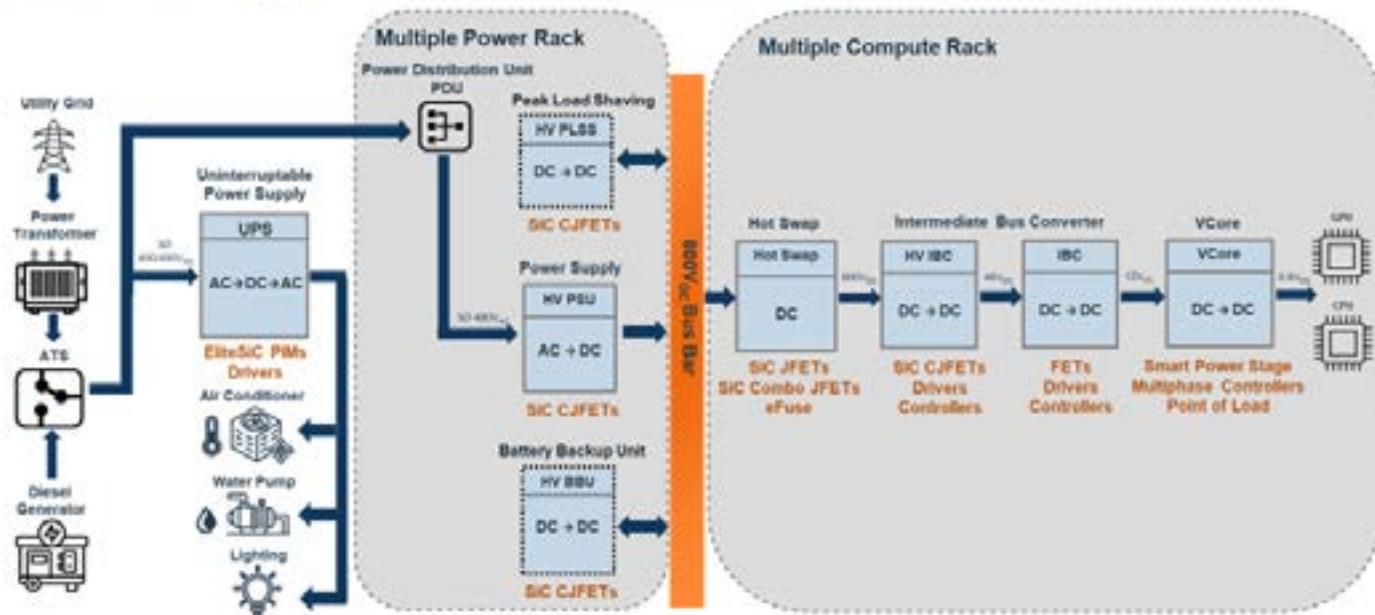
It also demands unsustainable amounts of copper, with a 1-MW rack requiring over 200 kg, scaling to 500,000 tons for a 1-GW data center (*Fig. 1*). On top of that, repeated AC-DC and DC-DC conversions introduce significant energy losses and increase system complexity.

A more efficient alternative is to convert 13.8 kV AC directly to 800-V high-voltage DC (HVDC) at the data center edge by introducing a solid-state transformer (SST). This reduces conversion stages, minimizes energy loss, and simplifies the power chain. Meanwhile, fewer PSUs and fans also improve reliability, reduce thermal load, and enhance energy efficiency, making HVDC a scalable, high-performance solution for next-generation data centers.

The key market trends in data center innovations include:

- High-voltage DC bus (400 and 800 V DC) to support dense server racks.
- Increased power density to minimize footprint and

Power Delivery from Grid to Processor in AI Data Center



1. The (\pm)400/800-V DC bus system architecture (up to 1 MW).

cooling costs.

- Fast switching and low conduction loss for energy efficiency.
- Robust protection mechanisms to safeguard sensitive components during power events.

Server PSU Requirements in AI Data Centers

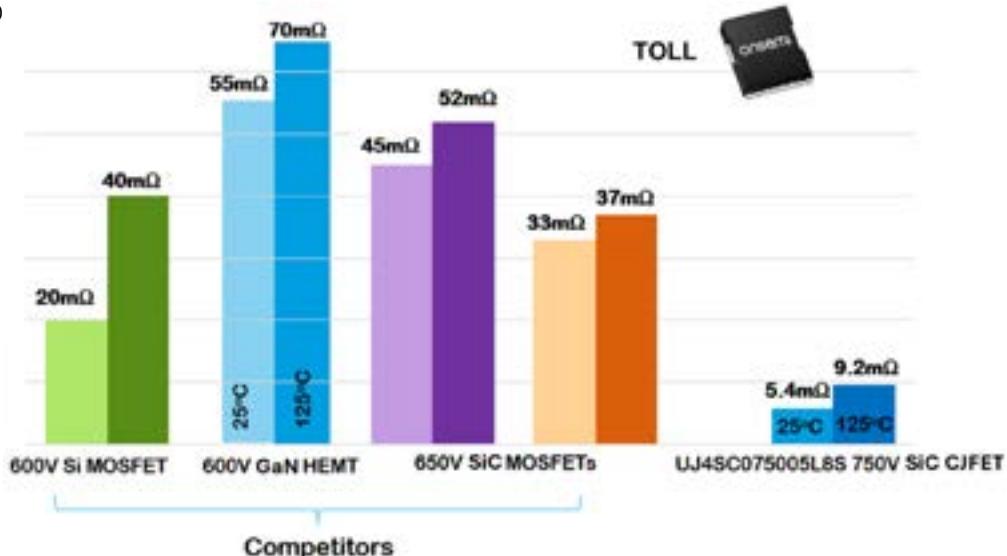
AI data centers utilize advanced server racks designed to support high-density computing, enhanced cooling solutions, and efficient power management. They often use high-density configurations (e.g., the power-supply unit, PSU, should meet or exceed the 80 Plus Titanium or even

Ruby certification), with each rack potentially supporting up to 100 kW or more. The total number of racks can range from a few dozen in smaller setups to several hundreds in larger facilities.

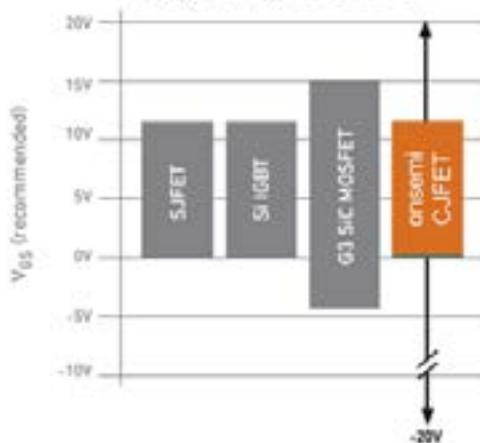
Open Rack V3 (ORV3) is the latest version of the Open Rack standard developed by the Open Compute Project (OCP). Server PSUs in AI data centers must meet stringent requirements:

- High efficiency across wide load ranges
- High power density to reduce system costs
- Compact form factors for space-constrained environments

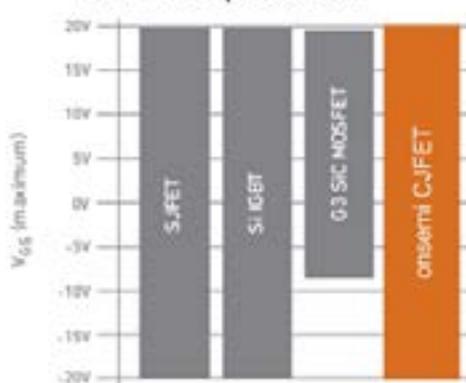
2. Comparing $R_{DS(on)}$ and area.



12V/0V Operation simplifies upgrading to CJFET



Superior gate and ESD protection



3. Comparing gate-drive voltages between power device technologies.

- Compatibility with standard gate drivers to simplify design

Traditional solutions using Si superjunction (SJ) MOSFETs often fall short in meeting these demands due to limitations in switching speed, on-state resistance, and thermal performance.

Optimizing Power Efficiency for Server PSUs: SiC Cascode JFETs

SiC cascode JFETs (CJFETs) integrate a normally-on SiC JFET with a low-voltage Si MOSFET to create a normally-off device. This cascode configuration offers several advantages:

- Lowest on-resistance ($R_{DS(on)}$) per unit area: Enables higher current handling and reduced conduction losses (*Fig. 2*)
- Fast switching speeds: Improves efficiency in both hard- and soft-switching topologies
- Gate-driver compatibility: Works with standard silicon gate drivers, simplifying integration (*Fig. 3*)
- Smaller die size: Reduces cost and improves switching loss and conduction loss

In AI server racks, SiC CJFETs enable high-efficiency AC-DC and DC-DC conversion across key power subsystems, including the PSU, battery backup unit (BBU), peak load shaving shelf (PLSS), and intermediate bus converters (IBCs). Their high efficiency and compact footprint support the demanding power profiles of AI workloads.

Comparing SiC CJFETs to SiC MOSFETs and Si SJ MOSFETs reveals the following:

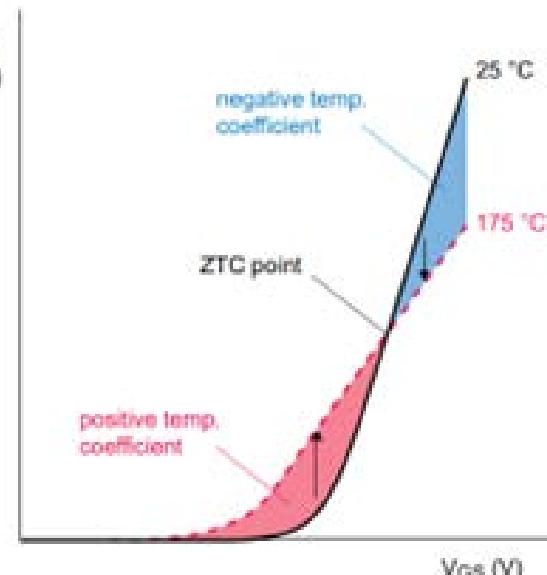
- SiC CJFETs offer significantly lower on-resistance per unit area, delivering 10X improvement over Si SJ devices and up to 50% improvement over SiC MOSFETs.
- Switching losses are drastically reduced, enabling higher frequency operation and smaller passive components.
- Thermal management is simplified, mitigating the need

for bulky heatsinks.

These benefits of SiC CJFETs translate into lower system costs, higher efficiency, and reliability for hyperscale data centers.

Hot-Swap Function in AI Data Centers

In AI data centers, hot-swap circuits play a pivotal role in ensuring seamless power-module insertion and removal without interrupting the system's operation. These functions are engineered to prevent high inrush currents during module engagement, deliver rapid fault response to safeguard sensitive electronics, and maintain compact, thermally optimized designs suitable for densely packed server environments.



4. The SiC JFET has a very small thermal instability zone in linear mode.

This combination of robustness and efficiency is essential for maintaining reliability and uptime in high-performance computing infrastructures.

SiC JFETs and Combo JFETs: Enabling Robust HV Hot-Swap Solutions

For example, [onsemi's](#) 650- to 1700-V SiC JFETs and SiC combo JFETs integrate advanced features that suit them for high-voltage hot-swap and eFuse applications. Their very low on-resistance ensures efficient power delivery with minimal thermal losses during conduction status. Furthermore, their thermal stability in linear-mode operation provides safe current-limiting function. And controllable turn-off speed offers robust protection against inrush currents and short-circuit conditions, contributing to enhanced system reliability and operational safety.

Key features of the SiC JFET include:

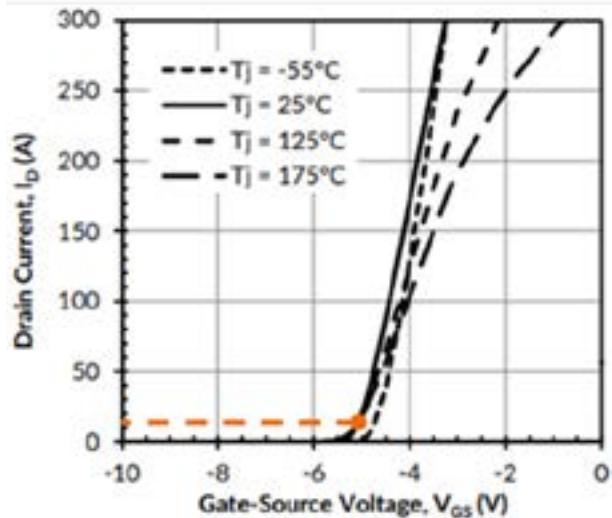
- Normally-on devices with ultra-low $R_{DS(on)}$
- Overdrive with gate-source voltage (V_{GS}) = 2-V $R_{DS(on)}$ is 10%-15% lower than $R_{DS(on)}$ with $V_{GS} = 0$ V
- Wide SOA and thermal stability zone in linear mode for current-limiting applications
- V_{GS} in the on-state is a direct measurement of junction temperature (T_j), ideal for self-monitoring circuits
- Provide fast response and high thermal conductivity

Additional key features of the SiC combo JFET include:

- Integrate a SiC JFET and a Si MOSFET in a single package
- Deliver a normally-off switch compatible with gate drive for Si/SiC MOSFETs
- Enable switching speed control through adjusting JFET gate resistance
- Enable paralleling of multiple JFETs
- Superior linear-mode thermal stability in hot-swap

In hot-swap circuits, power devices often operate in linear mode to control inrush current and ensure a smooth, safe startup under high capacitive loads. The adoption of

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5. The gate-source voltage (V_{GS}) of a JFET in the on-state serves as a direct indicator of junction temperature.

400- and 800-V HVDC busbar architectures in AI data center systems has significantly elevated the importance of SiC-based hot-swap solutions. In these high-voltage environments, SiC combo JFETs and SiC JFETs enhance system safety and operational efficiency by delivering the following critical functions:

- Prevent inrush currents during module insertion
- Protect against short circuits and overcurrent events
- Enable compact, efficient designs with fewer components

Unlike conventional Si or SiC MOSFETs, SiC JFETs exhibit a much wider thermal stability zone above the zero temperature coefficient (ZTC) point with negative temperature coefficient of current (Fig. 4). As a result, they can

COMPARATIVE ANALYSIS OF DIFFERENT DISCRETE TECHNOLOGIES

Feature	SiC CJFET	SiC MOSFET	Si SJ MOSFET
$R_{DS(on)} \times \text{Area (Rsp)}$	Lowest	Moderate	High
Switching speed	Fastest	Moderate	Slow
Thermal performance	Excellent	Good	Moderate
Cost efficiency	High	Moderate	Low

conduct more current at elevated junction temperatures without entering thermal runaway. This behavior ensures predictable performance and enhances system reliability under demanding thermal conditions.

In addition, the gate-source voltage (V_{GS}) of a JFET in the on-state serves as a direct indicator of junction temperature, enabling real-time thermal monitoring and protection as a temperature sensor (Fig. 5). SiC combo JFETs further integrate a low-voltage Si MOSFET with a normally-on SiC JFET in a compact package, combining thermal robustness with simplified gate drive (normally-off) and control flexibility.

Given these advantages, SiC combo JFETs and SiC JFETs are particularly well-suited for linear-mode applications such as hot-swap, eFuse, and ORing, where inrush current limiting, overcurrent protection, and thermal management are critical to system reliability.

As AI data centers continue to evolve, the need for high-performance, energy-efficient power solutions is rapidly growing. Devices such as onsemi's EliteSiC portfolio of 650V–1700V SiC CJFETs, SiC JFETs, and SiC combo JFETs offer solutions for server PSUs and hot-swap/ORing applications in AI data centers. These devices combine superior efficiency, thermal performance, and design flexibility, enabling data centers to meet the cutting-edge AI workloads.

By harnessing the unique properties of SiC technology, with a fully integrated end-to-end SiC supply chain, designers can build scalable, reliable, and cost-effective power architectures that support the future of AI.