Electronic Design

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Multiprotocol Wireless SoCs Untangle the IoT (Part 1)

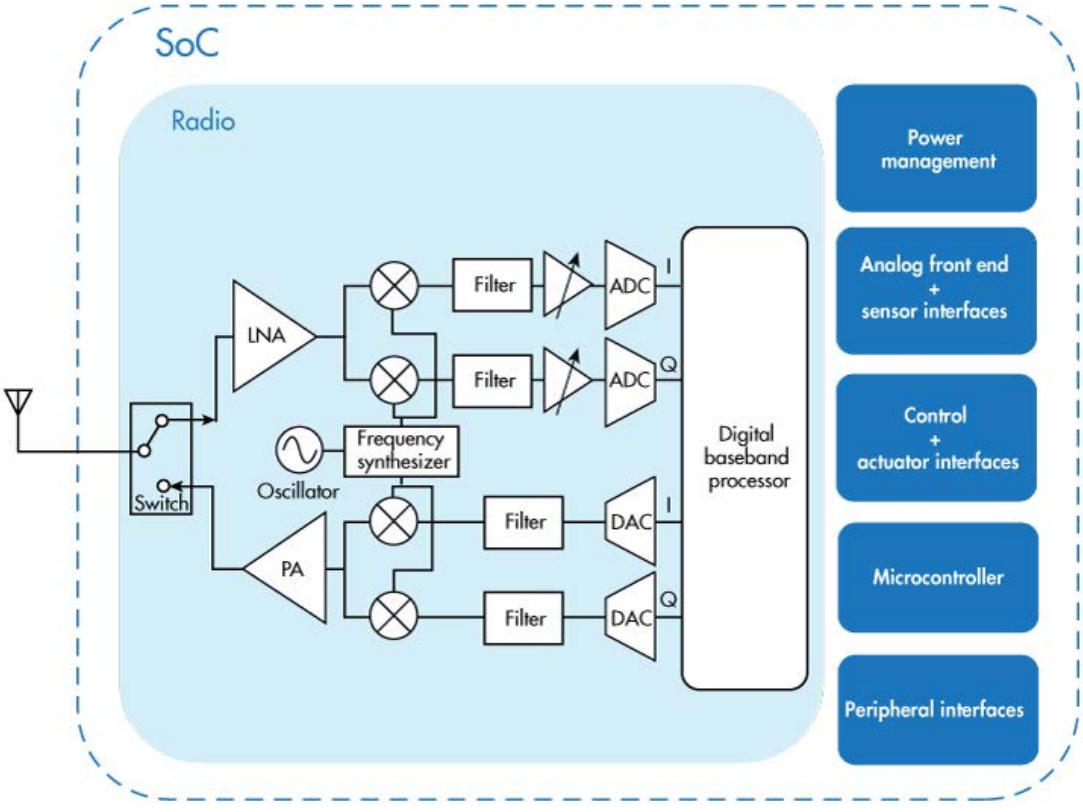
The latest multiprotocol wireless SoCs aim to connect unconnected "things" with a single chip. This roundup spotlights some of the latest solutions for short-range wireless connectivity.

The IoT is running into a wall of wireless complexity. In most cases, IoT devices rely on a wide range of wireless protocols, each serving a distinct purpose. Wi-Fi is used for local wireless networking; Bluetooth handles short-range, low-latency communication between devices; and Thread and other 802.11.4 protocols support mesh networking.

As a result, RF design is becoming increasingly complex. Integrating new functions or keeping up with new standards typically requires several chips or frequent hardware rework.

To untangle the complexity, companies are racing to roll out multiprotocol wireless SoCs that solve some of the biggest technical challenges in the IoT. These chips concurrently manage several protocols, replacing system- and module-level radio integration with a single chip.

By fusing processors, accelerators, power management, hardware security, sensor interfaces, and peripherals, such SoCs reduce design overhead and speed up time-to-market.



This is a typical block diagram for a generic wireless IoT SoC. Image credit: Adesto Technologies.

They can also help ensure compatibility between different IoT ecosystems.

By integrating everything — down to the radio's power amplifier (PA) and the other RF building blocks — into one chip, these chips can reduce the risk and cost required to integrate wireless connectivity into designs. They're also emerging as enablers of the Matter standard, which is gaining ground as a universal way for smart homes to communicate. Matter can bind together devices using different protocols and even those made by different companies.

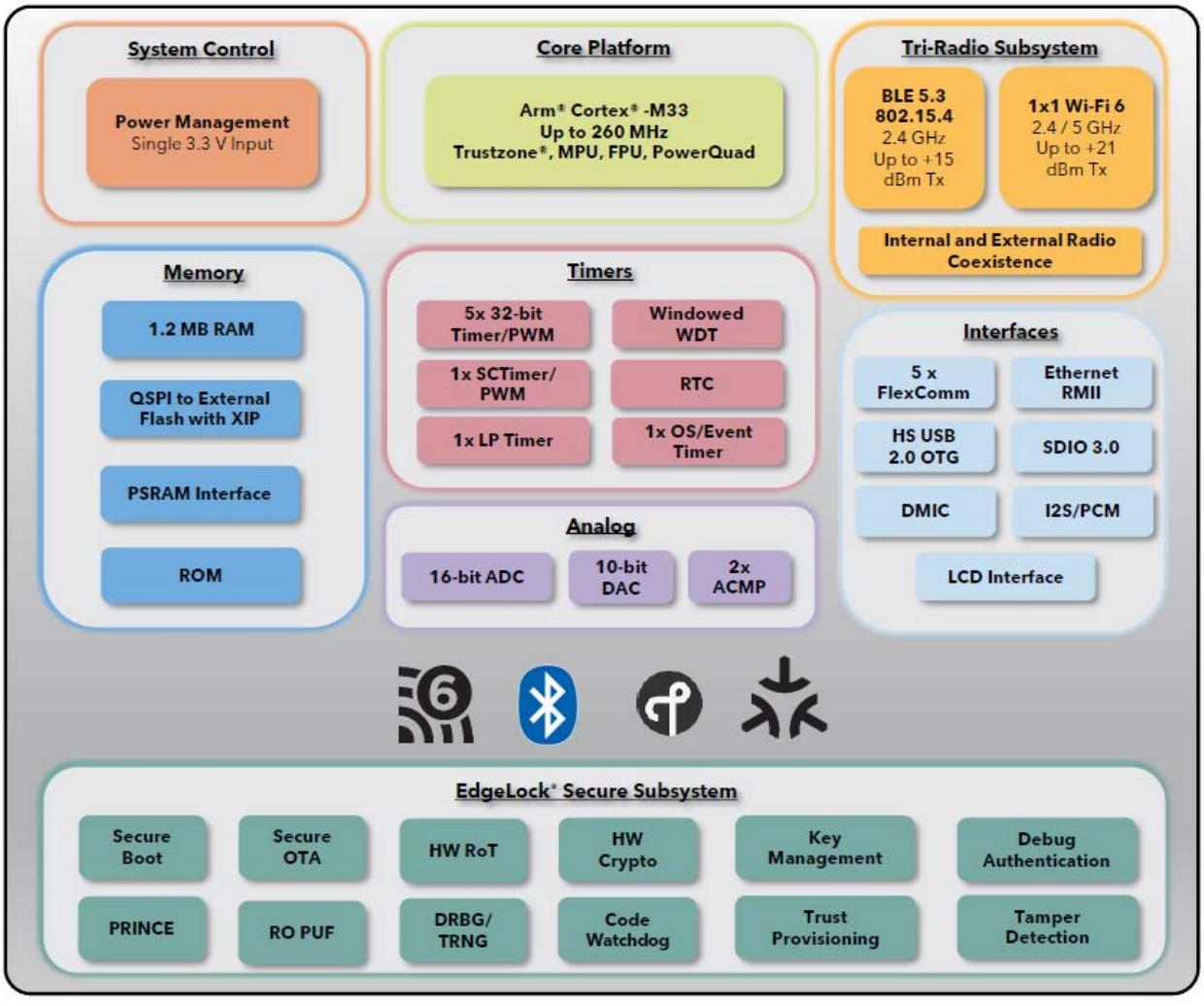
With demand for plug-and-play IoT connectivity on the rise, companies are adding more of everything, from radios to memory, to these chips, as seen in some of the latest solutions for short-range wireless connectivity.

Multi-Radio Wireless SoCs Bridge Gaps in the Smart Home

NXP is trying to bridge the gaps between IoT devices with its RW612x family of multiprotocol SoCs supporting Wi-Fi 6, Bluetooth LE 5.3, and Thread, as well as wired connectivity over Ethernet. The Matter-ready SoCs brings the performance of the company's i.MX RT series of MCUs to create a single-chip connectivity solution for applications such as thermostats, home displays, smart speakers, and home energy-management systems (HEMS).

According to NXP, the RW612x can be used in devices that act as a Matter controller, one of the core building blocks of Matter's network topology. The chip can also turn any always-on IoT device, including small-form-factor smart plugs and wall switches, into a Thread border router. These serve as switchboards for Matter devices, linking a Thread mesh network to wireless networks such as Wi-Fi that can connect further to the cloud. The Matter application layer runs on Thread and Wi-Fi network layers and uses Bluetooth LE for commissioning.

The RW612x unites all three radio technologies used by



The RW612x combines the three main radio technologies used by Matter into a single-chip solution. Image credit: NXP Semiconductors.

Matter into a single chip that can run them at the same time thanks to the company's internal and external radio coexistence technology to reduce RF interference.

The 20-MHz Wi-Fi 6 radio subsystem uses the 2.4- and 5-GHz bands to enable higher throughput, better efficiency, and longer range. The narrowband (NB) radio supports Bluetooth LE 5.3 as well as 802.14.5 wireless protocols such as Thread and Zigbee. The radios come with dedicated CPU cores and RAM to run the network stacks.

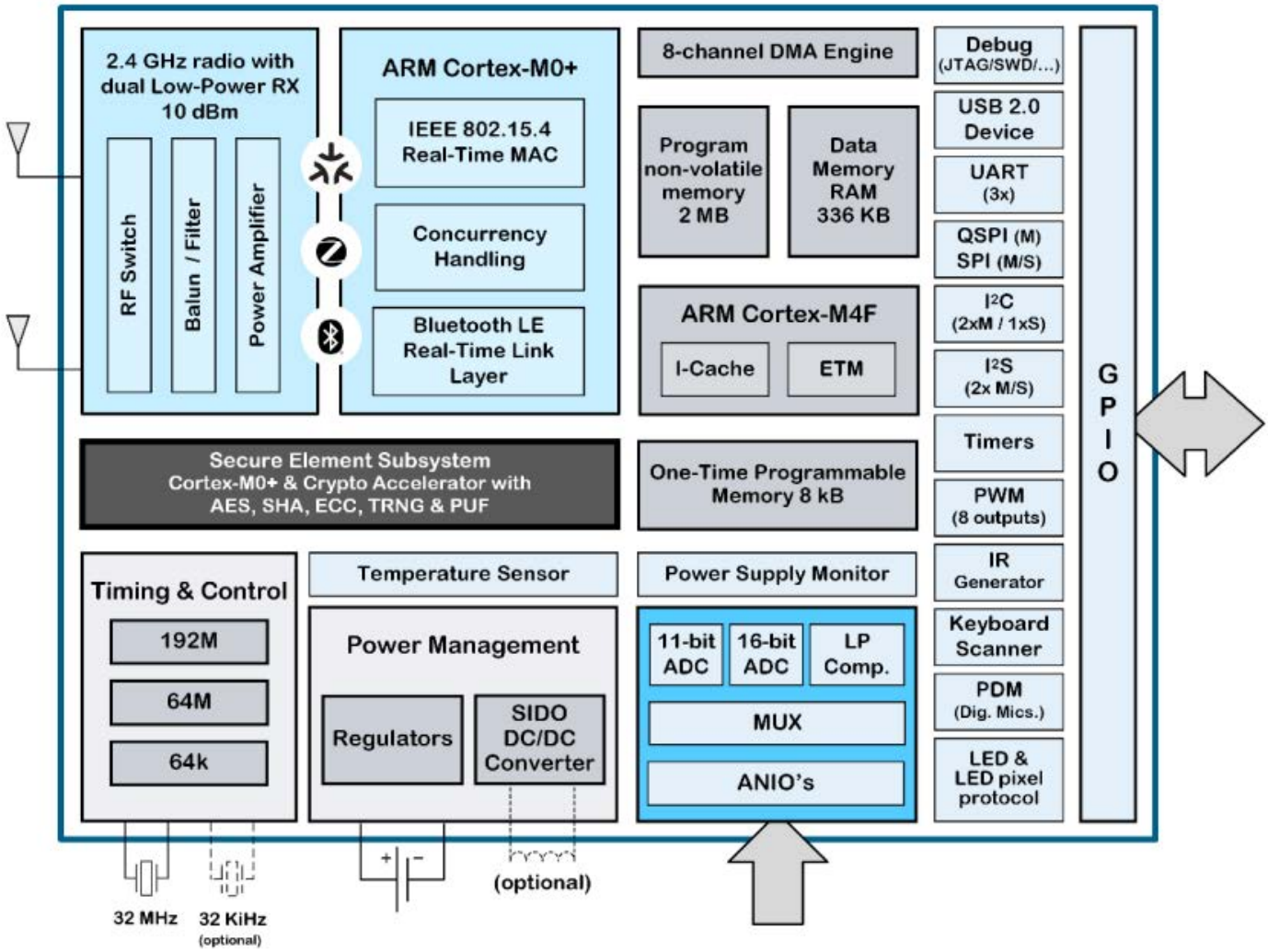
The wireless MCU features a power amplifier (PA) with up to +21 dBm of power output along with other parts of the RF front-end.

NXP said it includes all of the other building blocks for a Matter-ready wireless MCU. The Cortex-M33 CPU at the heart of it runs up to 260 MHz, and it comes with 1.2 MB of on-chip SRAM plus a quad SPI interface for securely accessing off-chip execute-in-place (XIP) flash memory.

The flash-less MCU is secured by Arm's TrustZone-M technology, but it adds a secure subsystem that acts as the hardware root of trust (RoT) for the system, runs secure boot and hardware cryptography, and supports side-channel protection and secure OTA.

NXP explained that it can run on a single 3.3-V power supply, with the integrated buck regulators and LDOs supplying internal power domains. It integrates a wide range of advanced analog peripherals, including a display driver.

While the RW61x is all about multi-radio connectivity, NXP introduced the MCX W71x as a single-chip wireless solution for IoT end nodes such as temperature sensors, smart plugs, and door locks. Powered by a 96-MHz Cortex-M33, the MCU leverages a low-power architecture and energy-efficient radio to support secure connectivity over Matter, Thread, Zigbee, and Bluetooth LE, while maximizing battery life. The upgradable radio subsystem enables new wireless protocols to be added to IoT devices for years to come.



The QPG6200L uses the same three-core CPU architecture as many other multiprotocol IoT SoCs. Image credit: Qorvo.

Multiprotocol wireless SoCs play a central role in the adoption of the Matter smart-home standard. Image credit: NXP Semiconductors.

Wireless SoCs Enables Concurrent Connectivity in Smart Homes

Most IoT devices implement a wide range of wireless protocols to connect to other devices in smart homes, with each serving a distinct function. But coordinating them all to maximize performance and minimize latency can be complicated in increasingly dense IoT networks. Qorvo tries to address the challenge with its Concurrent Connect technology, which sits at the heart of its family of smart communications controllers called QPG600.

The first chip in the family, the QPG6200L, is based on the same three-core CPU architecture as many other multiprotocol IoT SoCs — one for the wireless connectivity, one for the security subsystem, and the other for customer applications. The multiprotocol 2.4-GHz radio supports Bluetooth LE along with Thread and other IoT mesh-networking protocols, and it comes with separate receive paths for concurrent listening. The Cortex-M4 CPU core can execute code from 2 MB of non-volatile memory (NVM) or 0.3 MB of RAM at clock speeds of up to 192 MHz.

In most cases, multiprotocol IoT devices use time-division multiplexing (TDM) to send several signals over the same channel by dividing it into different time slots. Most wireless SoCs utilize dynamic multi-protocol (DMP) technology to switch back and forth between protocols such as Bluetooth and Thread because only one can communicate over the channel at a time. While this works for a small number of IoT devices, more complex networks can pose issues as IoT devices competing for a communication time may disrupt network activity.

In addition to obvious inefficiencies, switching between different protocols has other tradeoffs, increasing latency and ultimately resulting in data packet losses, as only one standard is communicated while the other is blocked.

Qorvo leverages ConcurrentConnect to continuously listen to and receive packets from different protocols at the same time — whether Zigbee and Thread, or Zigbee and Bluetooth LE to a smartphone, or Thread and Bluetooth LE mesh. The "concurrent listening" enables more intelligent close-to-instantaneous switching from Bluetooth LE to Zigbee or Thread with minimal latency. By integrating Concurrent Connect directly into the silicon, the company said that the chip can change protocols in a faster, more robust way to reduce data packet losses.

The QPG6200L can be connected to Bluetooth mesh and Thread networks at the same time, or a Bluetooth-based smartphone could be connected directly to the device while operating in a Zigbee or Thread network.

Qorvo said it delivers transmit power of up to 10 dBm with antenna diversity, which maximizes the reliable range of the device by using a pair of antennas instead of one. The SoC monitors the situation and makes sure the best antenna is used for Bluetooth and Thread at any time. This minimizes the impacts of signal degradation in dense IoT deployments.

According to the company, antenna diversity increases link budget by 8 dB, resulting in 70% more range compared to similar systems with only one antenna. This also reduces re-transmissions.

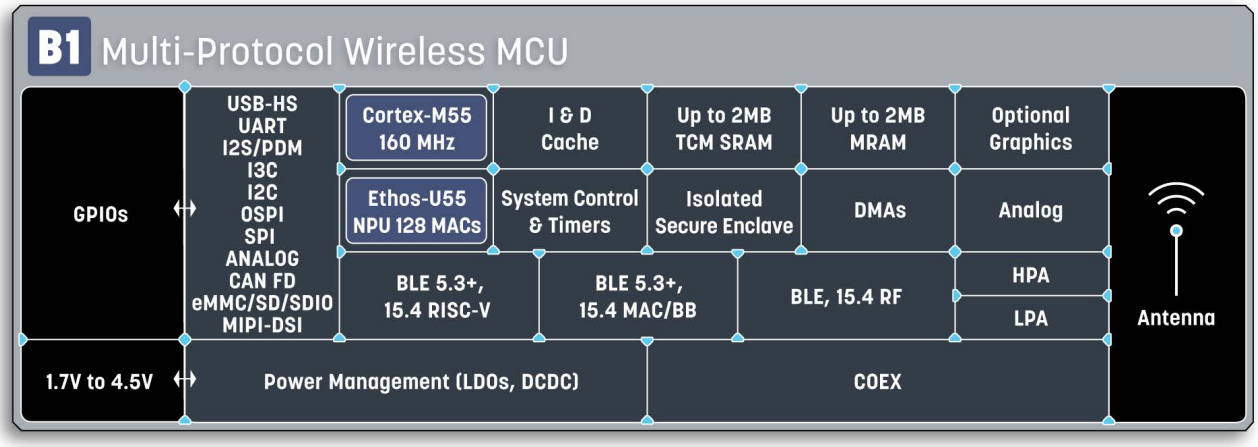
The power-management unit (PMU) gives it the ability to run on a standard coin-cell battery.

Three-in-One RF SoC Pushes into Compact IoT Devices

Synaptics brings multiprotocol wireless connectivity to battery-powered IoT devices such as wearables, smart watches, smart speakers, and home appliances with its SYN461x. While it requires a co-processor to run applications, the company said the RF SoC acts as the main controller for wireless connectivity, offloading the protocols from the host to save power.

The three-in-one RF SoC integrates Wi-Fi 6E, Bluetooth 6.0, Bluetooth LE, and 802.15.4 wireless protocols such as Thread and Zigbee in a single chip optimized for power savings.

The Matter-ready chip supports up to tri-band 1×1 Wi-Fi using the 2.4-, 5-, and 6-GHz bands. On top of standard Bluetooth 6.0, it comes with the latest capabilities in Bluetooth LE, including channel sounding for location and Auracast for wireless audio.



To save power, the Balletto dynamically powers only the logic and memory in use at any given time. Image credit: Alif Semiconductor.

The wireless SoC integrates the PHY and MAC for the Wi-Fi radio and a separate PHY and MAC for the other radio, which is used for Bluetooth and Thread/Zigbee. It features a pair of Cortex-M4 MCUs to control all of the wireless connectivity — one for the Wi-Fi stack, and the other for the Bluetooth and Thread/Zigbee stacks. Also included are a fully integrated RF front end with the power amplifier (PA), low-noise amplifier (LNA), and Tx/Rx switch, saving space and system costs by eliminating external components of the RF front-end (RFFE).

One technical challenge posed by wireless IoT protocols is that they operate in overlapping frequency bands. Wi-Fi and Bluetooth use the same 2.4-GHz band as Thread, Zigbee, and other IoT protocols, which can cause congestion, crosstalk, and other forms of interference that may block or delay the transmission and reception of RF signals. A multitude of wireless SoCs, including the SYN461x, are specifically designed at a hardware and software level to reduce interference between wireless protocols and make sure everything can coexist.

In many cases, wireless SoCs enable the radios to communicate in real-time, sharing transmission priorities to prevent any overlaps. Precise timing ensures tight synchronization of the radios, using microsecond-level time slots to avoid interference. The Wi-Fi radio can also shift into the 5- and 6-GHz bands to avoid any interference in the 2.4-GHz band, while timing protocols such as adaptive frequency hopping (AFH) in Bluetooth further reduce congestion by dynamically steering into less crowded channels.

By applying intelligent scheduling and isolation to manage traffic between radios, Synaptics said it can ensure reliable and efficient multiprotocol connections. The SYN461x also is able to coordinate its operation with external LTE and GNSS radios.

The entire Veros family is designed to be tightly integrated with Synaptics' Astra series of AI processors, and the company's Machina development kit acts as the link between the Astra platform and Veros SoCs.

Multiprotocol Wireless MCU Brings NPU to the Very Edge

Other chips come with a neural processing unit (NPU) to deliver fast, power-efficient AI execution. One of the latest is Alif Semiconductor's Balletto family of multiprotocol wireless MCUs targeting space-constrained IoT devices.

The Balletto chips bring more performance to machine learning and sensor fusion thanks to their hardware accelerators and large on-die memory. The Cortex-M55 CPU at the heart of it comes with Arm's Helium DSP technology, running at up to 160 MHz, and it's paired with Arm's Ethos-U55 that brings AI acceleration to the table. The chips are supplemented by up to 2 MB of SRAM configured as tightly coupled memory (TCM), up to 2 MB of MRAM serving as NVM, and an octal SPI interface to attach additional flash.

The Balletto chips also contain a Cortex-M0+ to secure the system and a RISC-V CPU to run the networking stack, enabling robust connectivity without requiring a separate MCU. With its dedicated processor and memory, Balletto's radio supports concurrent Bluetooth LE 5.3 and 802.15.4.2011 protocols such as Thread and Zigbee using a single on-chip antenna.

In addition, the startup said Balletto can be used in smart-home devices that support the Matter standard, plus it supports Bluetooth LE Audio and Auracast broadcast audio.

While the chip comes with a receiver sensitivity of –101 dBm, Balletto features a dual power-amplifier architecture: a high-power amplifier provides 10-dBm output for maximum range and signal strength, while a low-power amplifier outputs 4 dBm for optimized power.

Power efficiency may be hard to maintain when mul-

tiple radios are active. Every wireless protocol has different power requirements, and IoT devices that dynamically shift between different protocols or use several at the same time can rapidly deplete the battery.

To save power at the system level, Balletto features the startup's aiPM technology, which dynamically powers only the logic and memory in use at any given time. The PMU supports four system-level power modes, including a stop mode that draws 700 nA.

The chips incorporate many of the same sensor interfaces and peripherals present in other IoT SoCs. They feature an analog front end (AFE) with a digital-to-analog converter (DAC) and 24-bit sigma-delta analog-to-digital converter (ADC), plus camera and display interfaces supported by a graphics processor.

IP Brings Multi-Protocol Wireless Connectivity to Edge SoCs

Though multiprotocol wireless connectivity is a fundamental requirement for the latest IoT devices, integrating it into the latest SoCs is increasingly complex and costly. To remove technology barriers and speed up time-to-market for hearables, wearables, and other wireless consumer electronics, Ceva introduced its latest multi-protocol wireless IP platform, Ceva-Waves Links 200, with support for Bluetooth LE along with 802.15.4 protocols.

The IP is a drop-in solution for wireless IoT connectivity, enabling concurrent multiprotocol communication with advanced coexistence technology baked directly into the silicon. Ceva said it uses more advanced modulation along with a state-of-the-art 2.4-GHz radio designed for TSMC's 12-nm process to push the performance limits of Bluetooth in a low-power solution.

According to Ceva, the solution can run in high-data-throughput (HDT) mode that more than doubles the speed of standard Bluetooth, delivering a data rate of up to 7.5 Mb/s.

The Waves Links 200 is the latest multiprotocol wireless IP in the Ceva-Waves Links family following the Links 100, which comes with a Wi-Fi 6 1×1 40-MHz solution, a Bluetooth 5.4 dual-mode solution for Bluetooth and Bluetooth LE, and a Matter-ready wireless subsystem for Thread and Zigbee. Designed to be manufactured at 22 nm, the IP is pre-integrated with a multiprotocol radio that operates in the 2.4-GHz band used by all three wireless protocols.

Ceva said that its Waves Links 200 family offers further integration possibilities with Wi-Fi or ultrawideband (UWB). It can be further paired with the company's NeuPro-Nano family of NPUs, leveraging the 12-nm process for efficient AI acceleration.