Electronic Design

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Noise Considerations in ADC Signal Chains

This article addresses some basic noise principles and how to apply them to each analog-to-digital converter input node to minimize any noise convolving onto the output spectrum.

Many noise sources can plague high-speed radio-frequency (RF) analog signal chains, making design considerations that much more challenging. Both megahertz and sub-terahertz sampling-rate converters have analog, clock, and power inputs, which realize the converter as a multi-input "mixer" with a digital back end.

With continuously constrained converter headroom, maintaining a noise spectral density of 150 dB_{FS}/Hz is challenging with each new design. That's why it's paramount to recognize the importance of the surrounding noise contributions that may erode performance within the entire signal chain.

Indeed, there's an extensive range of noise principles—too many to even list. This article addresses some basic noise principles and how to apply them to each analog-to-digital converter (ADC) input node to minimize any noise convolving onto the output spectrum.

Defining Noise Bandwidth

Noise bandwidth isn't the same as the typical –3-dB bandwidth you may be accustomed to, such as an amplifier's bandwidth or filter cutoff point. Noise takes on a rectangular shape to specify the integration of the bandwidth. *(Without going into a lengthy derivation in noise bandwidth, see Reference 1.)* When integrating the noise in rectangular form, for a standard first-order system, the noise bandwidth will be 57% larger than the –3-dB cutoff. For example, 150 MHz of bandwidth determined by a second-order anti-aliasing filter (AAF) located between an amplifier and an ADC will result in a noise bandwidth of 183 MHz, or 1.22*150 MHz.

The *table* lists the integration noise bandwidth for multiple order systems, which a designer can use to help set final calculations in the signal chain.

System Order	Noise Bandwidth (Multiplication Factor)
1	1.57
2	1.22
3	1.15
4	1.13
5	1.11

Multiplication factor to use for resulting noise bandwidth vs. filter and system order.

Resistor Noise and Amplifier Noise Contributions

The second noise fundamental to consider is resistor noise. Think of resistors as very small heating elements that generate thermal noise. Even though their contributions to noise are small, they can add up quickly if high-value resistors are used. Resistive noise contributions add up even more quickly if high-value resistors are wrapped around an amplifier in a gain configuration.

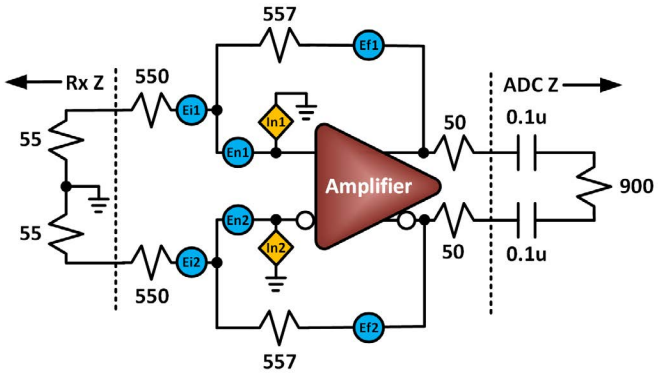
Equation 1 defines resistive noise or error as:

$$Er = \sqrt{(4kTR\Delta f)} \qquad (1)$$

where:

- k is 1.38 ´ 10^{-23}W/s/K (Boltzmann's constant)
- T is 290 Kelvin
- R is the resistance in ohms
- f is the noise bandwidth of the system in hertz

Therefore, 1 kΩ = 4 nV_{RMS}/Hz for 1-Hz bandwidth; resistor noise is equal to 4 nV/√(Hz) per 1 kΩ. The designer can use this reference ratio when calculating noise contributions with resistors that are wrapped around an amplifier to enable gain.



1. Generic amplifier noise model. (Credit: Texas Instruments)

Amplifiers are active devices, which means that they need a power supply to function properly. In most signal-chain noise analyses, the goal is to find or calculate the amplifier's referred-to-output (RTO) noise, which is the noise value required to complete the signal-chain noise analysis and how RTO noise affects the ADC's overall performance.

For example, using *Figure 1* as a generic amplifier model, if the amplifier's datasheet specifies a bandwidth of 320 MHz, that equates to a noise bandwidth of 1.57*(3-dB bandwidth), or 502.4 MHz per the previous section.

Then find the amplifier's voltage- and current-noise contributions, which are located in most amplifier datasheets. In this case:

Voltage noise or E_n = 5 nV/√(Hz)

Current noise or I_n = 2 pA/√(Hz)

The next step is to calculate the error ratios for the input (E_i) and feedback (E_f) resistive elements:

E_i = (550/1,000) ´ 4 nV = 2.2 nV/√(Hz)

E_f = (557/1,000) ´ 4 nV = 2.23 nV/√(Hz)

To round out the amplifier noise analysis, compute the input resistive voltage-noise, the amplifier's voltage-noise, and current-noise contributions based on the resistors used in *Figure 1's* noise model:

R_{INPUT} voltage noise = E_i × (1 + 557/605) = 4.23 nV/√(Hz)

Amplifier voltage noise = E_n × (1 + 557/605) = 9.6 nV/√(Hz)

Amplifier current noise = (I_n × 557 || 605**) × (1 + 557/605) = 1.11 nV/√(Hz)

**"557 || 605" denotes the total resistance of 557- and 605-Ω resistors in parallel.

Now, root sum square (RSS) these terms to compute the final RTO noise value:

Front-end noise = √((R_{INPUT} voltage noise)^2 + (Amp voltage noise)^2 + (Amp current noise)^2 + (E_f)^2) = √((4.23 nV^2 + 9.6 nV^2 + 1.11 nV^2 + 2.23 nV^2))

= 10.8 nV/√(Hz)

Total noise = √(Noise bandwidth) × front-end noise = √(502.4 MHz) × 10.8 nV = 241.7 μV_{RMS}

Note that amplifiers are different from operational amplifiers, simply because they typically include resistive elements internal to their package. Thus, the noise contribution is the overall noise given in the respective amplifier's datasheet. An amplifier with included resistors usually specifies the noise as referred-to-input (RTI) noise. Using the gain in the amplifier circuit enables conversion of the RTI number to RTO noise.

For example, if a specific amplifier in the RF signal chain has 1.3 nV/√(Hz) of RTI noise, and the designer wants to use a gain of 16 dB to translate the input signal more closely to the full scale of the ADC, see Equation 2 below:

The designer will need to know the RTO noise of the amplifier to fully calculate the RF signal-chain noise of the entire system. This number will become significant later when summarizing all of the signal-chain noises together.

References 1 and 2 offer more information about noise bandwidth, resistor noise, and amplifier calculations and considerations.

Clocking Noise Contributions

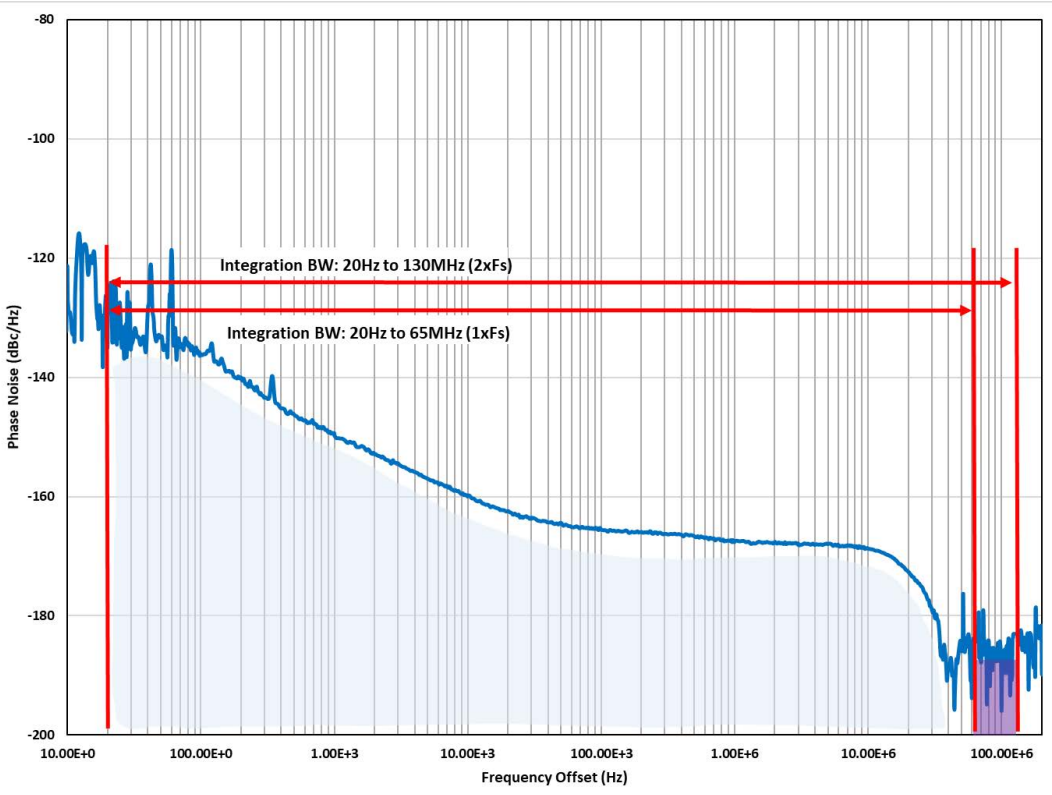
Another important noise contribution to overall signal-chain performance is clock noise or jitter. This contribution affects the performance of an ADC at its core and can quickly degrade its rated dynamic range capability if the right clocking signal chain, clock oscillator, voltage-controlled oscillator—or all three—aren't well-defined.

With just a basic understanding of how to factor in clock noise and an initial assumption that clock noise and jitter are broadband, it's possible to get a good sense of the influence that this metric may have on the total system's signal-chain performance.

To calculate jitter, set the lower integration bandwidth limit to a value close to DC to consider the entire phase-noise profile of the clock. It's recommended to use at least the ADC sampling frequency (F_s), and for even better analysis, 2 × F_s for the integration bandwidth. Many times, 2 × F_s is more appropriate to understand the broadband noise contribution and reach the sampling clock's noise floor *(Fig. 2)*.

For example, if the ADC is sampling at 65 MSPS, the integration bandwidth ranges from 20 Hz to at least 65 MHz (or up to 130 MHz for a more detailed noise consideration). Simply use the defined integration broadband jitter noise in seconds (preferably femtoseconds or below) and the analog input frequency or intermediate frequency (IF) of interest.

$$\text{RTI} = 1.3\text{nV}/\sqrt{\text{Hz}},\ \text{gain} = 16\text{dB thus, RTO} = 1.3\text{n} \times 10^{(16/20)} = 8.2\text{nV}/\sqrt{\text{Hz}} \quad (2)$$



2. ADC phase-noise integration bandwidth. (Credit: Texas Instruments)

The maximum error occurs when the clock amplitude is at its highest, assuming a sine-wave input.

Equation 3 calculates the root mean square (RMS) voltage error—that is, the sampling clock's additive noise to the RF signal chain. For example, a 30-MHz analog input IF and a clock jitter of 100 fs yields a broadband voltage noise or error of:

$$18.8\mu V \text{ or } Vn = (2\pi) \times (30MHz) \times (100fs) \quad (3)$$

References 3 and 4 offer more information about clocking considerations, and how these relate to ADC and RF signal chain performance.

Power-Supply Noise Contributions

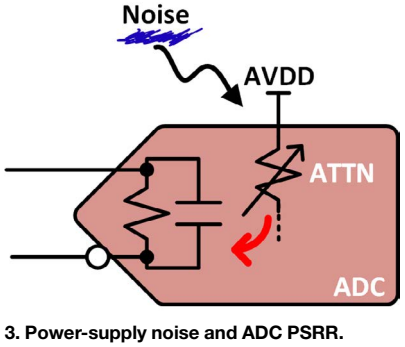
Let's explore how power-supply noise can influence RF signal-chain performance. Typically, in an analog supply domain (AV_{DD}), the analog power domains are the most sensitive to power-supply noise, so this supply type will be used as an example.

Similar to all active devices that require a power supply connected to them, all regulator types (low-dropout regulators and switchers) have some sort of noise. This noise, depending on how dominant it is, can also affect the ADC's performance, just like an amplifier's noise or anything else in the RF signal chain. Here's how.

As with clock noise, regulator noise can couple through the power-supply pins of the ADC or any active device that requires a power-supply connection. In the clock example, the internal circuitry of the clocking nodes is tied into the sample-and-hold structures internal to the analog inputs of the ADC. This makes it the perfect place for any noise or coupling through the clock pins to find its way into the internal signal path of the ADC.

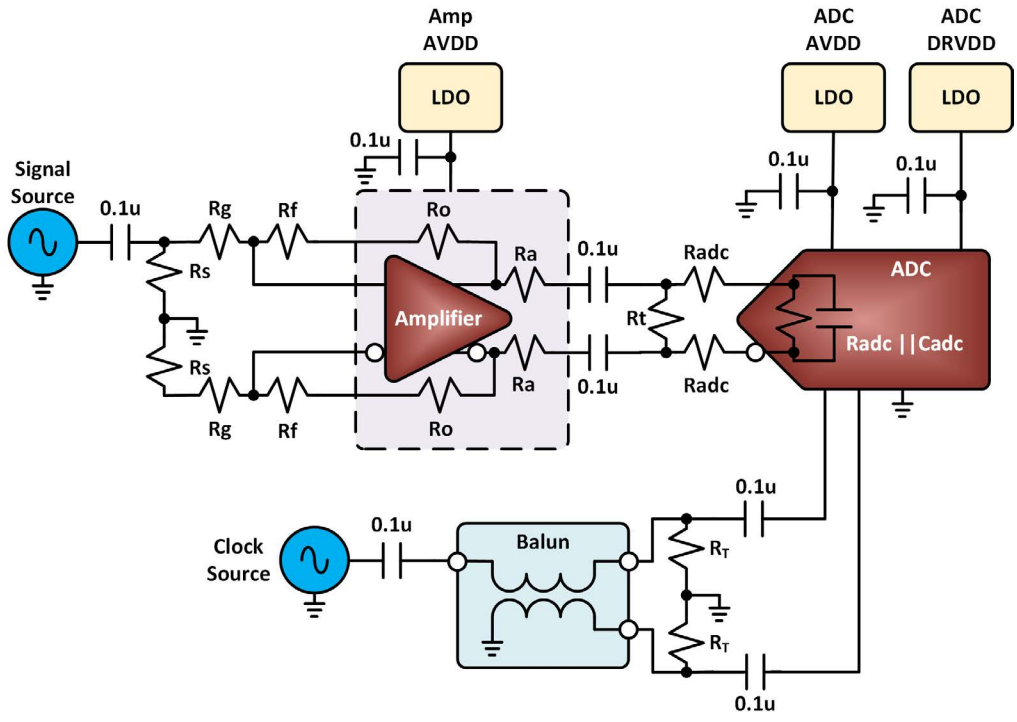
The coupling path has almost zero attenuation in this case. In the power supply's case, however, notice that the internal circuitry from the power-supply pin of the ADC includes an attenuation symbol *(Fig. 3)*.

This symbol represents the ADC's rejection of any noise or signal coupling through the power pins, which is measured as the power-supply rejection ratio (PSRR). Ultimately, this attenuation defines the amount of coupled rejection, or PSRR, from the internal circuit design inside the ADC. Some circuit design topologies allow for less noise attenuation than others; therefore, more noise can leak into the ADC's digitization path, degrading the ADC's performance.



3. Power-supply noise and ADC PSRR. (Credit: Texas Instruments)

To quantify the regulator's noise and its effect on the ADC, the designer can use the regulator's measured noise band, which is usually found in the regulator's datasheet. For example, a regulator can have 225 µV of noise over a 100-kHz bandwidth. Assuming that the noise is flat or Gaussian, the designer can use this specification to estimate how it might contribute to the overall performance of the ADC signal chain.



4. General signal-chain block diagram. (Credit: Texas Instruments)

However, the ADC's power-supply rejection (PSR) number also needs to be known. Sometimes this number is in the datasheet or is measurable on the lab bench.

In most cases, the PSR is around −40 to −60 dB over the first Nyquist in the AV_{DD}, which is typically the most sensitive converter supply. In this case, let's assume −40 dB for simplicity. The effective noise contribution is then 7.12 nV or 225 μV/√(100 kHz) × 10(−40/20).

Keep in mind that this is only for one supply domain. The designer will need to evaluate all supply domains in the same manner, and each domain may have different PSR values within the ADC, amplifier, and so on.

References 5 and 6 offer more information and insight on power-supply noise and PSR and its effects on ADCs (see References 6 and 7).

Putting All of the Noise Contributions Together

Figure 4 shows a simplified RF signal-chain block diagram noise model that builds on the preceding discussion.

The last step is to find the ADC's noise contribution in the signal chain. For example, an ADC may have an analog input full scale of 1.75 V p-p differential, while the datasheet lists the signal-to-noise ratio (SNR) as 71.7 dB_{FS}. By back-calculating noise out of the SNR equation, Equation 4 reveals the thermal noise:

EQ. 4a(below)

or

EQ. 4b(below)

Next, determine the noise contributions as previously described for the rest of the power supplies.

The AV_{DD} contribution for the ADC analog supply is 7.12 nV_{RMS}.

Do the same for the digital supply domain (DRV_{DD}) of the converter and the AV_{DD} of the amplifier. In these calculations, the PSRR of the DRV_{DD} of the converter is −80 dB and the PSRR of the amplifier's AV_{DD} is −60 dB:

Amplifier AV_{DD} = 450 μV/√(100k) × 10(−60/20) = 1.42 nV

ADC AV_{DD} = 225 μV/√(100k) × 10(−40/20) = 7.12 nV

ADC DRV_{DD} = 225 μV/√(100k) × 10(−80/20) = 71.2 pV

To find the total noise contribution of all of the power supplies, simply RSS these three noise sources, which gives a total of 7.2 $6nV_{RMS}$ or $\sqrt{(7.12\ nV^2 + 71.2\ pV^2 + 1.42\ nV^2)}$.

From the previous amplifier example, the RTO noise is 8.2 nV/√(Hz) with a gain of 16 dB.

Typically, the designer will use an AAF between the output of the amplifier and the input of the converter. Otherwise, all broadband noise from the amplifier folds back in-band. Therefore, by limiting this noise with an AAF, the assumption becomes that the bandwidth of the filter is 105 MHz (−3-dB cutoff), because the ADC is sampling at 250 MSPS and has a Nyquist band of $F_s/2$ or 125 MHz.

Generally, to capture the entire Nyquist band of interest without folding noise back in, a general estimate of 85% of the Nyquist band can be assumed. Therefore, the AAF can be designed to be somewhat smaller.

In this example, a two-pole inductor-capacitor filter (second-order system) for the AAF implementation was used, yielding a noise bandwidth of 105 MHz × 1.22 = 128.1 MHz. The noise contribution of the amplifier is thus 92.8 μV_{RMS} or

$$SNR = 20 \times \log(\text{full scale } (V_{RMS})/\text{thermal noise } (V_{RMS})) \quad (4)$$

$$71.7dB = 20 \times \log(((1.75/2)/\sqrt{(2)})/\text{thermal noise } (V_{RMS})) = \text{ADC thermal noise} = 161\mu V_{RMS}$$

8.2 nV × √(128.1 MHz).

Finally, collect all of the noise sources derived in the example signal chain using the following standard SNR equation (Equation 5) and RSS them all together:

EQ. 5a(below)

or

EQ. 5b(below)

This example identifies the total signal dynamic range in terms of the converter's SNR. By reviewing these contributions in more detail, the designer can easily see what part of the signal chain is "donating" the highest noise contribution aside from the ADC's own internal thermal noise. In this case, the amplifier's noise is the largest contributor. It helps the designer understand each individual noise source impact and offers insight into the tradeoffs one needs to make to improve overall system performance.

References 7, 8, and 9 offer more information about summarizing ADC errors and understanding these tradeoffs at the AAF and system level.

Conclusion

Understanding signal-chain noise tradeoffs and root causes of noise can lead to easier design tradeoffs upfront when designing high-speed signal chains. Knowledge of how both active and passive devices interact within a signal chain in terms of noise illuminates how to predict the total dynamic range performance outcome, in terms of SNR, of the entire signal chain. Keep these principles in mind when calculating signal-chain dynamic range tradeoffs. Otherwise, the next design may go noisy.

Rob Reeder is currently the application engineer for High-Speed Converters at Texas Instruments (TI) in Dallas. Rob's prior experience includes RF design at Raytheon Missile Systems in Tucson, Ariz., including analog receivers and signal-processing applications. He was also a system application engineer with Analog Devices in the High-Speed Converter and RF Applications Group in Greensboro, N.C., for over 20 years. He has published over 130 articles and papers on converter interfaces, converter testing, and analog signal chain design for a variety of applications. Rob received his MSEE and BSEE from Northern Illinois University in DeKalb, Illinois, in 1998 and 1996, respectively. When Rob isn't writing papers late at night or in the lab hacking up circuits in the lab, he enjoys hanging around at the gym, listening to EDM, building rustic furniture out of old pallets, and, most importantly, chilling out with his family.

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$$SNR = 20 \times \log\left((FS_{RMS})/(\sqrt{(ADC\ \mu V_{RMS}^2 + Amp\ \mu V_{RMS}^2 + LDO\ nV_{RMS}^2 + Clock\ \mu V_{RMS}^2)})\right) \quad (5)$$

$$SNR = 20 \times \log\left((1.75/2)/\sqrt{(2)}/(\sqrt{(161\mu V_{RMS}^2 + 92.8\mu V_{RMS}^2 + 7.26nV_{RMS}^2 + 18.8\mu V_{RMS}^2)})\right) = 70.4dB$$