

Use an LDO and PLD for Power-Supply Enable and Disable Functions

Discover how a low-dropout linear regulator and a programmable logic device can replace microcontrollers for enable/disable functions, reducing power consumption to just microamperes.

Many systems require enabling and disabling through control lines or when applying the input power. While a small microcontroller (MCU) can implement the enable/disable function, you still need to write, maintain, and flash code for it. Many designs using a system-on-chip (SoC) have an MCU within that chip; adding another is redundant. Moreover, the MCU in the SoC isn't low power enough to both remain always on and provide the enable controller function.

This article discusses a low-cost, low-power enable controller hardware solution that consumes only microamperes of current using a low-dropout linear regulator (LDO) plus a programmable logic device (PLD). The PLD comes pre-programmed with the logic you need to implement the decision-making function of the enable controller. *Figure 1* shows the proposed solution; its power supplies are typical for an automotive system powering an SoC.

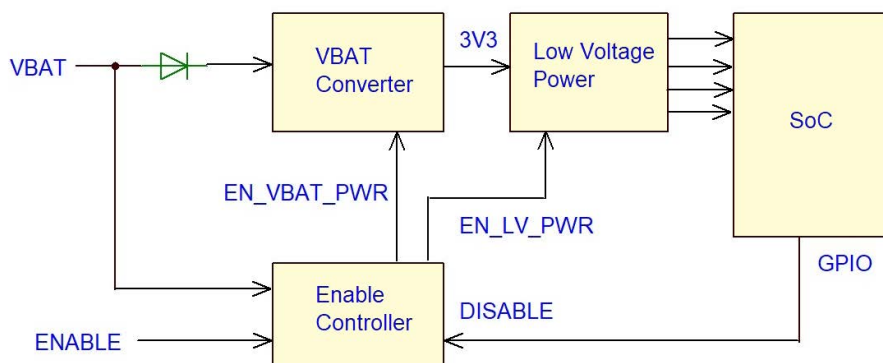
Enable Controller Solution

This solution employs the [TPS7B85-Q1](#) off-battery LDO¹ and the [TPLD801-Q1 PLD](#)² (*Fig. 2*). Features in the TPS7B85-Q1 are specifically useful in this application:

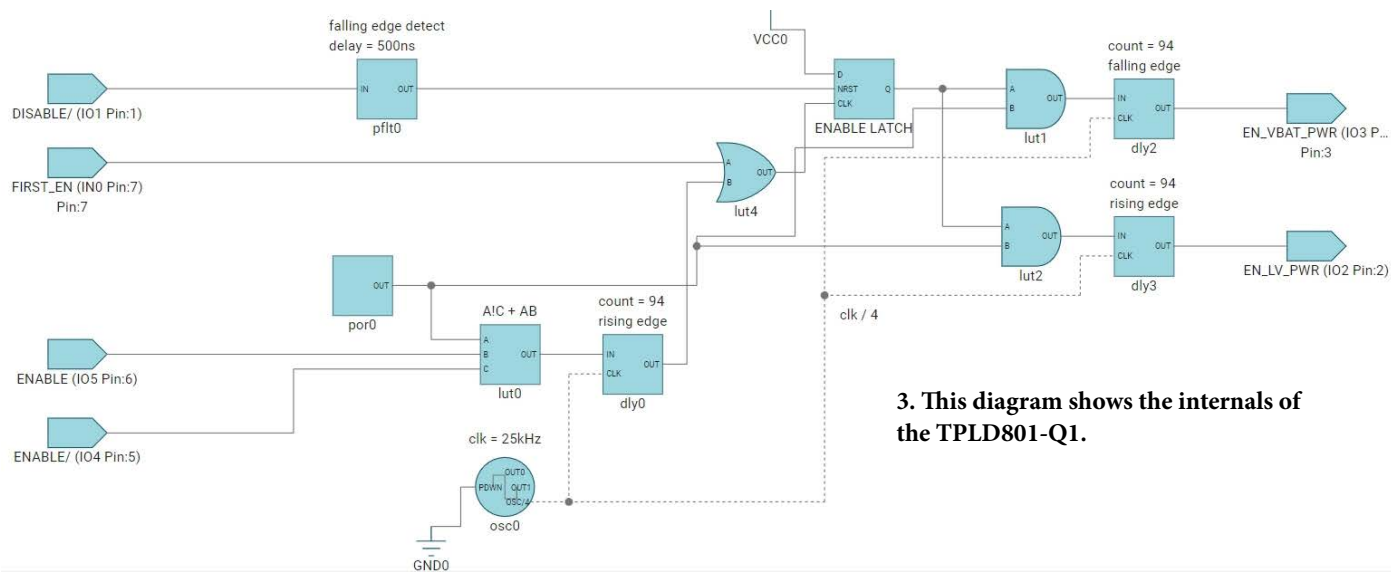
- The basic LDO function provides a fixed 3.3- or 5-V output voltage (V_{OUT}) from a battery voltage (V_{BAT}) of up to 40 V. This V_{OUT} provides power to the TPLD801-Q1.
- A power-good (PG) output with pin-programmable delay. When applying V_{BAT} , the LDO powers up. When the LDO V_{OUT} reaches regulation, PG goes high after a delay programmed by a capacitor on the DELAY pin. The TPLD801-Q1 uses the rising PG signal to detect and latch an initial application of V_{BAT} (FIRST_EN) to enable the system.
- An uncommitted SENSE comparator provides a logic high or low sense output (the SO pin) if its sense input pin (the SI pin) is above or below the 1.21-V internal voltage reference (V_{REF}), respectively. The SI pin has a maximum voltage of 40 V irrespective of whether the LDO V_{IN} is powered

or not. For blocking negative voltages, you can use diode D2. The comparator tests whether the ENABLE_IN signal's amplitude is above a certain voltage threshold. If it is, then the signal is allowed to pass to the TPLD801-Q1's enable input. This voltage threshold is adjustable through R4 and R5.

- A precision enable (EN) pin. The precision enable feature (as opposed to logic level enable) isn't documented in



1. Basic system diagram illustrating the SoC, power supplies, and the enable controller.



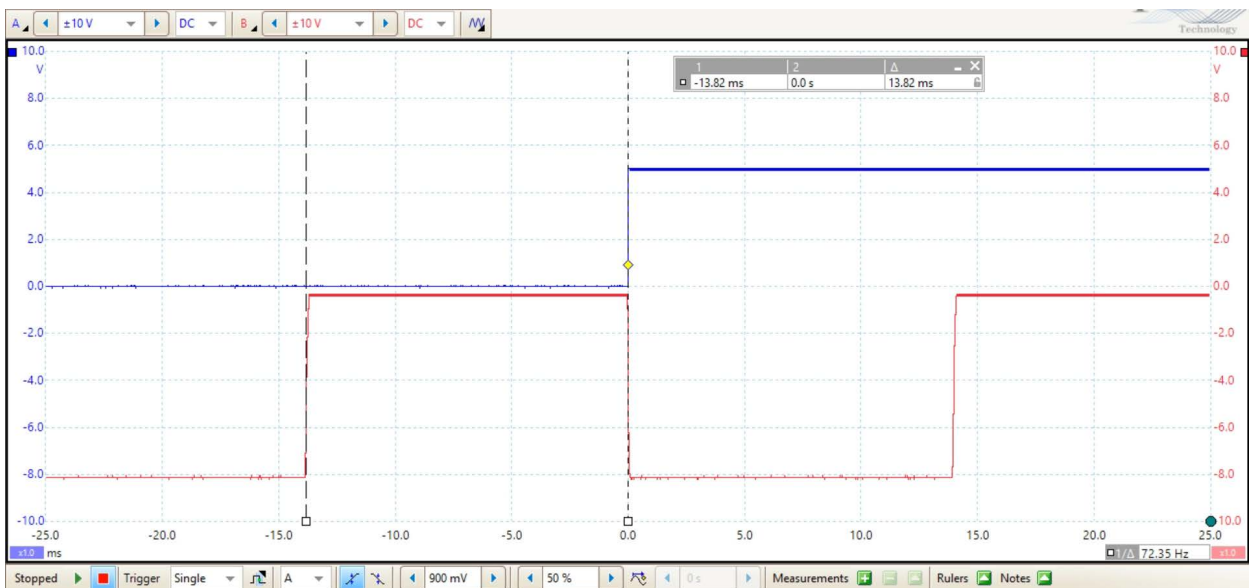
doesn't occur.

When the electronic control unit needs to power down, the SoC's MCU issues a rising edge through a general-purpose input/output. This `DISABLE` signal connects to the open-drain transistor shown in *Figure 1* and pulls down the `DISABLE/` pin of the PLD to reset the `ENABLE LATCH`. After the `ENABLE LATCH` resets, the `EN_LV_PWR` output goes low immediately; approximately 15 ms later, the `EN_VBAT_PWR` output goes low.

This 15-ms delay enables the low-voltage power rails to sequence down in the correct order required by the SoC before the front-end power supply becomes disabled. The

delay times between `EN_VBAT_PWR` and `EN_LV_PWR` rising or falling are configurable by changing the count of the delay lines.

Selecting the PLD inputs to be Schmitt-trigger inputs provides leeway in how fast the logic signals driving into them need to transition. The two enable output signals are configured as push-pull. (If using open drain instead, then this configuration gives a glitch on power-up, as the open drain outputs are pulled momentarily high by the pullup resistors before the one-time programmable memory, OTP, of the TPLD801-Q1 has loaded and configured the outputs to be open drain. Even with push-pull, the outputs are high



4. An 18-V `ENABLE_IN` signal is applied to the enable controller, which certainly has an amplitude that lets the `TPS7B85-Q1` comparator pass it to the PLD. `TPS7B85-Q1` SI pin voltage for a 18-V `ENABLE_IN` signal is shown in red and the `ENABLE LATCH` internal PLD voltage in blue.

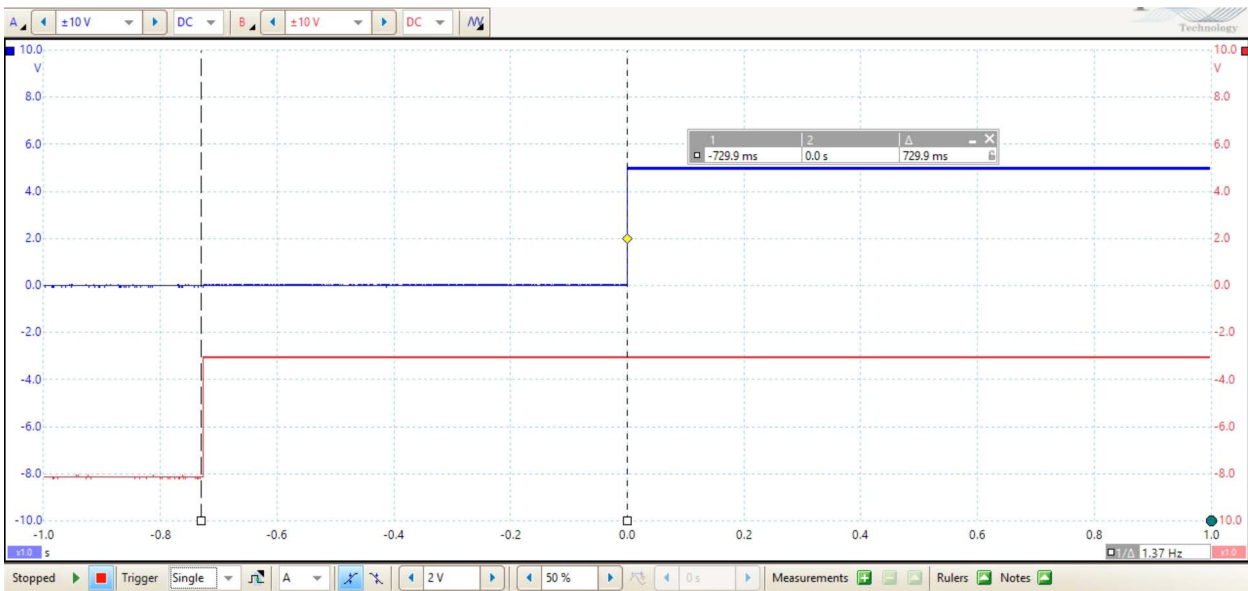
impedance before the OTP memory loads; thus, you may need external pull-down resistors.) *Figure 3* shows the overall PLD design.

Bench Test Results for the PLD/LDO Combo

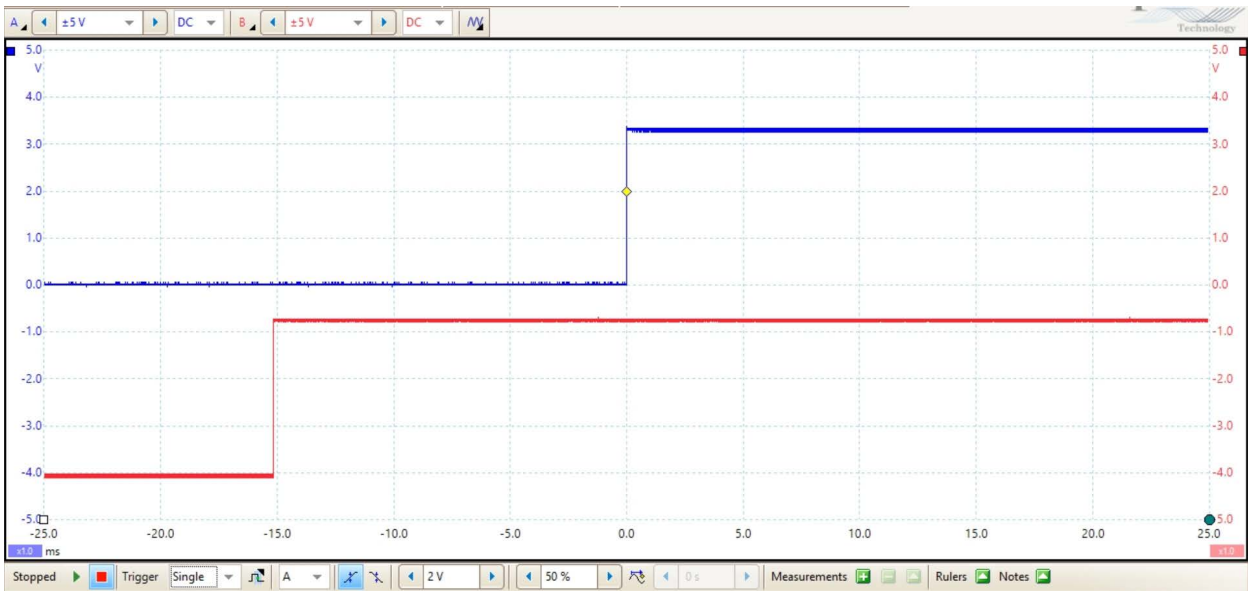
Figure 4 shows an 18V ENABLE_IN signal applied to the enable controller, which certainly has an amplitude that makes it possible for the TPS7B85-Q1 comparator to pass

it to the PLD. The signal also has a sufficient duration for detection being validated by the PLD. The ENABLE LATCH latches high in response to this ENABLE_IN signal and stays high even if the ENABLE_IN is toggled.

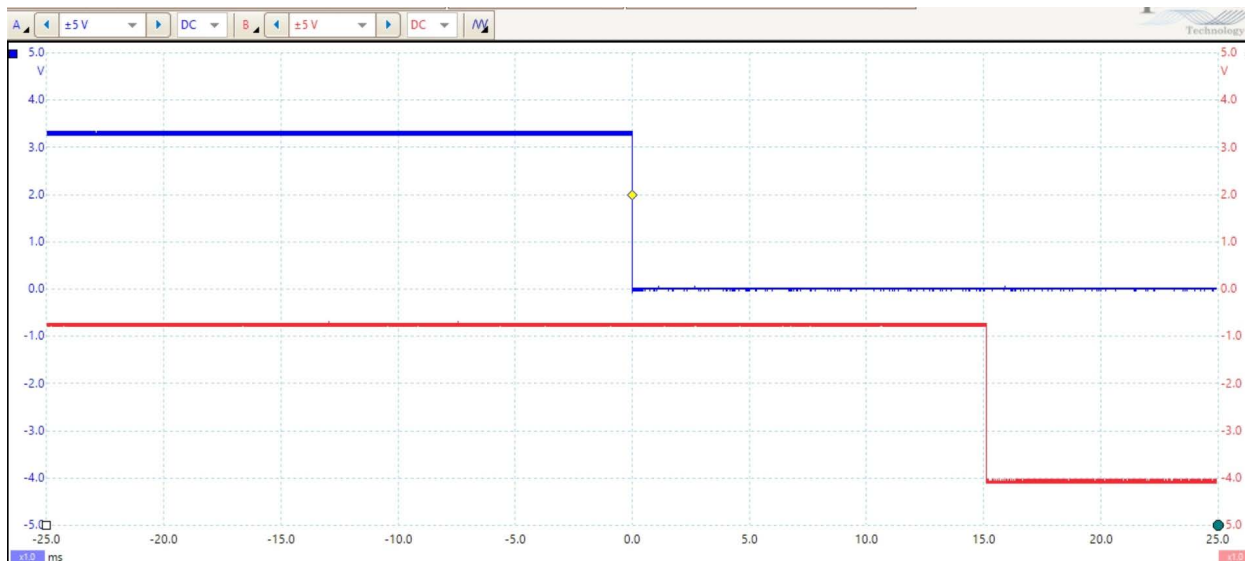
It's possible to successfully repeat this test for a low-amplitude, 3.4-V signal at the other extreme. Or you can repeat the tests for short duration, low-amplitude ENABLE_IN signals, or both, which are insufficient in duration or amplitude



5. This diagram reveals the behavior of the circuit when first applying the input power to the LDO. The TPS7B85-Q1 PG pin voltage is shown in red on first power-up and the ENABLE LATCH voltage is in blue.



6. These are the actual outputs of the PLD, including an approximate 15-ms delay during the power-up sequence. The EN_VBAT_PWR output is shown in red and EN_LV_PWR's output in blue from the PLD.



7. This highlights the sleep behavior, showing the EN_LV_PWR (blue) going low followed by the EN_VBAT_PWR signal (red).

to trigger the ENABLE LATCH to be high.

Figure 5 illustrates the behavior of the circuit when first applying the input power to the LDO. The PG pin goes high when the LDO regulates, and after a delay (set by CDELAY), the first power-on event is detected by the PLD and the ENABLE LATCH latches high. (This test used the default 1- μ F CDELAY capacitor of the evaluation board, which gives a much longer delay.)

The actual outputs of the PLD are shown in Figure 6, including an approximate 15-ms delay during the power-up sequence.

Figure 7 shows the PLD outputs during a DISABLE event, depicting the 15-ms delay.

Why the PLD/LDO Combo is Better than a Microcontroller

This low-cost and low-power, hardware-based solution for handling power-supply enable and disable functions removes the need for an external MCU and can be further customized. You also have the option of ordering a custom PLD with the logic design pre-programmed on it.

A pre-programmed PLD avoids the time and cost of writing and maintaining firmware for an MCU. Moreover, it avoids having to program an MCU in your production environment. These time-saving features of having the pre-programmed PLD and the fact that the TPLD801-Q1 and TPS7B85-Q1 hardware solution is low cost saves overall system expense.

The TPLD801-Q1 is available in a small package measuring 1.6×2.1 mm and the TPS7B85-Q1 comes in a 3-

$\times$ 3-mm package, which saves space in the overall printed circuit board layout. This is helpful to printed-circuit-board designers who often face the task of having to fit more functionality into the same board area.

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Dan Tooth is a Member of the Group Technical Staff at Texas Instruments. He joined TI in 2007 and has been a field application engineer for over 17 years. Dan focuses on the automotive and industrial markets and is responsible for supporting the TI analog and power product portfolio in ADAS, EV, and diverse industrial applications. He specializes in power-management and signal-chain applications. Dan graduated from the Loughborough University with a BEng in electrical and electronic engineering in 1994, a PhD in Power Electronics in 1999, and an MBA in 2004 from Heriot-Watt University.

References

1. “[TPS7B85-Q1 150-mA, 40-V, Low-Dropout Regulator with Power-Good and Integrated Voltage Monitoring](#),” Texas Instruments datasheet, literature No. SBVS360A, February 2020, revised November 2020.
2. “[TPLD801-Q1 Automotive Programmable Logic Device with 6-GPIO](#),” Texas Instruments datasheet, literature No. SCPS301, September 2024.