Electronic Design

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Meeting AI Data-Center Power Demands with Next-Gen Power Protection

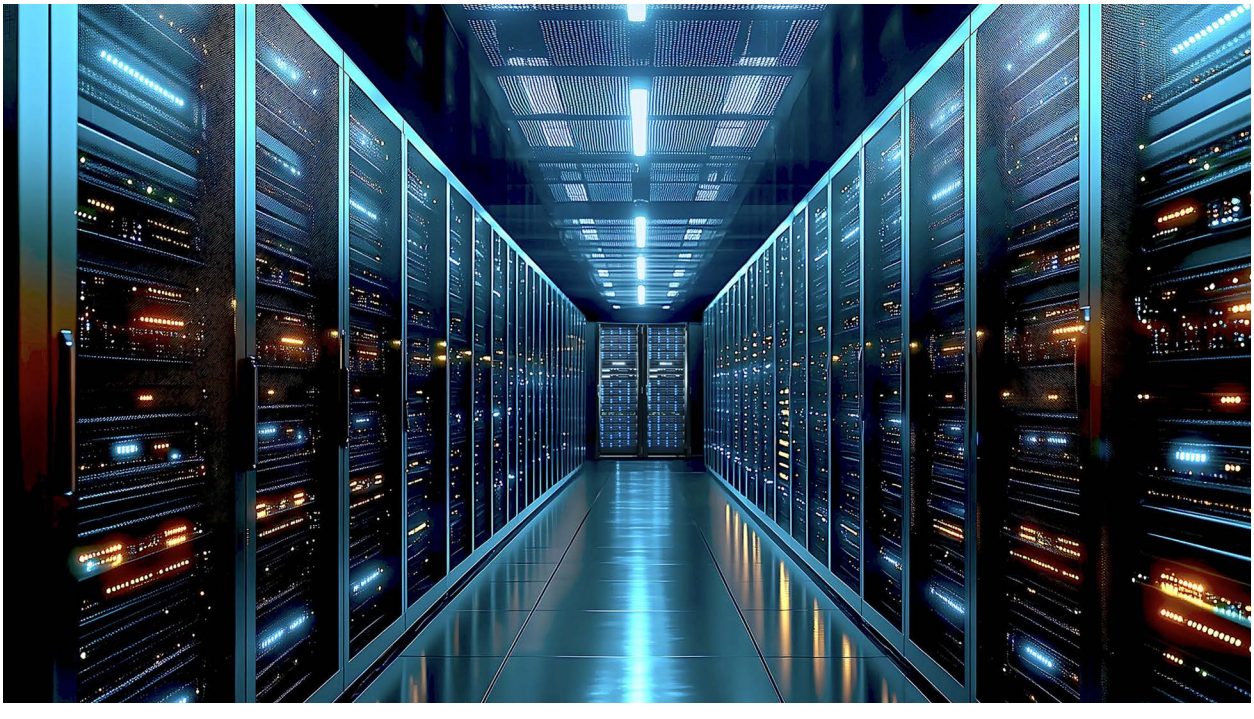
Sponsored by Texas Instruments: A new family of GaN power stages plus an advanced eFuse current-limit approach helps designers achieve safe, high power for modern data centers.

As high-performance computing and artificial-intelligence (AI) usage continues to escalate across the industrial landscape, data centers demand power-dense, efficient solutions to support the latest central processing units, graphics processing units (GPUs), and hardware accelerators.

A normal Google search requires about 0.3 watt-hours of electricity, but if you do the same search with AI using a large language model (LLM) or ChatGPT, it requires an estimated 10X the amount of power. To deliver larger amounts of power, you must extend to higher and higher voltages to reduce the current (because there's an I^2R loss).

To get ahead of the problem, data-center designers have been shifting to 48-V power architectures for enhanced efficiency and scalability to support these power-hungry devices. And it won't stop there: In the future, we're looking at 400- to 800-V energy funneling directly into the servers.

The need for increased power density and the shift to



TI's new TPS1685 hot-swap eFuse supports more efficient and power-dense data centers. (Source: TI)

higher power architectures introduces new challenges, though. As the demand for power ramps up, it can strain existing infrastructure and lead to overloads or failures. For starters, scaling power systems can be difficult and costly. And higher power density translates to more heat generation, which may lead to overheating and performance degradation.

Thus, different architectures are needed. On that front, Texas Instruments (TI) announced new power-management chips to support high-performance computing and AI in data centers. These PMICs include a new family of integrated gallium-nitride (GaN) power stages in transistor outline leadless (TOLL) packaging.

48-V Power Architectures

The way to get more power is to elevate the voltage. And we're talking up to a few hundred kilohertz higher. One way to process such power and deliver it efficiently is through faster switching, because that will require fewer magnetics and less area, and it will generate less heat.

However, if you're going to switch faster—all the way up to megahertz-type switching—at a high voltage, only one switch really does that in the under-20-kW range, namely GaN. It's simply the best power switch in the world right now—it requires the least amount of energy to turn on and the least amount of energy to reliably turn off.

Integrated GaN Power Stages

TI's new GaN power stages include the LMG3650R035 (650 V, 35 mΩ), LMG3650R025 (650 V, 25 mΩ), and LMG3650R070 (650 V, 70 mΩ). They come with an integrated driver and protection, and are housed in industry-standard TOLL packaging to simplify design.

The power stages incorporate a high-performance gate driver with a 650-V GaN FET, achieving high efficiency (>98%) and high-power density (>100 W/in.^{3}). The TOLL package speeds up the process of adding the GaN devices to existing designs.

For instance, by integrating a hot-swap controller with a 650-V GaN field-effect transistor (FET), the TPS1685 combo circuit protection and power-management IC reduces the solution size by half compared to existing hot-swap controllers in the market. It eliminates the need for a sense resistor and current-sense amplifier for current monitoring. The chip is housed in a 30-mm², low-profile quad flat no-lead (LQFN) package.

The TPS1685 provides multiple protection modes using only a few external components, including defense against overloads, short-circuits, and excessive inrush current. Applications with specific inrush-current requirements can set the output slew rate with a single external capacitor. A user-adjustable overcurrent blanking timer allows for systems to support transient peaks in the load current without tripping the eFuse.

eFuse Implementation

Traditional parallel operation of eFuses can present significant challenges given mismatches in the drain-to-source on-resistance ($R_{DS(on)}$), PCB trace resistances, and comparator thresholds. These mismatches result in uneven current sharing among eFuses and can cause premature tripping of individual eFuses, even when the overall system current is below the trip threshold.

To address these challenges, TI has introduced a total system current-limit approach in its eFuses *(see figure)*. This approach designates one eFuse as the primary controller to monitor the total system current. By relying on the total current rather than individual eFuse currents, the system avoids inaccuracies caused by mismatched path resistances and ensures that the system trips only when necessary, enhancing operational stability.

An evaluation module (TPS1685EVM) is available for the TPS1685. It incorporates two devices in parallel to evaluate a 54-V (typical) and 40-A (steady state) design that supports 2-kW input power-path protection at an input voltage of 48 V.

Summary

TI has put together a package with what's considered the best switching element—the GaN FET—plus the intelligence and diagnostics to streamline datacenter design and enable engineers to support rapidly growing power needs. It also includes BCD process technology that integrates bipolar, CMOS, and DMOS transistors on a single chip, enabling the creation of power ICs with high integration, smaller footprints, and lower power consumption.

The new power stages achieve high efficiency and high power density, and they integrate advanced protection features including overcurrent protection, short-circuit protection, and overtemperature protection. This is especially important for AC-DC applications such as server power, where designers are challenged to push more power into smaller spaces.