Electronic Design

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Taking a Quantum Leap from Lab to Fab

The road to a billion qubits: Achieving integration of semiconducting and superconducting qubits with full industrial 300-mm wafer fabrication.

Quantum computing is arguably one of the hottest topics in research right now. Quantum computers harness the power of quantum mechanical phenomena to solve certain problems faster than the best classical computers. If developed to a sufficient level of maturity, they could one day help compose the perfect medicine on a molecular level as well as help solve other—currently intractable—problems in materials research, chemistry, numerical mathematics, and cryptographic spaces.

The keyword here is "could." Before quantum computers become practical (that is, capable of solving currently intractable problems), major hurdles must be cleared. Notably, scaling up the number of qubits—the information units in these devices—remains a key barrier.

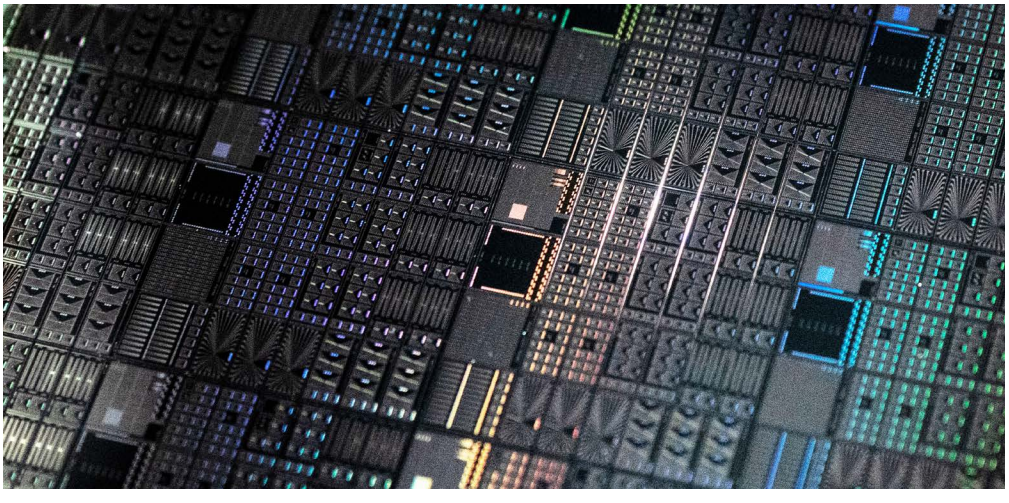
Qubits are notoriously unstable and prone to mistakes. Therefore, many millions of qubits working in unison are required to correct said mistakes and thus faithfully perform the transformational calculations promised by quantum computers.

To obtain a billion qubits, fabrication must be taken from lab to fab, thereby addressing yield and variance issues. Advanced industrial CMOS process flows allow for wafer-scale uniformity and high device yield, yet in a very different and highly optimized space: Off-the-shelf transistor processes can't be directly transferred to qubit structures due to the different designs and operation conditions in those devices, compared to quantum devices. Yet modifications of those processes, when properly matched to the requirements of qubits, could significantly address current qubit limitations.

Recent work of imec researchers now demonstrates the successful integration of semiconducting and superconducting qubits with a customized 300-mm wafer fabrication line *(Fig. 1)*. Moreover, imec's silicon (Si)-quantum-dot-spin-based qubits display record-low charge noise levels (average charge noise is 0.61 μeV/√Hz), a critical parameter to maintain quantum coherence.

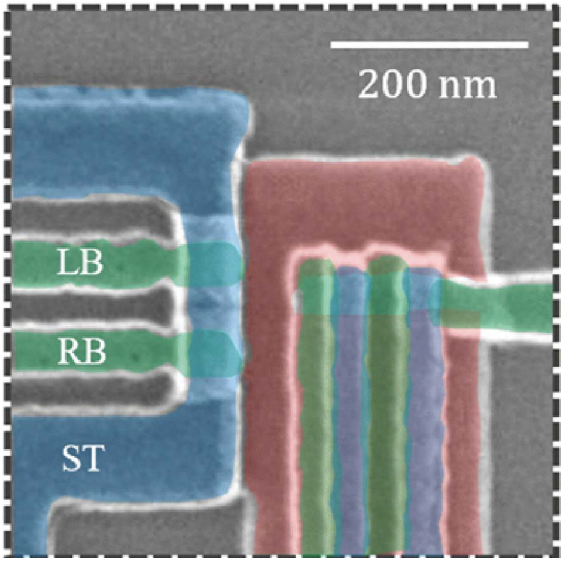
Silicon Spin Qubits: Tackling Charge Noise and Gate Defects

imec's silicon spin (Si spin) qubits are defined by semiconductor quantum dot structures that trap a single spin of an electron or hole. A major advantage of these qubits



1. The Si spin qubits are manufactured with state-of-the-art 300-mm integration flows. (Credit: imec)

for fabrication in semiconductor fabs or industrial lines lies in their close compatibility with existing Si-based manufacturing processes. Though there are several demonstrations of fab-made Si spin qubits, the final qubit performance typically shows higher noise and, therefore, lower coherence and fidelity compared to qubits made in a lab environment or academic cleanroom.



2. Shown is a scanning electron microscope (SEM) image of the overlapping qubit structure. (Credit: imec)

Coherence is the metric for the ability of qubits to be able to store quantum information for a long time, which is essential for performing quantum information processing tasks. It directly affects the fidelity of qubits—another quantum metric that defines the faithfulness with which a qubit can perform a certain operation.

Charge noise has been identified as one of the main culprits for reduced coherence. To keep the charge noise as low as possible, and thus achieve long coherence times, the quality of the Si/SiO_2-based metal-oxide-semiconductor (MOS) gate stack turns out to be paramount.

While this can be realized through lab-based techniques such as lift-off processes, which allow, in principle, for "gentle" processing, industrial manufacturing techniques like subtractive etch in reactive ion plasmas and lithography-based patterning have shown to easily result in degradation of the Si/SiO_2 interface quality. This is presumably due to the injection of charged defects during the plasma processing.

Through full gate stack optimization, including detailed analysis of the defectivity induced by different process steps, researchers demonstrate that the Si/SiO_2 interface—even with industrial processing—could provide very low-noise environments for qubit operations. This approach also offers the added advantage of higher yield and lower variance, which are the main arguments used in industrial CMOS processing to move away from lift-off and toward subtractive etching-based patterning.

The researchers found out that a medium-thick layer of high-quality, thermally grown oxide combined with polysilicon gates (instead of commonly used metal gates) and specific cleaning and etch processes yielded the best results. The optimized gate stack also showed a reduction in density of so-called spurious dots, unintended quantum dots defined by localized defects that form in the vicinity of desired quantum dots. Spurious dots affect the scalability of the qubits because they interfere with coupling of qubits, for example, in two-qubit gates between neighboring qubits.

The resulting qubits display charge noise that's up to an order of magnitude lower compared to previous state-of-the-art fab-based Si quantum-dot structures, and they achieve remarkably uniform quantum dot operation with high fidelity. In collaboration with researchers in Australia, the imec team demonstrated a record-high qubit control fidelity of 99.91% on the optimized devices—a result that was recently demonstrated at the 2024 Silicon Nanoelectronics Workshop attached to the annual VLSI conference. This confirms the maturity of industrial fabrication techniques for qubit development *(Fig. 2)*.

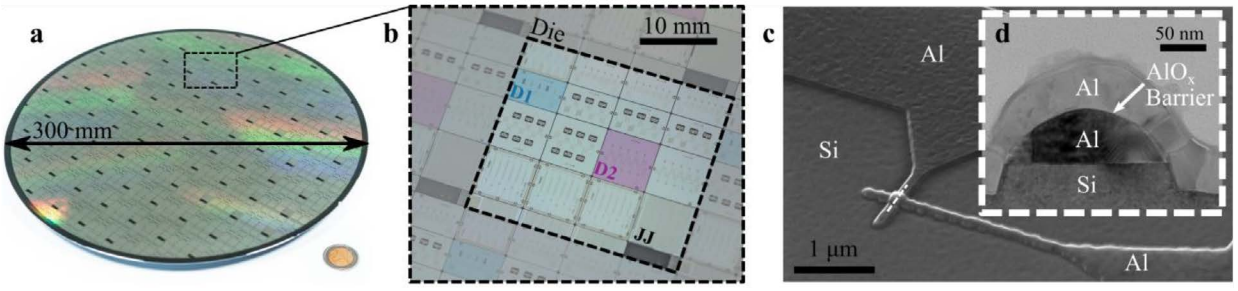
Si Spin Qubits: Further Optimization and Characterization

In the next steps, the researchers will further characterize the qubits and optimize the process, as well as assess larger quantum bit arrays. One of the outstanding questions remains how reduced charge noise could affect other metrics. For example, while reducing charge noise by using a thicker SiO_2 layer (from 8 to 20 nm) helps, it also increases crosstalk between different gates at the quantum dot, which can limit the fidelity of two-qubit gates.

Furthermore, the current process uses 300-mm industrial e-beam lithography, since that offers the flexibility to change the design at every iteration. However, the limited throughput of e-beam, and inherent limitations to the alignment accuracy of the gates, are drawbacks.

In contrast, optical lithography (the main workhorse of industrial CMOS technology) has been heavily optimized to reduce alignment errors. Therefore, moving from e-beam to optical lithography (in this case EUV lithography) should help in pushing the maturity of the processes.

Finally, upscaling and maturing single qubits is just the first step. Another challenge lies in integrating these qubits into functional arrays and letting them talk to each other. The current overlapping gate architecture is perfect to dem-



3. Photograph of the 300-mm wafer (a) and photograph of one die with highlights of Josephson Junction and qubit subdies (b). Tilted scanning electron microscopy (SEM) image of an overlap Josephson junction (c) and a cross-sectional transmission electron microscopy (TEM) image of the junction (d). (Credit: imec)

onstrate single- and two-qubit operations, but it will hit a limit going to tens or hundreds of qubits.

Consequently, the team is developing architectures that ensure scaling up to much larger arrays of qubits. Since such architectures require modified processes and development of a "quantum back end of line," compatibility with high-fidelity qubits will remain the primary focus in this effort.

Superconducting Qubits: Bringing Superconducting Qubits from Lab to Fab

While Si spin qubits are very promising in the long run because of their advantage for upscaling with their smaller size, long coherence times, and high integration density, as well as their close compatibility with CMOS manufacturing technologies, superconducting quantum circuits are arguably the most developed platform at the moment.

The energy states of superconducting qubits are easy to control and made to interact with each other, and that combination has led to demonstrations of medium-scale quantum processors coupling tens to hundreds of superconducting qubits together. These qubits show—in a lab environment—long coherence times (up to several 100 µs) and high gate fidelities (99.995% for single qubits), two important benchmarks for quantum computing.

Most of the superconducting qubits, however, are still made in laboratories where techniques such as shadow evaporation and lift-off are "gentle" processes that help produce extremely clean interfaces. This is particularly critical for the key element of a superconducting qubit: the Josephson junction (JJ).

To maximize coherence time, the various interfaces contained in the structures that make up the junction and the rest of the qubit must be as clean as possible. Even a single unlucky atomic defect present at one of the interfaces can cause the qubit to lose coherence. Unfortunately, these fabrication techniques are not fab-compatible and generally difficult to scale up, thereby challenging the production of larger numbers of qubits needed for quantum computing.

Earlier work from imec researchers already demonstrated the feasibility of creating the JJ using only CMOS-compatible materials and techniques in the lab. This so-called overlap JJ is created by overlapping a top electrode and a bottom electrode with a thin insulator layer in between.

Now, the researchers successfully transferred this process to a full fab environment. Superconducting qubits are manufactured on 300-mm silicon wafers using exclusively optical lithography and reactive ion etching with an impressive 98.25% qubit yield.

The qubits display excellent coherent times in excess of 100 µs, thereby establishing that the quality of the interfaces is sufficiently clean using fab-compatible processing steps. In addition, the imec team observed very good stability or aging of the JJ, significantly better than in the lab.

Shadow-evaporated JJs often show notable aging—increases in resistances of the junction over time indicate how it will behave when placed in a qubit and cooled down. These room-temperature resistances can drift from one day to another day by tens of percent, while the new overlap JJ is very reliable with only a few percent aging *(Fig. 3)*.

Superconducting Qubits: Improving Process Control and Exploring 3D

The researchers established for the first time a fabrication process on 300-mm silicon wafers achieving high coherence and across-wafer yield. The next step is to improve process control. This will tackle, for example, the observed qubit-to-qubit and wafer-to-wafer variability. In addition, various surface treatment, cleaning techniques, and new materials will be further explored, to keep improving the interface and with that qubit coherence time.

In the longer term, when moving beyond a few tens of qubits, 3D integration techniques will be paramount. First, to connect the qubits. Current solutions such as air bridges aren't ideal; they introduce crosstalk and surface losses. Second, to ramp up the number of qubits, keeping in mind that superconducting qubits are very large (millimeter size)

compared to, for example, transistors. These can't be significantly scaled down in 2D.

Even though moving to fab processing opens up access to state-of-the-art 3D technology, 3D integration remains very complex. One of the critical hurdles is protecting the JJ during stacking. Any 3D processing that happens after fabrication of the JJ can't affect or destroy it. For example, one hurdle to consider is that the thermal budget is restricted to 200°C, while established processes require significantly higher temperatures.

Conclusion

Integration of semiconducting and superconducting qubits with full industrial 300-mm wafer fabrication has been achieved with reproducible and high-yield qubits. The results confirm the maturity of industrial fabrication techniques for qubit development. This is a necessary leap to make systems based on hundreds and thousands of qubits work.

Kristiaan De Greve is Fellow and Program Director of Quantum Computing at imec, as well as a professor of electrical engineering at KU Leuven. He joined imec near the end of 2019 from Harvard University, where he was a Fellow in the physics department and retains a visiting position. Kristiaan is an electrical engineering graduate of KU Leuven, and obtained his Ph.D. in Electrical Engineering from Stanford University in 2012 as a Stanford Graduate Fellow, with award-winning Ph.D. research under Professor Yoshihisa Yamamoto on novel types of spin qubits, ultrafast means to manipulate such qubits, and pioneering experiments into the limits of light-matter qubit entanglement. At Harvard, he worked with Misha Lukin and Amir Yacoby to push the limits of magnetic quantum sensing as well as develop the world's smallest MRI system, and with Misha Lukin, Hongkun Park, and Philip Kim to develop two-dimensional semiconductors into a model platform for textbook quantum optics experiments in reduced dimensions. Besides his scientific interests, he holds additional physics, economics, and business degrees from Stanford and Harvard University.

Clement Godfrin is an imec Device Engineer working on silicon spin qubit. He received a nanophysics Master degree from Paris Saclay University and a PhD degree from Grenoble Alpes University. He came to imec in 2019, from a post-doc position at Sherbrooke University in Canada. Over this journey in the field of quantum computing, he specialized in the dynamics of single nuclear high-spin, also called qudit, either to implement quantum algorithm proof of principle on single nuclear spin of a molecular magnet system, or quantum error correction protocol, on single donor nuclear spin.

Shana Massar achieved double Master of Science (M.Sc.) degrees in Chemical and Materials Science Engineering from the Universite Catholique de Louvain (UCLouvain, Louvain-la-Neuve, Belgium) and in Functional Advanced Materials Engineering from Augsburg Universitat (Augsburg, Germany). Shana Massar joined imec in 2020 as Development Engineer supporting the integration of the SpinQubit project. She then moved to the position of R&D Engineer and is now leading the integration of the Superconducting Qubits project.

Anton Potočnik is a Senior Researcher at imec, where he's exploring quantum computing based on superconducting circuit technology. His main topics of interest are investigating sources of decoherence in qubits, interfacing qubits with cryo-CMOS electronics, and exploring novel techniques for scaling up superconducting quantum devices. Before joining imec, Anton was a postdoc at ETH Zurich in Prof. Wallraff's group, where he worked on analog quantum simulations. One of his notable achievements was modeling photosynthetic processes with superconducting devices. Anton received his PhD in physics from the University of Ljubljana in 2013. During his undergraduate studies, he worked on exotic superconductivity and his work led to the discovery of a new type of matter called the Jahn-Teller metal.