Electronic Design

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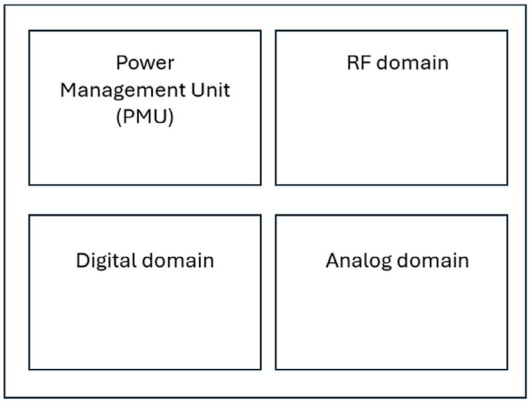
Addressing RF Coupling in Wireless SoC System Design

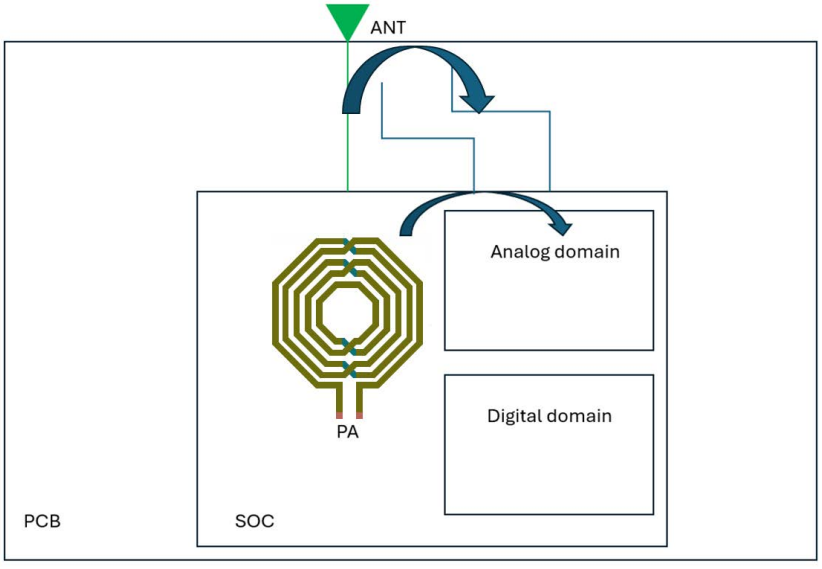
RF coupling is one of the most important and tricky issues that RFIC designers always must confront while developing wireless SoCs.

Wireless system-on-chip (SoC) designs require implementing all circuit domains on the same die. This enables manufacturers to reduce cost and support integrity. On the other hand, crosstalk between these domains can be problematic and degrade the overall performance.

Electromagnetic interference (EMI) is caused by radiated radio-frequency (RF) signals. Various techniques are available to lower EMI in system design. For instance, radiated RF can be addressed with filtering and shielding; however, this doesn't mitigate on-chip RF coupling.



1. The annotated domains are typically found within wireless SoCs (Credit: Si-Vision).



2. The arrows indicate possible RF coupling mechanisms in a wireless module (Credit: Si-Vision).

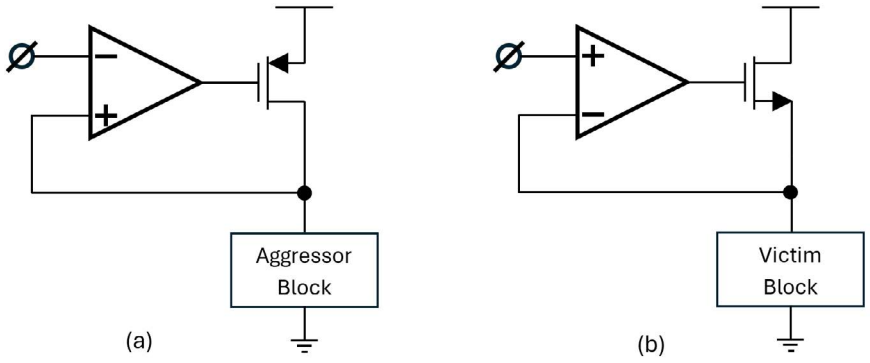
Channels for RF Coupling

RF coupling is an example of crosstalk between the RF domain and other domains *(Fig. 1)*. Wireless transmitters are required to generate output power in the range of ~10 dBm. Power amplifiers (PAs) generate these levels of power while sometimes incorporating on-chip inductors or transformers.

Due to electromagnetic radiation of the inductors, a fraction of the transmitted power can couple to other domains inside the SoC. Whether the coupled component is at the same transmitted frequency or its harmon-

ics, it degrades transceiver performance. This becomes evident when the output signal spectrum of the integrated frequency synthesizer becomes spurious.

The same coupling mechanism can happen outside the SoC on the PCB level, where the antenna will radiate and impact critical PCB routes of other domains near to it *(Fig. 2)*.



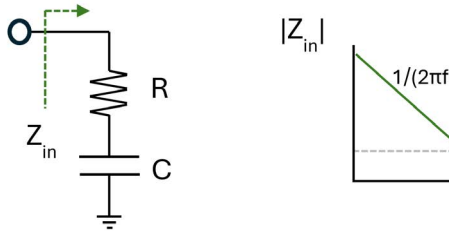
3. Shunt regulators protect the supply from aggressor blocks (a). Series regulators protect sensitive blocks from supply noise (b) (Credit: Si-Vision).

Reducing RF Coupling

Generally, any block that operates at an arbitrary frequency (f_1) is considered an aggressor for a victim block that operates at another frequency (f_2) and vice versa. There can be exceptions when one frequency is an exact integer multiple of the other.

The links through which the aggressors affect victims include:

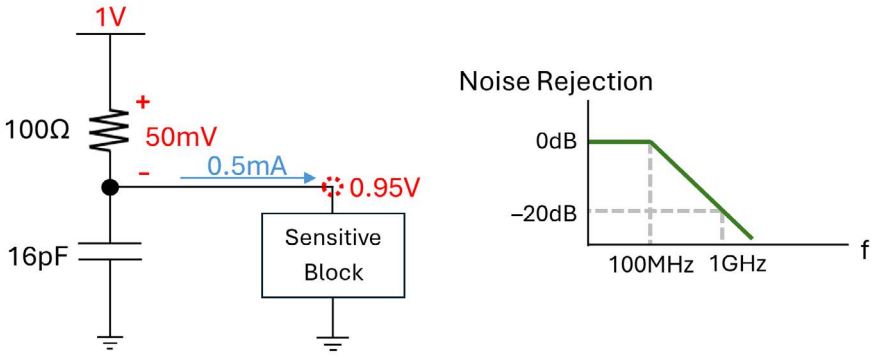
- Supply networks
- Parasitic capacitive coupling
- Parasitic magnetic coupling
- Substrate coupling



4. Parasitic resistors in series with supply decaps degrade their performance (Credit: Si-Vision).

Reduction of Supply Network Coupling

Different regulators can be used to decrease coupling through supply networks. Consider an aggressor block that's insensitive to supply noise. Such a block should be supplied from a shunt regulator,[1] like that in *Figure 3a*. The reverse power-supply rejection ratio (PSRR), which is the signal transfer function from the regulator output to its supply, is small.

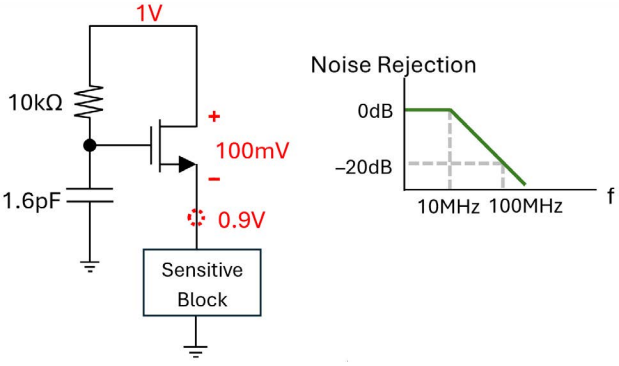


5. This is an example of a reasonable tradeoff between supply headroom and noise filtration in a passive supply filter design (Credit: Si-Vision).

Similarly, sensitive blocks to supply noise, which have negligible contribution to supply contamination, should be supplied from series regulators[1] *(Fig. 3b)*. Forward PSRR, which is the transfer of supply noise to the regulator output, is small in series regulators.

Another common way to decrease coupling through supply networks is by adding an ample capacitance of supply decoupling capacitors near each block. However, this must be done carefully to maximize the range of frequencies in which the decoupling capacitors are effective.

Parasitic resistance of the decoupling capacitor routing should be minimized to increase its quality factor. When the decoupling capacitors are realized by MOS devices, the length of the unit decoupling capacitors should be mini-



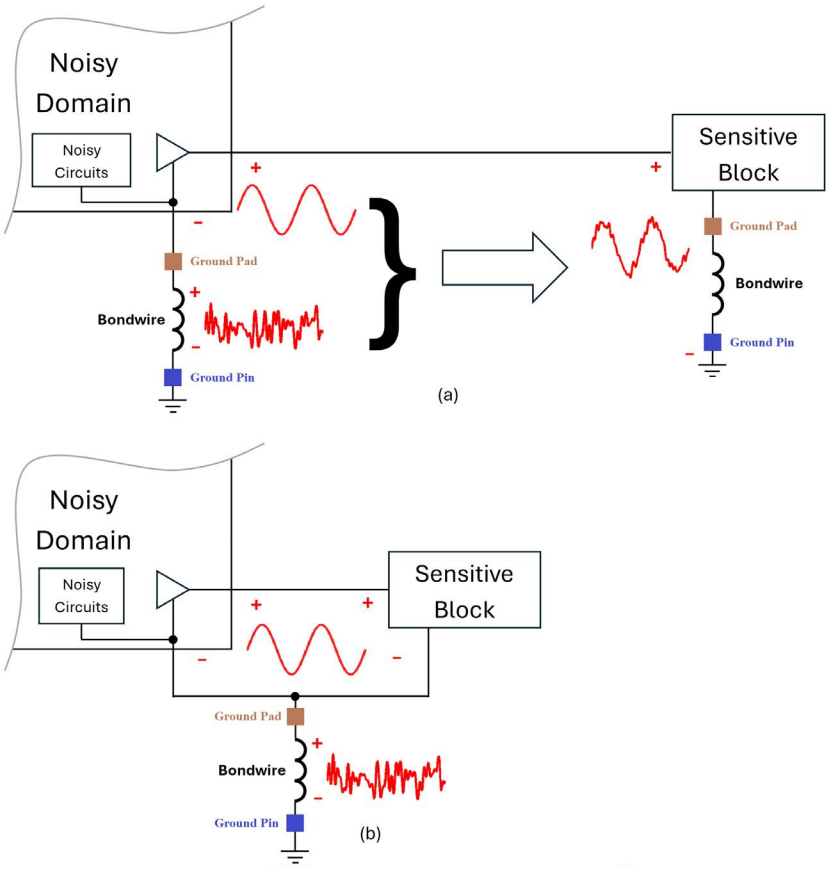
6. The filter capacitance can be greatly decreased in the active supply filter, which results in a compact design (Credit: Si-Vision).

mized to decrease its channel resistance.[2] Impedance of a capacitor in series with a parasitic resistor saturates at the parasitic resistance value at high frequencies *(Fig. 4)*.

One infrequently used technique to mitigate supply network coupling is to add passive or active supply filters.[1] Design engineers may initially reject this idea as there's an associated loss of supply voltage headroom. However, consider a block that has a 1-V supply and consumes 0.5 mA *(Fig. 5)*.

Insertion of a 100-Ω resistor decreases the supply headroom by just 50 mV. When the added filter capacitance is 16 pF, supply noise at 1 GHz gets attenuated by 20 dB. A similar argument can be made for the area-efficient active filter utilizing a native NMOS device *(Fig. 6)*.

Finally, separating ground connections of different blocks and connecting them to different pads may lead to severe issues.[3] Separation can contaminate sensitive blocks instead of isolating them. This counter-intuitive mechanism is illustrated in *Figure 7*.



7. The input signal to a sensitive block can be contaminated when the ground pads of the communicating domains are separated (a). The same signal is safely transferred when the ground pad is shared (b) (Credit: Si-Vision).

Reduction of Parasitic Capacitive Coupling

Parasitic capacitive coupling is handled on the layout level. Sensitive and noisy nodes should be shielded with their reference supply rails. Ground plane design can help as well.

Capacitance is inversely proportional to distance between conductors; therefore, increasing spacing between traces will help.

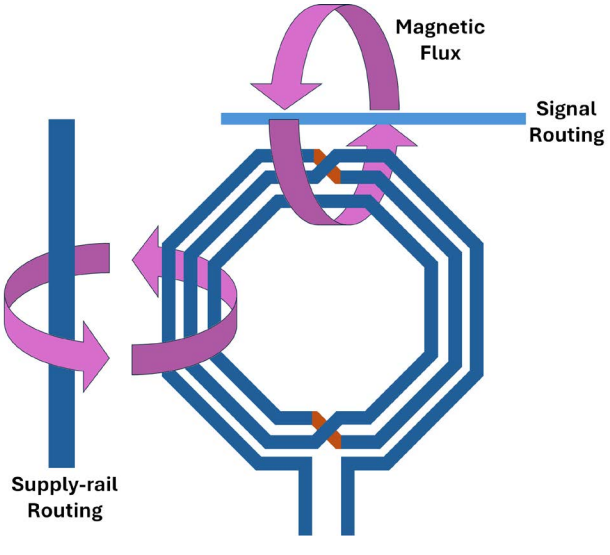
Reduction of Parasitic Magnetic Coupling

Long routes can be magnetically coupled to each other when they have the same orientation. This effect is more pronounced when coupling occurs between a long parallel route to one side of a spiral coil *(Fig. 8)*. The situation worsens when the coil carries currents of both high frequencies and large magnitude, as in the case of power amplifiers.

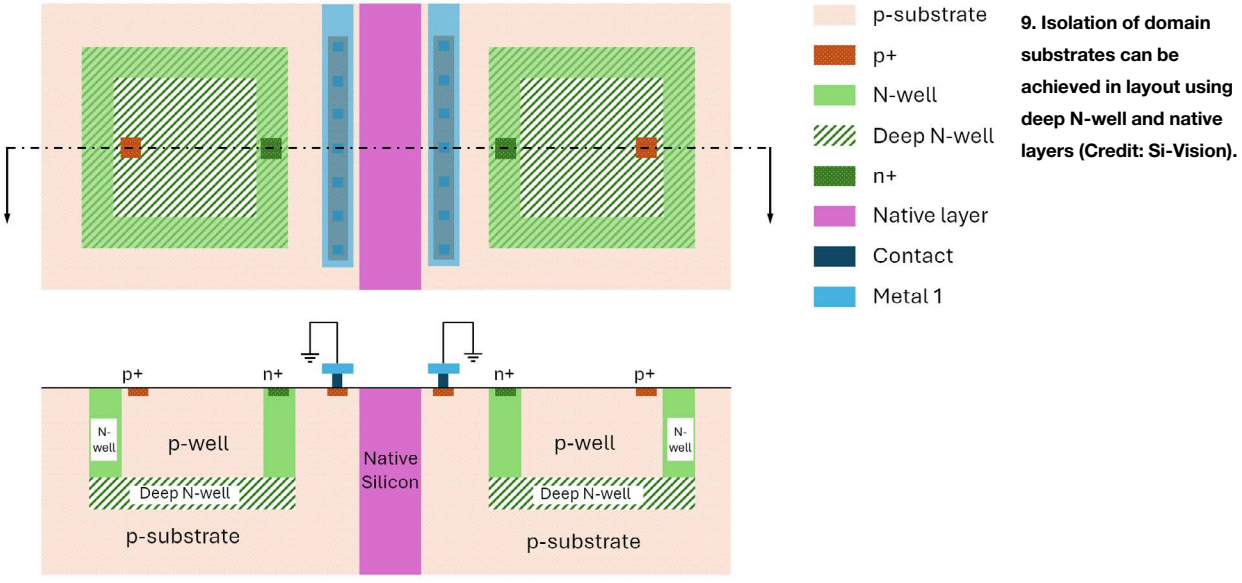
To diminish this magnetic coupling, sensitive routes should be as far as possible from coils and other noisy routes. Also, when routes are orthogonal to each other, magnetic coupling decreases substantially.

Reduction of Substrate Coupling

Sometimes noise coupling can occur through the sub-



8. Magnetic coupling between a spiral coil and adjacent long routes is a serious concern (Credit: Si-Vision).



9. Isolation of domain substrates can be achieved in layout using deep N-well and native layers (Credit: Si-Vision).

strate. To overcome this, different circuits can be isolated into wells using the deep N-well layer. Moreover, the high-resistivity native layer should be added in between the isolated domains, with adjacent bulk ties that provide low-impedance paths to different ground pads.[4] This technique is illustrated in *Figure 9*.

Finally, a couple of guidelines can be followed to further decrease noise transfer from one domain to another. Differential signaling should be used whenever possible for inter-domain connections. This minimizes transfer of the reference node noise. Also, the signal drivers at the boundary of one domain could be deliberately weakened to minimize the electrical transfer of all signals to other domains. This approach is very effective when handling CMOS logic signals, such as high-speed clocks and digital buses.

Don't Overlook Coupling Reduction Techniques

RF coupling in wireless SoC systems can be a real problem and could degrade overall performance. Special attention should be paid when designing the SoC floorplan and identifying aggressor and victim blocks. Coupling reduction techniques should be implemented to get the required high performance.

Karim Saleh received B.Sc. and M.Sc. degrees in electronics and communication engineering from Ain Shams University, Cairo, Egypt in 2004 and 2011, respectively. From 2006 to 2011, he was an RFIC design engineer at SySDSoft Inc.; from 2011 to 2014, he worked at Intel Egypt IMC; from 2014 to 2022, he worked at ADI/Bosch Ireland; and since 2022 he's been Analog design manager at Si-Vision Egypt. His work involves circuit design of RF transceiver and analog/digital PLLs.

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