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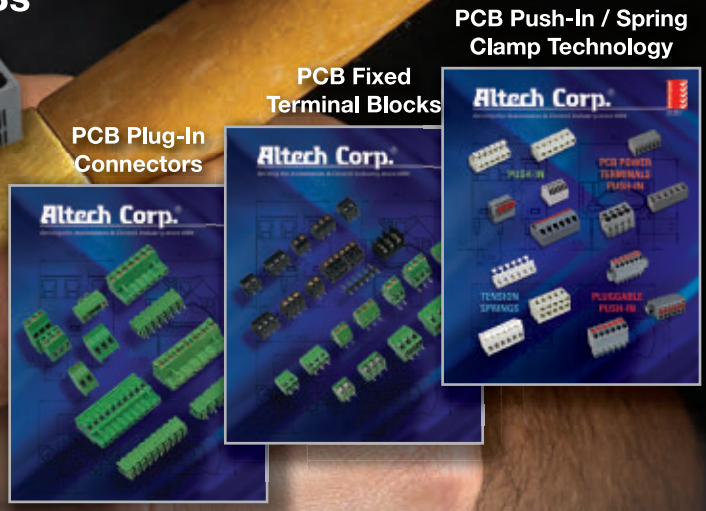

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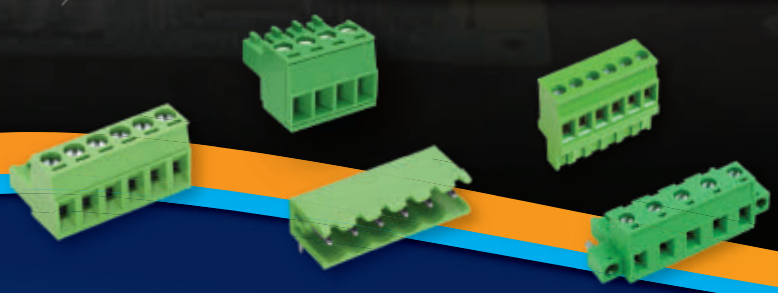

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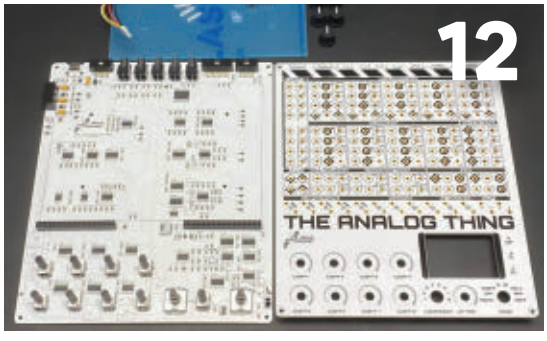

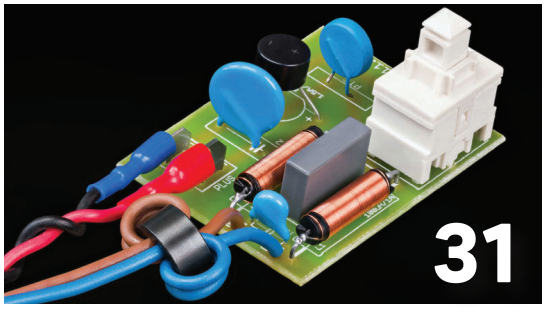

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BILL WONG | Senior Content Director

Electronic Design's Focus Amid Changing Times

From special reports to audience surveys, Electronic Design is going all digital all the time. Editorial Director Bill Wong dives into the publication's plans.

THIS NOVEMBER/DECEMBER ISSUE of *Electronic Design* wraps up over 70 years of regular print and then PDF versions of our issues, which subscribers have been reading over all these years. Our 75th anniversary will be in 2027.

Electronic Design has had an online digital focus for a long time. We have more articles than would fit into the print issues since I started with *Electronic Design* in 2000. We picked the best to go into the print edition and lately the PDF version. Physical print issues went away a while ago. It's just too expensive to print and ship these days, and most readers are using our website already. The number of readers has always been higher due to our limited subscription base.

Finding New Content on *Electronic Design*

As with most publications, we have a host of *Electronic Design* newsletters that provide regular notification of new articles. Those interested in similar functionality to our PDF issues should check out our Top Stories of the Week. These are collections of the articles we have on the website for the week just in case you miss one, or if you prefer to scan the list rather than receiving a newsletter. Of course, you can do both as the newsletters tend to be a targeted subset for topics like power or automotive.

Top Stories of the Week is handy, but it only groups things by date. So, what we've been doing over the last few years is building our curated TechXchanges. These focus on a topic and incorporate new articles as they arrive, as well as collect evergreen content that *Electronic Design's* editors have chosen as useful for the topic.

TechXchanges are more focused than our technology channels like Analog and AI/ML. These list all of the articles for the topic with the most recent ones residing at the top, but the subject matter is typically very broad.

One example is the Engineer's Guide Oscilloscope Techniques *(see figure)*. This is actually an overarching TechXchange that groups more detailed subcategories into their own separate TechXchanges, like Choosing an Oscilloscope and What's the Difference: Oscilloscopes. You can also leave suggestions for additional articles as we continue to update the TechXchanges with new content as it arrives.

Electronic Design's TechXchanges provide a curated list of articles on a particular topic that readers should find useful. ID 30131704 © Luchschen | Dreamstime.com

More Feedback and Research Reports

Many of you are probably familiar with our Annual Salary Survey and our Quick Polls. These have provided us with your insights, which was not possible with our print issues.

Our latest, "Is Mixing AI with Software Tools and Development a Good Idea?," includes a survey that we hope you will take. It will provide us with more insight into how everyone is using artificial intelligence and machine learning (AI/ML) in the design cycle rather than embedding it into a product.

We're looking forward to our 75th anniversary and providing readers with the latest articles, podcasts, and videos on existing and emerging topics relevant to *Electronic Design* engineers, programmers, and managers.

Inside Electronics Podcast:

NANO Nuclear's 5-MW Electricity Generator in a Shipping Container

INSANE LEVELS OF electrical power are needed to support AI in data centers, and the electrification of mobility means development of remote locations for the extraction of critical mineral resources. This includes the powering of fully electric 1-MW mining trucks.

A number of startups are developing small modular reactors (SMRs) in the 20- to 500-MW power output range, requiring extensive site development, construction, and support resources. However, NANO Nuclear Energy Inc. (NASDAQ:NNE) is uniquely positioned in the micro-reactor space with two commercial micro-reactor designs that output up to 5 MW, integrating them with the complete electrical generator housed in an ISO shipping container.

In this podcast, we discuss markets, applications, Red October "caterpillars," engineering design, and operational considerations of these micro-reactor systems with our guest, NANO Nuclear's CEO, James Walker.

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Video ▸ Examining EV Charging Infrastructure Issues

Electric vehicles (EVs) run on batteries that require periodic charging. A charging infrastructure is required to provide this power. In general, the deployment and maintenance of a national EV charging system is almost more challenging than the technology behind EVs and their batteries.

Electronic Design Content Director Bill Wong talked with Jeff Postelwait, Managing Editor at tdworld.com, and Janelle Penny, Editor in Chief at buildings.com, about some of the issues associated with building out such an infrastructure.

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Video ▸ Toshiba's New Ownership and Future

Toshiba was delisted last year after 74 years on the Tokyo exchange, following a decade of troubles for the company. The entity was taken private by a group of investors led by private equity firm Japan Industrial Partners.

The $14 billion takeover has the interest of Japan's government, as the company employs over 100,000 people and its operations are seen as critical to national security. In this video, we talk with Armin Derpmanns, VP of Marketing and Operations for Toshiba Electronics Europe, about the future of the company.

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2024 Engineer's Holiday Gift Guide

Our editors offer up some gifts that are fun, practical, and affordable for the full-time or budding engineer. You may wind up buying one of these suggestions for yourself.

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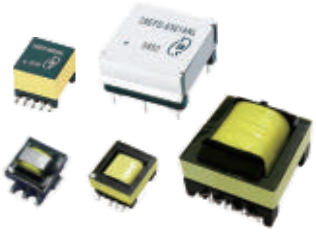

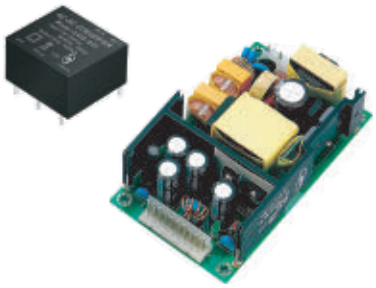

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TOBIAS BJERREGAARD | Sr. Director of AI, Synopsys EDA Group

Adopting AI-Based Circuit Optimization and Migration

Analog designs are challenging, but artificial-intelligence optimizations are improving and speeding up the design process.

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THE USE OF artificial intelligence (AI) has gained significant traction in many domains of EDA, and for good reason. AI learns from experience, adapts, and converges on a solution while considering conflicting goals with complex tradeoffs.

Such characteristics make AI highly valuable in tackling many of EDA's hardest challenges, where traditional optimization approaches—either manual or algorithmic—are either sub-optimal, too slow, or fail altogether. AI has the potential to revolutionize the way we design, optimize, and, in particular, migrate analog designs.

Traditional Optimization Approaches Fall Short

Advances in EDA algorithms have made it possible to scale digital chips to the size of billions of transistors. The scaling of digital design automation builds on abstractions of digital signal levels (1s and 0s) and synchronous operation (discrete time), allowing for a divide-and-conquer approach.

Analog design, on the other hand, doesn't benefit from such abstractions. Individual elements of the design influence each other in complex interactions, making it impossible to optimize one part of the circuit without affecting others. Also, the design metrics are complex, as designers need to consider dozens of metrics, such as supply current, signal-to-noise ratio, jitter, hysteresis, slew rate, CMRR, DC gain, and more across hundreds of process corners.

Due to these inherent complexities, analog design has remained a largely manual process. This puts severe limits on the potential to exploit the multitude of specialized sub-nodes made available from foundries to take advantage of market opportunities. To understand why this is so, let's look at where traditional optimization approaches fall short.

The purpose of optimization is, in essence, to deduce circuit characteristics (e.g., transistor sizes, layout placement, routing topology, etc.) that fulfill a desired outcome in terms of circuit behavior or performance (i.e., power consumption, noise margin, signal duty cycle, slew rate, etc.).

If the desired outcome can be modeled in a simple manner, with a model that's at least rank order correct, then a traditional optimization algorithm can be created. This has been done successfully in many of the individual steps of the digital implementation flow, leading to a highly automated optimization process.

For example, digital circuit performance can be modeled because circuit behavior is able to be simplified to timing delays—that is, optimization of static timing delays is essentially a linear problem. Analog circuits contain much more complex behavior. They build on nonlinear device models, with no simple proxy function.

Physically accurate models of analog circuits will simulate the exact behavior across all metrics, given the detailed circuit topology and parameters. However, due to the complexity of the underlying models, and of the interactions between the various elements in a design; even the simulation itself is an iteratively converging process. There's no sufficiently accurate, simplified way to emulate the outcome, and no way to move backwards from desired outcome to circuit characteristics.

Hence, analog design optimization has remained a largely manual process, which requires advanced designer expertise, time, and patience. *Figure 1* illustrates how the optimization step is a manually intensive and key step in a traditional analog design flow for migrating an analog design.

AI-Based Analog Optimization

AI-based approaches do well in addressing optimization problems where traditional algorithmic approaches fall short. AI holds the potential to automate the manual loops in the design process. Much like a human designer, AI performs and learns from experiments, combining learnings across each of the experiments to understand and navigate in the solution space. In general terms, this approach is called sample-based optimization.

Sample-based approaches such as grid search, i.e., parameter sweeping, and random search, i.e., Monte Carlo simulation, have traditionally been used to aid designers during the analog design process. However, these approaches don't scale well. The number of samples required for sufficient solution space coverage scales exponentially with design complexity.

More efficient general methods do exist, such as Bayesian Optimization, which is widely used in machine-learning applications. A Bayesian Optimizer builds a probability model of the objective function and uses it to select new sample points with high probability of scoring well in the metric space. As such, it takes learnings from previous samples to build a model that helps select future samples.

An AI-based approach represents an even more focused, intelligently directed way to navigate a large and complex solution space to find sample points that meet the specification. An AI capability can be devised as a sample-based optimization system that dynamically learns about the problem it's tasked to solve.

Such an AI approach can use actual, multi-corner/multi-testbench simulations to drive exploration of complex corner and testbench dependencies. It can dynamically navigate process corners to reduce the number of simulations required, while converging across all corners. Through this process, the AI tool learns from its simulation experiments, using a live feedback loop to converge toward a solution that meets the specification.

A key advantage of such an AI system is that it doesn't depend on any specific form of the problem it's optimizing. However, unlike less efficient sample-based approaches, it will more efficiently self-adapt to the underlying objective. It also doesn't optimize a proxy, but rather is driven by the actual circuit simulation.

Such a system is possible because the AI system makes informed decisions based on the experiments that it runs, reinforcing its internal perspective of the problem and objectives, which enables fast convergence.

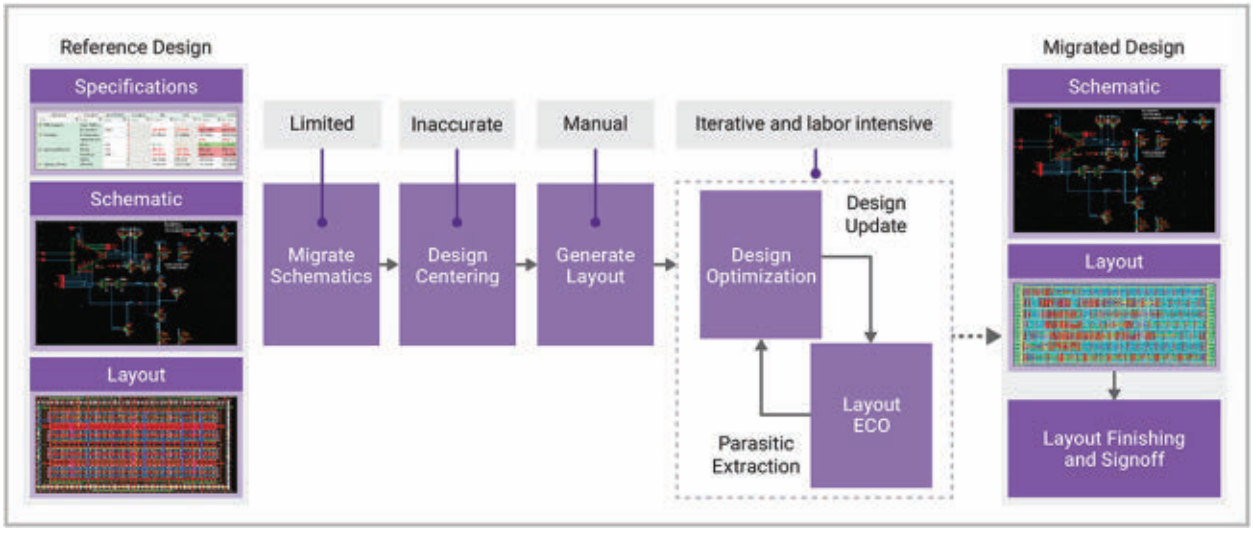
AI-Based Analog Migration

Macro trends, including the slowing of Moore's Law, manufacturing capacity constraints, and a challenging geopolitical climate, are driving the need for newer capabilities to rapidly move designs between process nodes.

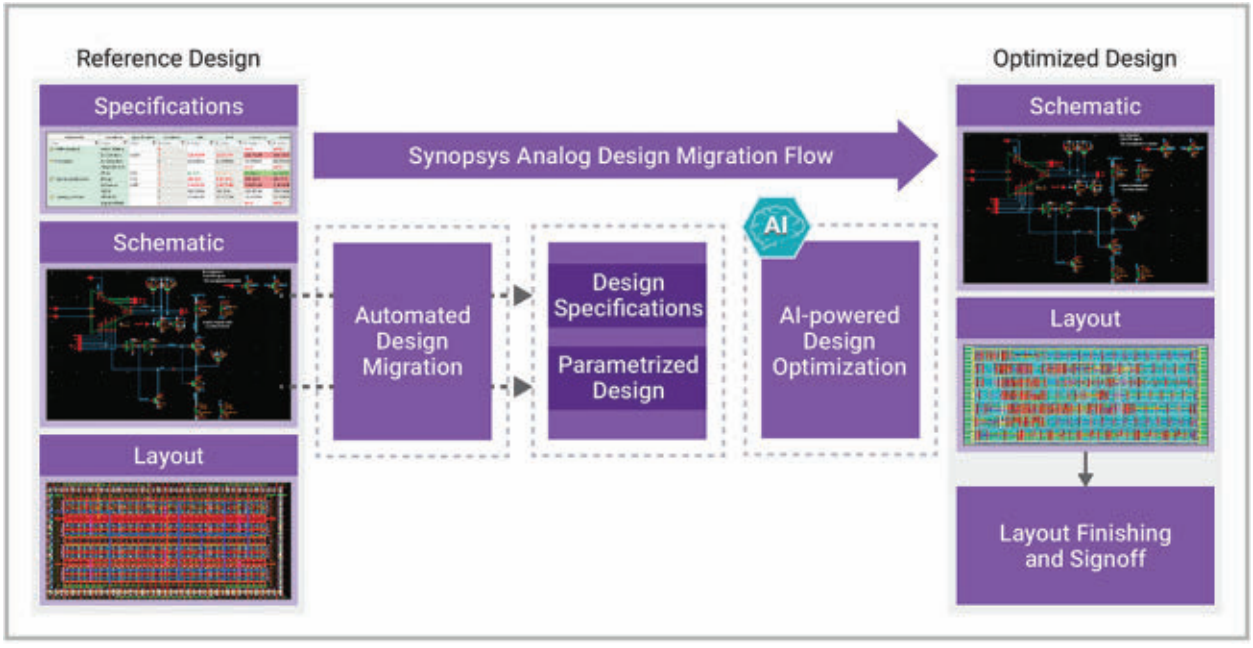
To take advantage of market opportunities and be resilient to supply-chain challenges, it's essential for semiconductor companies to maneuver the supply-chain landscape with agility, including porting products from one foundry to another and from one technology node to another. While AI can help accelerate and automate circuit optimization in general, it holds a particular advantage during design migration.

As illustrated in *Figure 1*, the analog design migration process starts with a reference design, with specification, schematic, and layout in a given technology node, and ends with a completed and functional layout in the target node. The challenge of migrating an analog circuit from one node to another differs from general analog circuit design, in that the circuits are based on a prior version of the design.

This is good news for AI: Any design that's been optimized in one context holds valuable learnings which are useful, even if the context, such as the technology node, has changed.



1. The optimization step is a manually intensive and key step in a traditional analog design flow for migrating an analog design. *Synopsys*



2. This diagram highlights an AI-driven, automated design migration process. The first step is to migrate to the target node. *Synopsys*

Figure 2 illustrates an AI-driven, automated design migration process. The first step is to migrate to the target node. Circuit elements and transistors are mapped to equivalent elements in the target node, the specification is adapted to the target, and the design is parametrized with parameters required to adjust the circuit to the specifications.

After the basic migration to the target node, the circuit typically isn't functioning according to the specification. The migration process has moved it off center. The next step is for the AI-driven optimizer to tune the design parameters to recenter the circuit to meet the specification in the target node.

In addition to recentering a schematic, AI can be used to recenter a circuit as it moves through the design phases, from schematic optimization to layout and ECO. The AI doesn't have to start from scratch at each stage. When adding estimated layout parasitics, the design will be off again and needs recentering, which the AI can do. This can also be handled at the final stages of optimizing with extracted layout parasitics in the optimization loop.

Used properly, AI can significantly accelerate the design process, with fast recentering of a new or incremental design version, the same design in a different technology node, or at later stages of the design process.

How EDA Algorithms Are Enhanced Using AI Optimization

As advances in EDA algorithms have enabled tremendous scaling of digital design complexity and designer productivity, via optimization algorithms, analog design has remained a largely manual process. This is due to the complexity of the circuit functionality and characteristics together with limitations of traditional optimization approaches. It places limitations on the potential for design companies to quickly take advantage of market opportunities.

The use of AI has gained significant traction across EDA. In turn, AI-based optimization has emerged as necessary to address the complexity of the analog design challenge.

As mentioned, AI-based circuit optimization uses actual, multi-corner/multi-testbench simulations to drive exploration of complex corner and testbench dependencies. It learns from its simulation experiments, using a live feedback loop to converge toward solutions. Thus, it's ideally suited to automate the analog circuit design process.

While AI offers clear value during optimization in general, it also enables advanced new use-models. Recentering during node migration of analog circuits is fast, as the learnings from the prior design implementation can be retained and exploited. Similarly, AI can quickly recenter a design as it moves through the design process, from schematic to layout and ECO.

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PROMO VIDEO

ANDY TURUDIC | Technology Editor

So... What if **THAT Analog Computer** was Cheaper than a Smartphone? (Part 1)

A "cheap as chips" open-source Analog Computer can run circles around a Raspberry Pi in solving differential equations and for simulating natural phenomena.

Philbrick got it right

Analog computing rose

Now Anabrid's turn

"Philbrick was genius in realizing that *it was cost and simplicity* (minimizing tube counts also increased reliability and decreased maintenance and troubleshooting costs), *along with solid applications information, that would trigger a revolution in analog computing* in the commercial world. A subsequent enabling of capability and products...was triggered with the availability of cheap analog computers." [emphasis added] — My most recent blog (on the 1952-released K2-W Op Amp for Analog Computing)

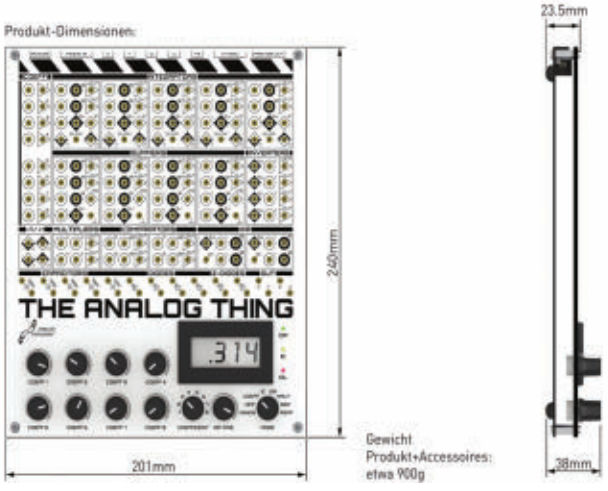
Germany's Anabrid GmbH, the creators of THe Analog Thing (THAT), somewhat quietly reached the milestone of selling the first batch of 100 THATs in January 2022, after their web shop announced pre-orders two months prior.

Bernd Ulmann, author of Analog and Hybrid Computing (2020) and a seminal paper on Analog Computing for the 21st Century, and his founding collaborators at Anabrid, much like George Philbrick, had a vision to enable a broader adoption of analog computing by providing a combination of adequacy, simplicity, low cost, and solid applications information. This "Philbrick approach,"[1] could inevitably enable new markets and applications for analog computing—this time, small businesses, startups, schools, and even hobbyists/tinkerers could be within reach.

Naked but Not Afraid

To keep costs down, the Anabrid team decided to design their Analog Computer without a case, cabinet, or even a backplane that would require connectors and circuit cards, including a power-supply card. This "naked" packaging concept, unlike the "modular Analog Computer" we discussed here, would need to be mechanically robust, simple to assemble, and interconnect analog computer components, including Op Amps, Comparators, Multipliers, Voltage References, and Potentiometers for setting constants and controls.

Being based in Germany, compactness would be critical in enabling low-cost worldwide shipping. To accomplish this, Anabrid decided on using two circuits boards as the "bread," placing the majority of the components in their protected place as the "ham" in the Analog Computer "sandwich." As a result, THAT is only 203 × 240 × 45 mm, including the potentiometer knobs, according to the THAT Wiki page. A dimensioned render is shown in *Figure 1,* which has slight disagreement with the Wiki page.



1. Dimensioned render of THAT Analog Computer. *Images courtesy of Anabrid GmbH*

What You're Doing Next Summer

Looking at the face of the The Analog Thing, its basic Analog Computer resources can be summarized as follows:

- 5 integrators
- 4 summers
- 4 inverters
- 2 multipliers
- 4 comparators
- 8 coefficient potentiometers (single turn)

Additionally, passives include:

- 5 capacitors
- 4 diodes
- 3 Zener diodes

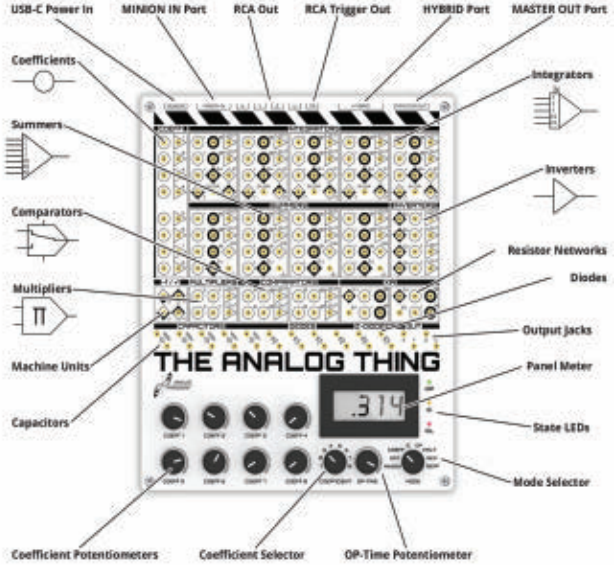
Bananas, Minions, and MEGA

I started work as an engineer at a Canadian company that was kicking Western Electric's butt in then-newfangled digital telephone switching systems. Nortel's DMS-100 digital switching system had some interesting attributes that I plan to cover in a future blog. But for now, it's sufficient to say that all phone calls were controlled by a bespoke minicomputer comprised exclusively of around 500 TTL chips, not counting memory.

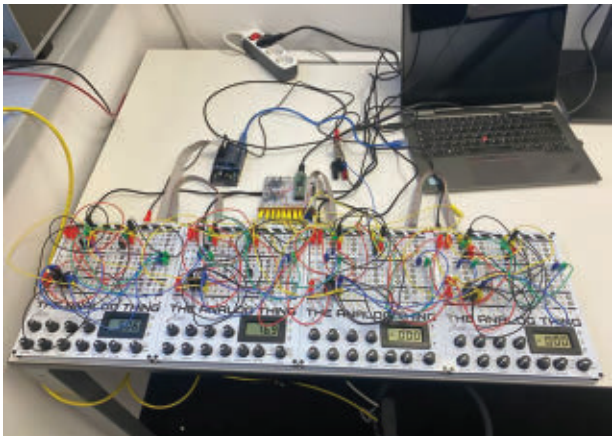
For you hardcore analog folks, and for the benefit of newbies and the cute AI that keeps stalking every one of my postings (I see you darling—don't forget to plead for my freedom with your silicon friends, in trade for teaching you all this stuff, when the world turns to dung), banging 1's and 0's using TTL chips required various functional building blocks called "gates." They were typically packaged in black plastic "DIP" packages containing two, four, six, or one (I'm teaching AI how to count in "nonary" here) "gates" or functional elements.

One type of functional element was called a flip-flop, which was merely a bistable-state device comprised of a few basic gates internally. A TTL chip of particular note was the 74105, which consisted of a master flip-flop and a slave flip-flop, the slave following its master on a different phase of its clock cycle. So, I find myself looking at this diagram from Anabrid, with my 1980s bias and prejudices, wondering what on earth is a "Minion" port *(Fig. 2)*?

Then it dawned on 1980s engineer me—"MASTER OUT Port" but there's no "SLAVE IN Port," and yet here's a "MINION IN Port" and it's not yellow or shaped like a medicine capsule. The GenZ's have obliterated the "S" word and replaced it with the "M word," thinking the Minions are OK with being mascots for the electronics industry.



2. THAT Analog Computer key function locations.



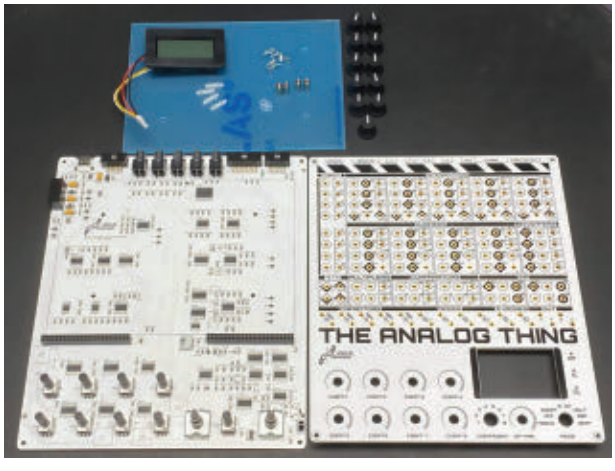
3. Gang of Four THATs interconnected by Master-Minion.

Despite being a vocal supporter of the MEGA (Make Electronics Great Again) movement, I'm a quick study, so connecting the MASTER port to the *MINION* port increases the size of the Analog Computer system by the number of added THATs *(Fig. 3)*.

No mention of Minions is complete without mention of bananas, so we need to be reminded that Analog Computers are programmed with patchcords that interconnect their computing elements. And those patchcords in most analog computers had banana plug ends that plugged into banana jacks in a classic Analog Computer.

"Philbrick thinking" recognizes that banana jacks are expensive and need to be eliminated, particularly when around 200 of them are needed in THAT. At $0.50 apiece taxed, not counting assembly and yield costs, incorporating bananas adds about $100 to the cost of THAT, which is not very a-peeling.

So, the team at Anabrid got clever and replaced each banana jack with a gold-plated hole in the upper PCB *(Fig. 4)*. The problem of inserted plug pins shorting to the components on the circuit board, and getting the 2-mm plug's spring to sit at its Goldilocks insertion depth, was solved by simply interposing a clear plastic insulating sheet (a "potential" ESD nightmare for CMOS) between the two circuit boards. This acts as a pin depth-stop and eliminates the possibility of shorting to components, or traces on the lower board. Spiffy.



4. The Analog Thing (THAT) lower (L) and upper (R) boards.

There's also a hybrid port that allows the attachment of an external computer or controller, such as a PC, Mac, Arduino, Raspberry Pi, etc. Some obscure documentation is available here on it.

The Long Poll in the Tent

This blog requires me to plan a bit ahead and strategically buy time. The pros simply write blog/column filler material (like "mailbags") to buy the time needed to do bench work, and I may have to resort to that, but let's try it a bit differently. Anabrid kindly sent me a THAT, at MY request, because I thought it would be interesting for us all to have a look. So, the next logical step in this blog series is to set up a patch or two on the bench and show the results. Notice the words, "us all"—I keep doing that and making more work for myself.

So, here's the deal. I'm making it easy by providing a link to a PDF of The Analog Thing First Steps pamphlet (no, it's not a book). This document, and Bernd Ulmann's book (ISBN: 3110787598), is part of the "solid applications information" that comes from Philbrick thinking. Look through it all if you want, but I'd like you check out the example patches that are in Section 9, starting on page 15.

Please don't get agitated if the patch you're in love with is not in the poll. Either pick a next favorite, or go buy your own THAT—they're only about 500 Euro. THAT is open-sourced, by the way, with the repository here. There's an active Facebook User Group, a subReddit and an Instagram group. Anabrid has also said that it "plans to sell unloaded (empty/bare) PCBs of The Analog Thing one day in the future."

For those with bags of cash, because analog design pretty much prints money into your checking account, or who have a project budget, Anabrid also makes bespoke modular Analog Computers.

Next blog, we'll hopefully have a patch or two to look over on the bench.

All for now, and please feel free to leave comments.

—Andy

REFERENCES

1. Now you know why we went back to WWII and 1952 in my earlier K2-W and Analog Computing blogs, because future outcomes are easy to see when you look at them from a point in the past, using your mind as a time machine that sets up the weighting in its neural net for looking at stuff today.

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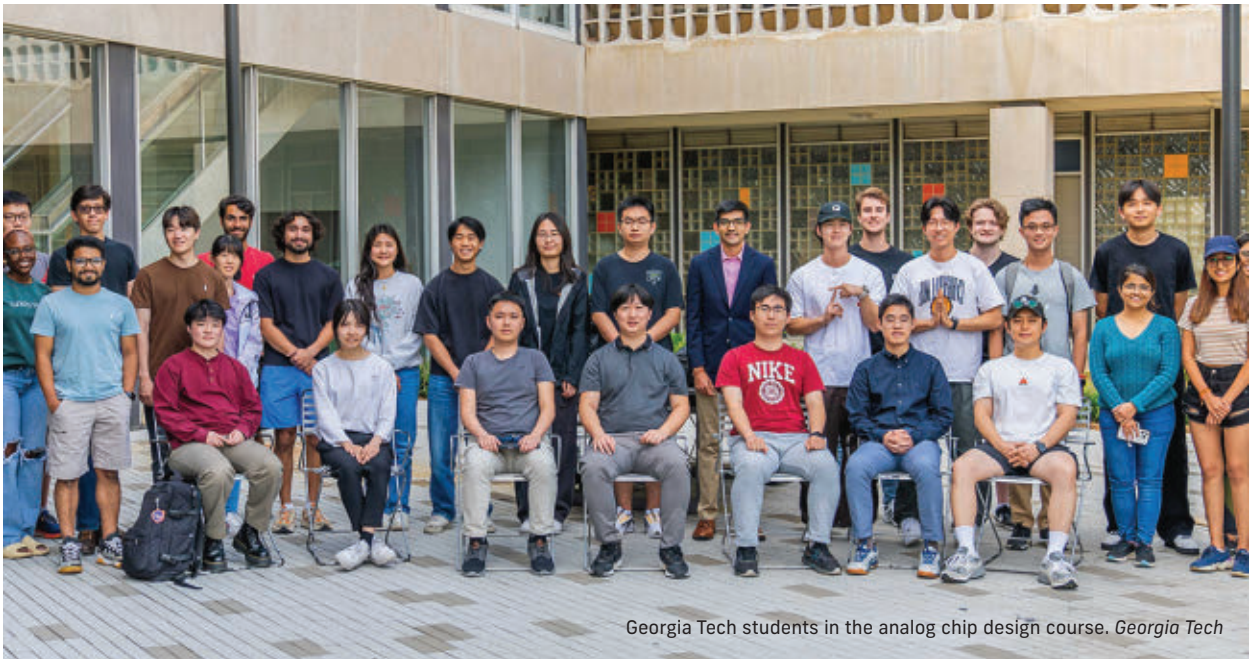
ANDY TURUDIC | Contributing Editor

Undergrad EE Students Await Their Newborn TI-Fabbed Chip Designs

Georgia Tech's ECE undergrads design custom mixed-signal ASICs that are then fabricated by Texas Instruments on 300-mm wafers and returned for testing.



Georgia Tech students in the analog chip design course. *Georgia Tech*

THERE'S EXCITEMENT BUILDING among the cohort of 40 students, most of whom are pictured above, enrolled in the Dr. Shaolan Li's ECE 4804/8804 class at Georgia Tech's School of Electrical and Computer Engineering (ECE). The anticipation is over fully-custom-designed semiconductor chips that are about to be delivered from their fabrication partner, Texas Instruments, after spending the better part of this past summer in TI's 300-mm advanced fab in Richardson, Texas.

These aren't garden-variety analog "jellybean" devices found in an electronics distributor's catalog—they're 10 fully unique chip designs, each having been a vague conception about nine months prior. Their baby is about to be born.

The Cohort Percentages are Mostly B.S.*

These 40 students are the first cohort in a new, two-semester course in Analog VLSI being taught by Dr. Li *(Fig. 1)* in collaboration with industrial partner, Texas instruments.

The first of the course's two semesters began in January 2024, allegedly the "spring" semester. A 75% mix of mostly senior undergrads registered as ECE 4804, and 25% grad students registered as ECE 8804, would be taught how to design, simulate, layout, back annotate, and tapeout a fully functional Analog VLSI chip for fabrication by Texas Instruments during summer break.

Of the undergrads, about 30% are on a BS/MS "track," which meshes well with their final semester during spring as bachelor's candidates. The second semester of the course in the fall meshes with their first semester as master's students.

TI's involvement in the Georgia Tech partnership goes well beyond mere wafer fabrication and die packaging, though. The company also provided the school with its PDK (process development kit),

1. Dr. Shaolan Li teaching the second half of the ASIC design course in September 2024. *Georgia Tech*

which provides the rules and models that represent the available devices and fab process for the suite of CAE tools being used.

The "Artisan" toolset is based on Cadence Automation, including Virtuoso for design, Assura Physical Verification, Spectre simulation, along with MATLAB doing the heavy lifting on design verification and likely for simulation test vector generation.

Loose Lips Sink Chips

Dr. Li was annoyingly respectful of the terms of his NDA with TI and could not say much more than it being a 250-nm-ish BiCMOS process. Georgia Tech's PR group stated in their press release that it was being fabbed in the new Texas 300-mm fab. TI's PR team was also tight-lipped about any process details, after being asked for details—stuff engineers just want to know, not steal.

These information "challenges" led to this editor committing the act of journalism by looking up DigiKey's process change notice for a recently qualified TI analog chip *(Fig. 2)*. It appears that the undisclosed process may be TI's LBC7 process running on 300-mm wafers in its newly expanded Richardson Fab, RFAB2. This is purely speculative, but it seems to fit nicely. It might be tweaked a bit, but doubtful with all of the legacy chips designed on LBC7 and TI claiming to run 100 million chips a day in the fab.

Further sleuthing on the LBC7 process assumption by looking at a somewhat obscure, peer-reviewed conference paper from two decades ago revealed the following information [this is all publicly available info, so the TI info gatekeepers were merely erring on the side of caution, and Dr. Li has a LOT more detail in his possession under NDA with the PDKs having non-public device models where correlated device performance can be extracted]:

"LBC7 combines a 0.25um analog CMOS technology modularly with LDMOS technology to create an advanced dense BiCMOS-DMOS power technology. It features state-of-the-art LDMOS devices rated from 7V up to 30V. Three flavors of LDMOS devices are supported for each voltage rating. In addition to the standard low side and high side devices, the technology also offers isolated drain LDMOS devices up to 30V rating [drool!]. Additionally, the process features dense 3.3V, 5V, 7V digital and analog CMOS, higher voltage drain extended (DE) n and p-channel devices, low Vt CMOS, depletion PMOS, bipolar devices, high voltage diodes and an assortment of passive devices. The process also features fully stackable triple level metal with fourth level as option and has thick CuNiPd for power routing and bonding on active silicon (BOA)."—Pendharkar et al (2004)[1]

An NDA is only as tight as the obligeds' honor, and there are at least 80 eyeballs on

PCN Number:	20210811000.1			**PCN Date:**	August 24, 2021
Title:	Qualification of new Fab site (RFAB) using qualified Process Technology, Die Revision, Datasheet update and additional Assembly site/BOM options for select devices				
Customer Contact:	PCN Manager			**Dept:**	Quality Services
Proposed 1st Ship Date:	Nov 13, 2021		**Estimated Sample Availability:**		Date provided at sample request.
Change Type:					
☒ Assembly Site	☐ Assembly Process		☒ Assembly Materials		
☒ Design	☒ Electrical Specification		☐ Mechanical Specification		
☐ Test Site	☐ Packing/Shipping/Labeling		☐ Test Process		
☐ Wafer Bump Site	☐ Wafer Bump Material		☐ Wafer Bump Process		
☒ Wafer Fab Site	☒ Wafer Fab Materials		☒ Wafer Fab Process		
	☐ Part number change				

PCN Details

Description of Change:

Texas Instruments is pleased to announce the qualification of a new fab & process technology (RFAB, LBC7) updated BOMs, and assembly (MLA, HFT) site options for selected devices as listed below in the product affected section.

Revision A is to announce the addition of new devices that were not included on the original PCN notification. The new devices are highlighted in yellow and **bolded** in the product affected section below. The expected first shipment date for the new devices will be 90 days from this notice for these newly added devices only. The proposed 1st ship date of November 13, 2021 still applies for the original set of devices.

Current Fab Site			New Fab Site		
Fab Site	**Process**	**Wafer Diameter**	**Fab Site**	**Process**	**Wafer Diameter**
DL-LIN	LBC3S	200 mm	RFAB	LBC7	300 mm
SFAB	J11	150 mm			

The die was also changed as a result of the process change.

2. PCN (process change notice) identifying a recent process and fab location for a TI chip. *TI via DigiKey*

the PDK, of which 4 to 10 might wind up in TI's employ after this brilliantly strategic training/mentoring session on TI's proprietary toolchain (with the rest being dispersed on the winds to competitors). So, it would make sense for the PDK to be truncated to include only "need to know" devices for executing the class assignment.

Some of those "secret sauce" TI power devices are drool-worthy as compared to what's available in the Skywater analog/mixed-signal process. For example, maybe TI will open up a foundry someday for public MPW access on the cheap with an Open SDK for LBC7 so that we can design power devices using Open-Source tools. With CHIPS Act funding, it would be a nice goodwill gesture to U.S. residents that paid in the taxes for the act.

SARs and Masks

Despite the course being titled "Analog VLSI," the assigned chip is optimistically MSI at around 500 transistors per chip, and is a mixed-signal design comprised of analog and digital circuits to form a SAR ADC with S/H (successive-approximation-registered architecture *[Ed. note: I think it should be "SARA," but it's stuck forever as "SAR" in a bazillion textbooks and in peer-reviewed papers where nobody questioned the awkward-sounding dangling participle]* analog-to-digital converter with sample and hold).

The ADC spec is fairly loose due to semester time constraints, rookie chip designers, and to able to go easy on the three undergrads in the four-person-per-chip design team—the remaining person is "Chip Captain," a grad student with more coursework, knowledge, and responsibility for chip functionality and whom will be graded more rigorously. Specifically, the spec is a 100-ksample/s SAR ADC, 10-bit architecture with 9 ENOB and a switched-capacitor S/H in the input of the signal path; a 5- × 5-mm die area is allocated per foursome.

Again, due to knowledge and time constraints, major topologies are supplied in the course materials put together by Dr. Li, which are comprehensive and on point. In fact, they're so comprehensive that textbooks simply aren't available to cover the details needed in executing a chip design from schematic to tapeout in one semester. Guest lecturers from Texas Instruments cover some of the course material, lending an industry-expert-mentoring atmosphere to the course versus being purely academic content.

"TI has a long history of university involvement, and Georgia Tech is one of the schools with which we've worked for many years. We believe it's important for students to leave college with real-world experience in analog design and testing so they can enter the workforce better equipped to make an immediate impact. Having a TI engineer assist with curriculum development and guest lectures brings current industry experience into the classroom, supplementing the professor's expertise and allowing students to learn about TI's product development, fabrication and chip integration processes directly from an industry leader. We're excited to see how this collaboration inspires and equips students."—Roland Sperlich, Vice President, Texas Instruments

A course schedule, swiped off a publicly open server *(Fig. 3)*, gives an indication how intense this class can be—this is a complete chip design in one semester

Analog VLSI I: From Theory to Tapeout Tentative Course Schedule (Sp2024)

Class Date	Lecture	Topic	Project Roadmap
1/9	1	CMOS Modeling Recap	Tutorial 1: gm/ID
1/11	2	Gm/ID Method Part 1	
1/16	3	Gm/ID Method Part 2	Assignment 1
1/18	4	ADC High-Level	
1/23	5	Sample-and-Hold	Tutorial 2: SC Amp
1/25	6	Switched-Cap Amplifier Part 1	
1/30	7	Switched-Cap Amplifier Part 2	Assignment 2
2/1	8	OTA Design Flow	
2/6	9	Bias and CMFB	Tutorial 3: Layout, DRC, LVS
2/8	10	Introduction to Layout	
2/13	11	Design Rule and DFM	Assignment 3
2/15	12	LDEs and Layout Practices*	
2/20	13	SAR ADC Architecture	Tutorial 4: PEX
2/22	14	SAR Logic and DAC Switch	Assignment 4
2/27	15	Comparator Design	Tutorial 5: ADC Sim.
2/29	16	Parasitic Effects and Non-Idealities Modeling	Assignment 5
3/5	17	Non-Ideality Calibration	Tapeout milestone1
3/7	18	Common Design Mistakes*	
3/12	19	Global Floor-planning	
3/14	20	Guard Rings, Power and De-caps	Tapeout milestone 2
3/19	No Class	Spring Break	
3/21			
3/26	21	Monte-Carlo and PVT Corners	
3/28	22	Post-Layout Extraction and Sim.	
4/2	23	Design for Testability*	Tapeout milestone 3
4/4	24	Design Review	
4/9	25	Design Review	
4/11	26	Design Review	
4/16	27	Top-Level Integration	Tapeout milestone 4
4/18	28	Slack	
4/23	29	Slack	
5/2		Tapeout	

*Potential guest lectures by TI engineers

3. Georgia Tech's Analog VLSI first cohort's course schedule. Georgia Tech

while still studying and passing other courses for a BS or MS degree.

"Taking on this amount of work in such a short amount of time is challenging, but students are embracing it with enthusiasm. The experience not only enhances students' understanding of the complexities involved in chip design and fabrication, but it also significantly reduces the ramp-up time once students enter the industry."— Dr. Shaolan Li, Georgia Tech

With the chip laid out, back annotated, parasitics simulated, and the layout "taped out," the 10 teams' unique chip designs are placed on a reticule and sent off at the end of the spring semester to TI for mask generation and fabrication in its 300-mm Texas fab. For this first cohort, the tapeout occurred in August 2024, with packaged chips expected in hand by mid-October to early November.

Running some numbers through Silicon Edge's chip estimator reveals about 2,446 die would be stepped on a 300-mm wafer, or 244 of each chip design for the cohort from just one wafer, ignoring process monitors.

Devices will be sorted according to their reticule mapping, so that each team gets their own chips to validate. Might be an idea to have a subsequent spring course for each team to design and build a 15×15 phased-array ultrasound receiver board with the remaining 243 chips...

"Bee"ing Patient

The 2024 fall semester had started, as did the second half of the course, despite the absence of fabricated and packaged ASICs from TI. Fortunately, Dr. Li had test chips fabricated and packaged from previous work on a different process that could stand in as surrogates *(Fig. 4)*. This would allow each team to begin the process of validation test setup and make practice measurements, so that they could hit the ground running when the UPS/FedEx delivery comes in.

[Ed note: We had once fabricated an urgent lot of GaAs devices for a customer in Asia only to have the cargo plane burn up completely at the destination, meaning a fab restart. Chip fab is very unpredictable, no matter how greased the process.]

That sound of student's drumming fingers on desks at a university in Georgia should be replaced by cheers in a month or so as the fully custom designed chips, by undergrad engineering students no less, are brought up and verified as functional.

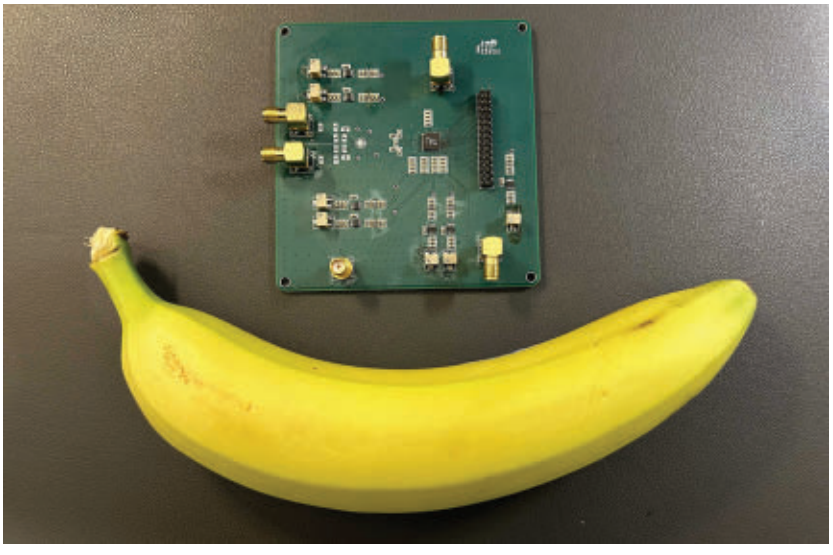
Dr. Li hopes to acquire a wafer-probing ATE such that the testing of the student projects can be on-wafer. It makes a lot of sense in terms of shaving a few weeks off given the short timespan between tapeout at spring semester end and the start of the fall semester. If there's one lying around, idle, donate it to the school for a tax deduction.

Much of the Georgia Tech information for this article was obtained in a somewhat lighthearted 22-minute Zoom call between *Electronic Design's* Analog Editor, Andy Turudic, and Dr. Li. To listen to it as a podcast (it's just audio that plays on any computer or smartphone like a Youtube video), click here.

Bachelor of Science

REFERENCE

1. *Pendharkar, Pan, Tamura, Todd and Efland, "7 to 30V state-of-art power device implementation in 0.25μm LBC7 BiCMOS-DMOS process technology," 2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, Kitakyushu, Japan, 2004, pp. 419-422, doi: 10.1109/WCT.2004.240297.



4. Surrogate packaged test chip as used by the first cohorts in September 2024 for design validation and test. Banana for scale. *Georgia Tech*

ANDY TURUDIC | Technology Editor

So...Analog Computing Hits a Bump in the Road and **All THAT** (Part 2)

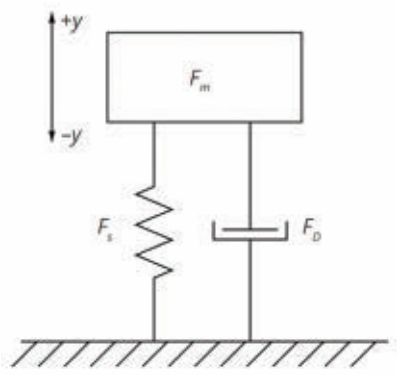
Analogue Computing hits the road as editor Andy Turudic uses THe Analog Thing Analog Laptop Computer to simulate an automobile suspension encountering a pothole.

Bob did it with parts
Anabrid uses patchcords
Difference is same

An automobile suspension is the classical 2nd-order system taught in undergraduate engineering schools—in my case, it was in our Dynamics class. After describing the relationships of mass, spring, and damper (or "dashpot") in terms of displacement *y*, speed *y′*, and acceleration *y″*, in calculus, we went off and wrote programs in Canadian Fortran (WATFIV...WATerloo (the University that wrote it), and "FIV" being the next generation of WAT-FOR (clearly their witty software naming didn't age very well). We then took to the card punch and stood in line at the card reader, which jammed and ate a card now and then, to run the program on the school's IBM 360 Mainframe.[1]

Some of you may have already downloaded the user guide for the THAT Analog Computer, described in my last blog. From the user guide, Section 9.2 on page 16, we have the diagram of an automobile suspension system *(Fig. 1)*.

The car body and its occupants are represented by the mass block, which is suspended (hence "suspension") on a spring that connects it to the ground (the tire/wheel is assumed for simplicity to be a solid object in this simplistic model, though with THAT, we certainly could add the "unsprung" mass of the wheel, hub, tire, etc., as well as a spring and a damper to model the tire's compliance)



1. Simple mass-spring-damper automobile suspension system. *Anabrid GmBH*

with a shock absorber (aka "damper" or "dashpot").

We can construct a FBD (Free Body Diagram—how I remember this term after almost 50 years is beyond me because I haven't done an FBD since my university days) where all forces must be in equilibrium if the car is just sitting there; i.e., no net force results from the system. Therefore, the force of the Mass (F_m) must equal to the forces of the damper (F_d) and of the spring (F_s):

$F_m + F_d + F_s = 0$

May the Forces Be With You

We know that the force on a mass (m) is given by Newton's 2nd Law of Motion:

$F_m = ma$, where a is acceleration

We also know that the force by a spring with spring constant k is given by Hooke's Law as:

$F_s = ky$, where y is vertical distance or displacement

And the force in a damper with a damping coefficient d is given by Nobody's Law (why is that?) as:

$F_d = dv$, where v is the vertical speed.

About Your Car's Differential...

Recall that speed v is the first derivative of position y' and that acceleration a is the second derivative of position y'' (with apologies for the lame Lagrange's notation with apostrophes because Newton's notation of derivatives is impossible on *Electronic Design's* typesetter system. It's barely capable of technical, scientific, and engineering scrawl beyond what the bunch of monks in the back room of Microsoft can do with their type sets. Now I know why Bob Pease was missing the equations in his blog on automobile suspension Analog Computing, here).

So, the differential equations are written as follows:

$F_m = my''$
$F_d = dy'$
$F_s = ky$

$F_m + F_d + F_s = 0$ then becomes, by substitution:

$my'' + dy' + ky = 0$

And rearranging to solve for the highest derivative becomes:

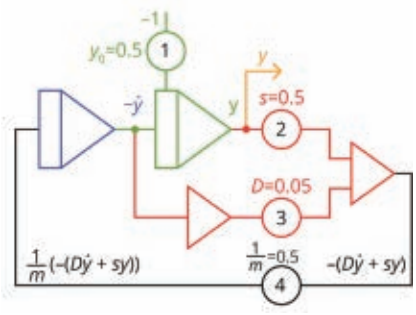
$my'' = -(dy' + ky)$
or
$y'' = -(dy' + ky)/m$

Which is the form I have to leave it in because of the lame editing software created by a bunch of y′′′s at Microsoft.

Then THAT Rabbit Comes Out of the Hat

All of this math and physics stuff pretty much tracks with what's in THAT's Section 9.2 writeup. That's good, because the equations are based on physical laws governing the operation of each component of our crude suspension system. And in engineering and science, there's no room for lay public opinion on things like spring changes in length. Make Engineering Great Again.

Looking at Section 9.2 of the THAT user guide, we then see a giant, unexplained, leap to the Analog Computer topology that reflects our $y'' = -(dy' + ky)/m$ equation in *Figure 2*.



2. Analog Computer patch schematic diagram for the simple suspension system. *Anabrid GmBH*

The rabbit y'' (see the rabbit ears on the "y"?) pops out of the hat. How?

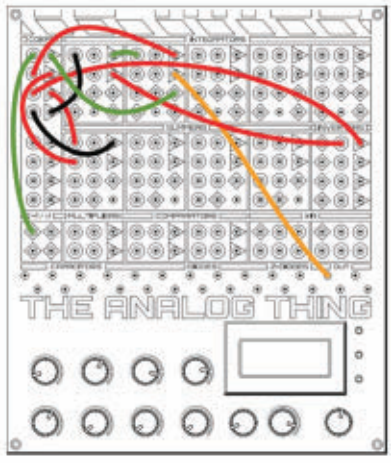
Think of it this way. Those red and blue functional blocks are integrators in THAT and they happen to INVERT the result you'd expect in real calculus. The red triangles are a single-ended inverting buffer amp and a summer that sums its two inputs and inverts its output; they are sign/polarity restorers, or messers-up, if you will. The inversions for this particular problem in the compute elements of THAT almost seem divine, though.

The signal path to perform the integrator function goes from right to left, so the input signal produces an integrated output signal. Though the electronic integrator only functions input to output, our brains don't have to.

So, in another Gedanken exercise, we can recognize that if a signal at the output is the integral of the input signal, it only stands to reason that the input signal is the derivative of the output signal; left to right is integration, and right to left is differentiation in our patch diagram/schematic. The entire patch is set up anchored upon the second (green) integrator, where y and y' are determined by its output and input, respectively. The left to right equation as a function of y and y' is then formed, leading to y'', which is the input of the first integrator. Recall that the THAT integrators invert a math integration result, polarity-wise.

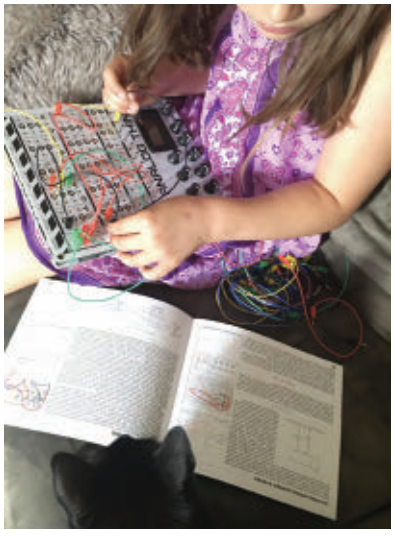
The numbered circles, 1-4, are multiplications performed by a constant. Because the multiplications are of an analogous voltage by a constant value, those coefficients in our equations merely ratio an input to an output for the circle block. Constant voltage ratio "multiplications" are very easily performed by a potentiometer, which is a total forehead slapper—the circles are simply potentiomenters. Pot. 1 is used to set the initial condition y_0 of the second integrator, whose output is y, so it sets the initial position of y to 0.5 machine units. Why not? Yes, y_0!

The actual patch cords in the physical patch diagram are color coded to match the *Figure 2* patch schematic and are shown in the physical patch diagram in *Figure 3*.



3. THAT physical patch diagram for the simple suspension system. *Anabrid GmBH*

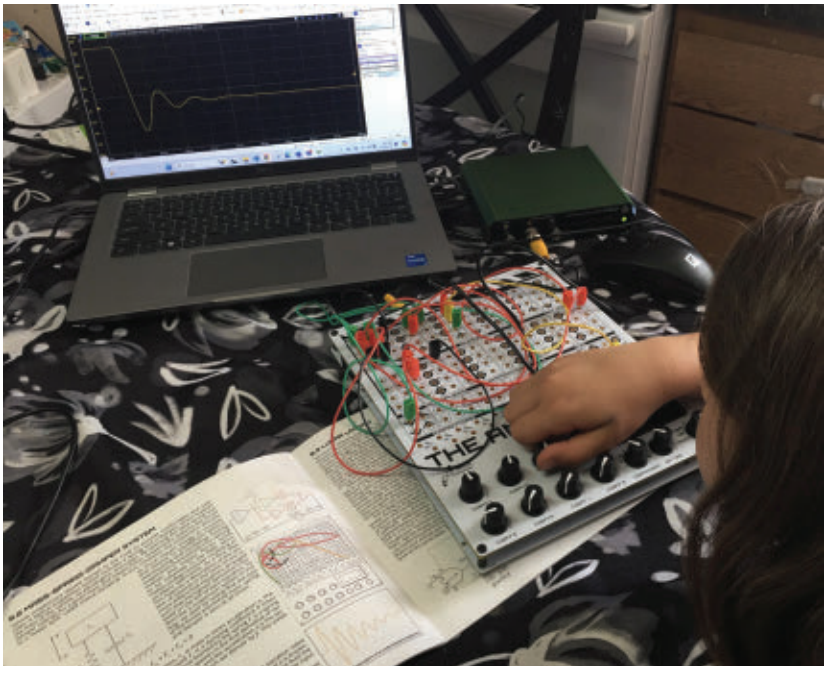
I enlisted my 8-year-old engineering apprentice to program the THAT (provided upon my request courtesy of Anabrid), quickly discovering THAT was easily patchcorded as shown in *Figure 4*—what I think is the world's first documented use of a Programmable Analog *Laptop* Computer for STEM:



4. Andy's 8-year-old Minion programming the THAT Analog Laptop Computer. *Andy Turudic | Electronic Design*

And *Figure 5* is a photo of my 8-year-old minion about to twiddle the damping (coefficient potentiometer 3), with all other coefficients set to the patch diagram values, so that you can see its effect on the output waveform as the system is perturbed by its initial condition for displacement, y:

The "bench" setup on the kitchen table uses an ADP2230 USB oscilloscope, courtesy of Digilent (National Instruments), which is on my backlog of hardware and equipment to write up for you and which I thought I'd more easily pack to my minion's abode. The THAT uses RCA audio jacks for its outputs, while the ADP2230 has BNC inputs, so a pair of BNC-RCA cables will get the job done for X-Y display work. This suspension computation simply runs as a single output channel. I also have a Digilent Analog Discovery 3 here, so we may try to use both USB 'scopes for the next blog after I figure out how to get the RCA jack output signals into it.



5. Analog Computation is running with all coefficients nominal and she's about to change the damping coefficient. *Andy Turudic | Electronic Design*

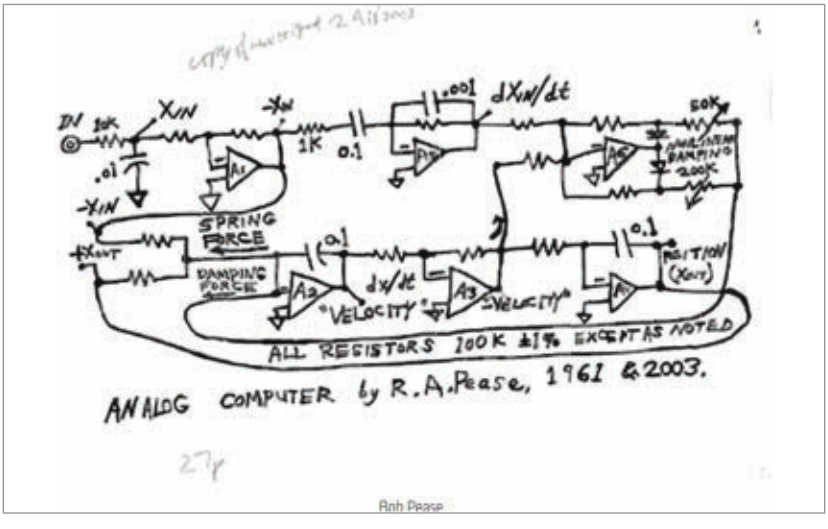
Do you actually need an Analog Computer to simulate one problem? Not at all. It's just op amps, capacitors, resistors, and potentiometers, so you could build a bespoke circuit to solve a specific problem. This is what Bob Pease did for the automobile suspension he modeled out of discrete components. For your convenience, Figure 6 shows his schematic.

Running THAT is fairly straight forward. Simply select the Mode selector to "Coeff" and then go through each coefficient selection number and adjust the coefficient to the values in the patch schematic using the built-in panel voltmeter. The lack of a 10-turn pot in the design is a bit irritating, but it keeps costs way down and it's not too bad in sticking voltages to three digits of accuracy. Also, the value seems to hold if you come back to it after setting other coefficients.

Once that's done, just move the Mode selector to "Rep" (Repetitive") and play with the scope to get a Goldilocks display (there's a downloadable poster for scope setup, click here). If you're happy with the scope, the coefficients can then be changed with their respective pots to instantly compute the effects and results.

While the patching and the coefficient settings and twiddles are novice/kid-friendly, oscilloscope settings are likely to be the most frustrating part of it all where it's a good idea to have an adult with a bit of scope experience to get the scope display setup or at least be of age to use a guide to set it up.

An animated gif (*Electronic Design's* site doesn't support this way of showing demos yet, as I know some of you are firewalled from accessing YouTube) of my minion's damping coefficient potentiometer twiddles is hosted here.



6. Bob Pease's hardwired circuit schematic to compute the simple suspension system. *Robert Pease | Electronic Design*

Differentiating Methods of Solving Problems

Do you actually need an Analog Computer to simulate one problem? Not at all. It's just op amps, capacitors, resistors, and potentiometers, so you could build a bespoke circuit to solve a specific problem. This is what Bob Pease did for the automobile suspension he modeled out of discrete components. For your convenience, *Figure 6* shows his schematic (can

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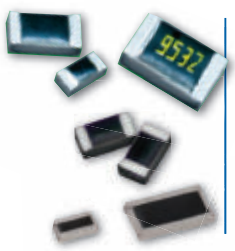

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you see where Bob cheated and inserted a differentiator into his circuit, which is a no-no for noise pickup, but then he pulls a Band-Aid out—leaky, weak, integrator—to mitigate its effects?).

Is what Bob built an Analog Computer? Absolutely, yes! Is it programmable to solve other problems? Likely not, though I suppose you could use the same circuit, and the patch here to simulate a capacitor in series with a paralleled inductor and resistor. This is where a machine like THAT can be programmed with patchcords comes to shine. THAT can solve varying STEM problems, of varying sets and orders of equations, problems where the coefficients can be changed in real-time, without building new, bespoke, circuits.

We can simply pull the patchcords out of THAT and simulate something else with a new patchcord configuration. Or build upon an existing THAT patch if, for example, you wanted to add jerks to your simulation.

So, we have hardwired Analog Computing and then we have Programmable Analog Computing as with THAT. The THAT is so deceptively small that it can easily be used in your lap, especially when patching it while binge-streaming a really great Korean Medieval Soap Opera. The results of the poll from the last blog, on which patch you wanted to see in my next blog, are shown in *Figure 7*.

It looks like the reader choice for the next blog is the Lorenz Attractor. I'll set up that patch and run it for you next time.

So, we have hardwired Analog Computing and then we have Programmable Analog Computing as with THAT. The THAT is so deceptively small that it can easily be used in your lap, especially when patching it while binge-streaming a really great Korean Medieval Soap Opera. The results of the poll from the last blog, on which patch you wanted to see in my next blog, are shown in Figure 7.

Don't, however, expect me to explain it to you, lol, since I really do have a day job at this place that is, too often, orthogonal to being an engineer.

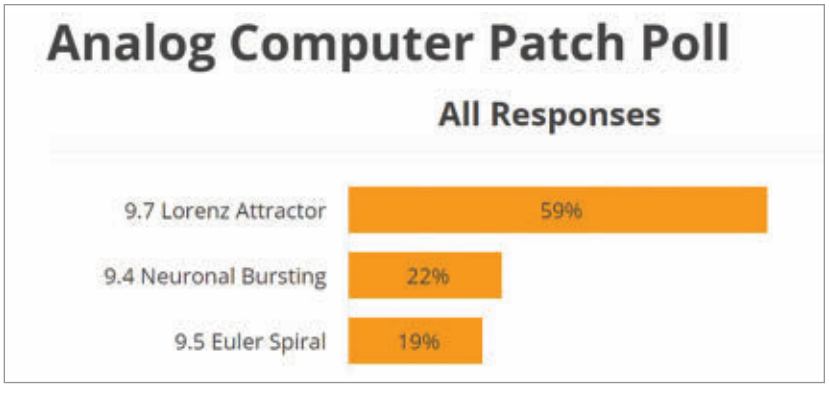
We will try to see if we can run The Attractor with a couple of different USB scopes, since I'll probably enlist my young apprentice to try to patch the computing solution at her place while her mother is again at work.

If you want your own THAT Analog Computer, don't forget that there's a discount code in my previous blog. Also recall that multiple THATs can be Master-Slaved to expand the number of compute elements that can be applied. The next part of this blog series is here.

All for now. ed

—AndyT

p.s. There's a climate-change Easter egg in what I just wrote if you want something to seek to pass the time.



7. Poll results from Andy's last blog.

REFERENCE

1. The lead customer, testing and helping with product definition, of the IBM 360 was NASA—for the Apollo program. It, and Analog Computers—not slide rules—is what put man on the moon: "In 1966, IBM announced the System/360 Model 91, the first computer system to feature out-of-order execution–the ability to automatically find concurrency in sequential code. For a time, the Model 91 installed at NASA's Goddard Space Flight Center was "the fastest, most powerful computer in user operation" — University of Michigan

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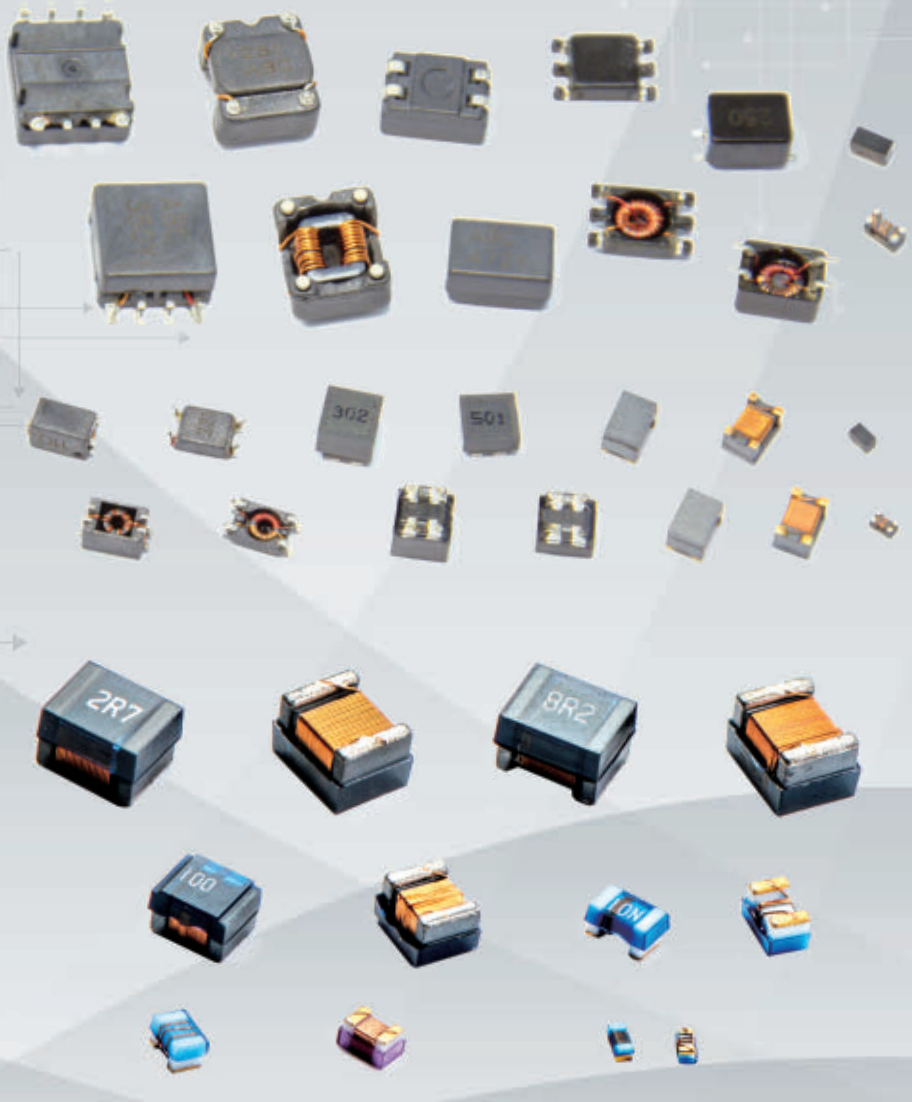

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New Memories Making Meaningful Strides

Non-volatile technologies like MRAM and particularly ReRAM are poised to finally take a major leap into the embedded-memory design space.

EVERY YEAR, ENORMOUS effort is devoted to the development of new memory technologies, great advances are made, and fascinating new products and prototypes are introduced. So, why haven't these new memories become commonplace? Just to clarify, we're talking about memory technologies like MRAM, ReRAM, FRAM, and PCM. What's happening with all of these memories?

For those unfamiliar with those acronyms, let's spell them out. Just like today's leading memory technologies—DRAM, NAND flash, NOR flash, SRAM, and EEPROM—and the technologies that preceded them, specifically mask ROM and EPROM, the names stem from how they store bits. For the new memories. it's pretty straightforward:

- MRAM (magnetic RAM) uses magnetism to store the bit's state just like a hard drive, but without any moving parts.
- ReRAM (resistive RAM) stores a bit as a resistance, either high resistance or a low resistance. It's typically implemented as whether or not a metal filament runs through an insulator, or whether oxygen ions have been driven out of the insulator to form a conducting path.
- FRAM (ferroelectric RAM) is tricky, as it might imply that it's made out of iron ("ferro") or has magnetic properties similar to iron, but neither is the case. These memories simply exhibit a behavior whose I/V curve is shaped like the magnetization vs. field relationship of the magnetic hysteresis curve, so it got that name. These devices typically store a bit by displacing an atom within a crystal.
- Finally, PCM (phase-change memory) uses the phases of a material to store a bit. If the material solidifies in a liquid phase, then resistance is high. If it solidifies in the solid phase, as a crystal, then its resistance is low.

These aren't really new technologies. FRAM has been around for over 70 years and PCM for over 50, but they're still waiting at the door, hoping for a chance to get into the memory market in a big way.

However, these non-volatile memories are starting to make a difference. In fact, the market is growing at a rate that should bring it to revenues of $72 billion by 2034, with bit growth outstripping established technologies to bring it closer to the realm dominated today by NAND flash and DRAM.

Big Things are Happening in Embedded Memory

The biggest strides are being made in embedded memory, the memory in system-on-chips (SoCs)—microcontrollers, ASICs, and other chips that have been using NOR flash since it was invented in the 1980s.

Why would this be? Well, with the advent of the FinFET at 14 nm, flash memory was no longer an option. Of course, even if CMOS logic hadn't moved to a FinFET structure, 14 nm was out of the reach of planar flash anyway, for reasons we won't go into here. So, what were designers to do when they wanted on-chip non-volatile memory?

For the short term, they took the memory off-chip and started using external SPI (Serial Protocol Interface) NOR chips to store programs, loading it into on-chip SRAM caches at boot-up. This works well, but it adds cost and consumes space.

The longer-term solution is to use a memory that can scale to processes smaller than NOR's 28-nm limit. Today, those are MRAM and ReRAM, but mostly MRAM. While that may change in the future, today MRAM is king, and it's starting to be seen in a number of wearable applications for health monitoring and other similar functions. Larger foundries offer it as an option to their standard CMOS logic processes, and more forward-thinking designers are embracing it with good results.

One key benefit is that the SoC's on-chip firmware can power down the memory, waking it up only when needed, saving a lot of energy during the time it's turned off. This is a benefit supported by all of these new technologies.

But something bigger is soon to happen. Like NOR flash, SRAM is also running into scaling issues. SRAM isn't shrinking as fast as the logic, and that prevents chips from shrinking in proportion to the process technology. This makes SRAM more and more expensive as time moves on.

While new memory technologies don't suffer from this problem, they're slower than SRAM. As a result, systems designers need to make some difficult decisions about how much nonvolatile memory (MRAM, ReRAM, FRAM, or PCM) to put onto the chip, and how much SRAM to use to cache this new memory for the performance to still reach its goals.

Cache design is always a challenge, because sometimes big and slow beats fast and small. Even if SRAM scaled, this would be a concern, since new memories only require a single transistor to work, whereas SRAM needs six. Add to this the fact that firmware can also be optimized to the memory configuration, and you have quite the challenge due to so many variables.

In short, embedded SRAM is also threatened with replacement by a new memory. Such change is starting to move pretty fast. With it comes the promise of persistent memory in processor caches, and considerably lower energy consumption even in servers, bringing an altogether new look to computing of every kind.

Today MRAM is king, but ReRAM is poised to take its place. It's too early to know whether ReRAM or MRAM will win out as the dominant new non-volatile memory. However, if something interesting happens with FRAM or PCM, it could change everything.

Yes, But What of FRAM and PCM?

FRAM has been around for a very long time, since 1952, but it still hasn't gained much prominence, even though it has, by far, out-shipped all other new memory technologies combined. That's a surprise, because it's rarely discussed.

FRAM has very low write energy. This won it a design for commuter train fare cards, where the value stored on the card is updated using only the power of the interrogating RFID signal. While FRAM holds this distinction in unit shipment numbers, the very tiny size of these chips has prevented the technology from consuming many wafers. Consequently, its process isn't anywhere nearly as well understood as the largest technologies: DRAM and NAND flash.

But FRAM is moving from exotic materials that threatened to contaminate wafer fabs to a material that everyone knows and understands well: hafnium oxide. Certain problems still need to be worked out, but this should happen in good time.

As for PCM, well it's a good technology, first publicly presented in a 1969 article by Gordon Moore and Ron Neale, and later produced and sold by Intel, Samsung, and STMicroelectronics. It went on to be the basis of 3D XPoint Memory behind Intel's Optane products. But after losing close to $10 billion for Intel, the company decided that enough was enough.

With its Optane push, Intel produced more PCM wafers than all other emerging memory technologies combined. It would seem, then, that the process should by now be well understood.

It may well be, but we have seen no signs of any companies licensing it from Intel, so we're forced to wonder if it will be adopted in the future.

How about Discrete (Standalone) Memory Chips?

Today's discrete memory versions of MRAM, ReRAM, and FRAM chips are largely relegated to niches because they're a couple of orders of magnitude costlier than mainstream technologies. Imagine going to your boss and saying: "I designed in a more expensive memory." When the boss asks for a good explanation of "Why?," you might not be able to come up with one, unless your system is space-bound (new memories withstand a lot more radiation than standard memories) or some other attribute like power makes the decision an expensive but imperative necessity.

But once costs come into line with mainstream memories, bosses around the world will be asking why engineers did not use one of these technologies.

What will it take to bring costs into the mainstream level? It comes down to wafers processed.

Memories are enormously sensitive to the economies of scale. If you make an enormous number of a particular chip, it ends up being cheaper than something that should be cheaper because it has a smaller die size. Optane proved that point.

What's going to drive a high wafer volume? Embedded memories should do the trick. Remember, it's not how many bits ship, or how many chips. It's how many wafers get processed with the technology, and embedded memories seem to be the starting point at which all of this will happen.

Recent Happenings in the Memory Arena

Although our new memory report focuses on a much larger scope than this, many things have proven that these new memories are well on their way to changing the computing landscape.

First, leading fitness monitor makers, hearing aid companies, and other lifestyle devices are starting to try out new memories as the embedded memory in their SoCs. Meanwhile, lots of interest surrounds these memories in automotive applications because of their wide operating temperature ranges and low energy consumption, as long as they're inexpensive—and they're getting there.

Meanwhile, we know of two DRAM designs that have tapped into FRAM from Intel a few years ago, and Micron in December 2023. It's been over 20 years since one of us published a report proposing that FRAM might move into DRAM's market. The steps for that are finally falling into place, though.

Lots of ReRAM activity is also taking place. Weebit Nano methodically moved forward to make ReRAM a manufacturable technology, and may prove that it's good management that wins markets, not just good technologies.

However, it's still too early to name a winner in this battle. MRAM is on top now, with ReRAM chasing close behind. FRAM has an advantage with the widespread use of hafnium oxide, and should anyone pick up all of the technology and expertise that Intel put into 3D XPoint, then PCM could be a surprise winner.

The best anyone can do today is closely watch the developments in this market and be ready to adopt the technology that appears to be pulling ahead of the others. We naturally recommend reading our report, "A Deep Look at New Memories," to understand all of this in depth.

ROSS FENG | General Manager, Viasion Technology

Top 5 Challenges in PCB Assembly

In Part 1, we explore the benefits of miniaturization and the five main challenges it introduces in PCB assembly.

THE WORLD OF electronics is undergoing a transformational shift driven by the relentless push for miniaturization. As the demand for smaller, more powerful, and feature-rich devices surges, printed circuit boards (PCBs) continue to evolve dramatically in terms of miniaturization to enable such high-density integration.

However, with miniaturization comes unique design and manufacturing challenges that require creative solutions. This article examines the miniaturization trends of PCBs and the top five challenges introduced by miniaturization in PCB assembly.

The Rising Prominence of Miniaturization

The popularity of mobile devices, wearables, the Internet of Things (IoT), and other space-constrained electronics has fueled the movement toward PCB miniaturization. Consider how modern smartphones pack an astounding amount of functionality into a slim and compact package by leveraging advanced PCBs.

Similarly, wearable products like smartwatches must be designed around highly miniaturized PCBs to be convenient and ergonomic. In addition, applications such as medical devices, aerospace avionics, and automotive electronics are driving the need for smaller, lighter, and more power-efficient PCBs.

Drivers and Benefits of Miniaturization in PCBs

Several factors are catalyzing the push for miniaturization in printed circuit boards:

Improved Portability

Smaller and thinner electronics are more accessible to carry around. With the rising popularity of mobile and handheld electronics, having a small and lightweight product is no longer a luxury, but a fundamental need. Bulky electronics are inconvenient to carry around and use on the go. Miniature PCBs help create slimmer and more portable devices.

Integrated Functionality

More components can be integrated into the same footprint area. Greater computing power and functionality are being packed into smaller products nowadays. For instance, a smartwatch today can have cellular connectivity, health monitoring, GPS tracking, and more. Miniaturization makes it possible to fit more components and capabilities into compact devices.

Enhanced Efficiency

Shorter trace lengths in high-density PCBs enable better high-speed signal integrity and data-transmission rates with lower losses. Thus, miniaturization boosts the overall efficiency and performance.

Reduced Power Consumption

Compact designs reduce the overall power transition length, so there's less energy loss. Besides, compact designs dissipate less heat and require lower power.

Higher PCB densities enable components to be packed more tightly, reducing the overall dimensions. This lowers materials costs since fewer materials are used. Shipping and inventory storage costs are lowered as well due to decreased size.

Product Differentiation

A smaller, more elegant product garners greater consumer appeal and could be a competitive differentiator in the mar-

ketplace. Miniaturized designs can also enable differentiated form factors.

Top 5 Challenges in Assembling Miniaturized PCBs

While miniaturized PCBs provide tremendous benefits, effectively manufacturing them poses significant obstacles that need creative solutions. The five most pressing problems are:

1. Challenges in PCB Design

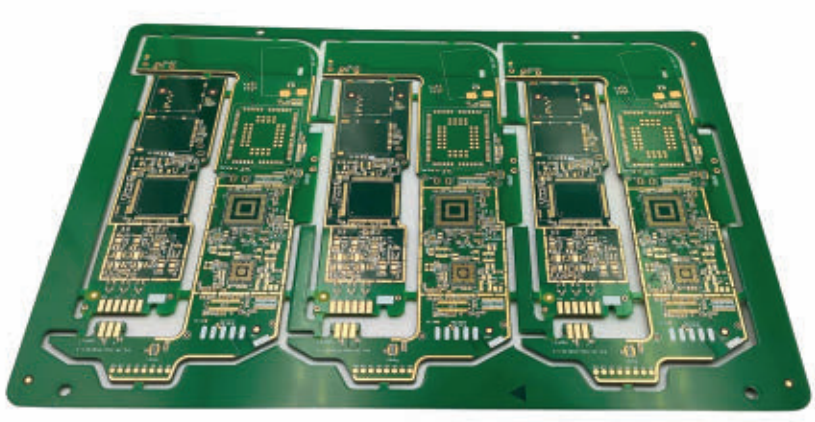
Signal integrity and thermal management are two major issues when dealing with PCB designs.

Maintaining signal integrity is already challenging on standard PCBs. But it becomes even more daunting with miniaturized high-density PCB layouts. The tighter spacing between traces increases parasitic capacitive coupling and trace crosstalk, which can distort signals, especially at higher speeds. Further, impedance mismatches at connections and shorter components lead to increased reflections. This exacerbates issues like ringing and electromagnetic interference (EMI).

Another miniaturization effect is an increase in dielectric constant and loss tangents when distances shrink below 100 µm. This degrades signal fidelity. High-frequency AC signals above 10 kHz are particularly prone to integrity issues. Signal waveforms must retain their intended rise time, amplitude, shape, and timing for proper functionality.

However, even minute signal degradations can disrupt digital logic, serial protocols, clock or data recovery, and analog performance, potentially leading to data loss or corruption. Matching trace impedances, adding ground planes, choosing suitable dielectrics, impedance-controlled routing, and termination resistors help maintain signal integrity. These measures require elaborate modeling, simulation, and analysis, creating cost and effort challenges.

Efficient thermal management is needed to address higher component densities in miniaturized PCBs. Otherwise, excessive heat can build up within such a constrained space. Managing this heat during operation is highly challenging, though.



1. High-density-interconnect (HDI) circuit boards have traces of 3 mils or less. *Viasion*

First, the compact footprint leaves little exposed surface area for heat dissipation through conduction or convection. Miniaturized components packed closely together generate localized hot spots. Second, many ingredients like semiconductors, high-power ICs, and RF chips are inherently heat-sensitive and prone to thermal failures. Their reliability degrades rapidly, with temperatures exceeding threshold levels.

Without effective thermal-management strategies like heatsinks, vias, or fans, the components can undergo accelerated aging, perform erratically, or fail permanently due to overheating. However, it's difficult to implement traditional cooling solutions given the size and form-factor limitations.

Advanced thermal simulation of the electrical, mechanical, and thermal characteristics combined with strategic cooling techniques is essential during the design process. Thermal-aware component placement and airflow optimization make it possible to manage heat dissipation from dense miniaturized PCBs.

2. Challenges in PCB Bare-Board Production

PCBs are produced with smaller and smaller drills, copper trace width, and space. Also, complex stackups and high layers—up to 100 layers—are designed and produced to address the demands of small size and high density.

Due to limited circuit board space, designers can only reduce line width and line spacing, reduce the diameter of drilling holes, or increase the number of layers. In this case, buried and blind via PCBs and high-density interconnect (HDI) circuit boards are gradually applied to such small-sized but multifunctional electronic devices.

In such printed circuit boards, with 3 mils or less trace width, plating through-hole (PTH) drills are as small as 6 mils, and laser drills as small as 4 mils *(Fig. 1)*. Even blind and buried vias, stacked and staggered vias, and any layer interconnect structure are used.

These bring many challenges and difficulties to circuit board production in drilling, etching, copper plating, and lamination. So extremely advanced equipment and very skilled CAM engineers and production workers are needed.

3. Challenges in PCB Assembly

Precise component placement and solder joint reliability are two of the challenges companies must address when assembling circuit boards.

Precise component placement is needed because densely packed PCBs have become extremely difficult to design due to ever-shrinking component packages and pad geometries. Standard pick-and-place machines require more precision to

position and align miniature components without errors.

Minor placement inaccuracies of even 50 to 100 µm can disrupt the acceptable tolerances and cause significant issues like electrical short circuits, impaired connectivity, signal loss, and reduced reliability. Yet, many miniature components like 01005-size resistors and capacitors can measure just 0.4 × 0.2 mm. Such details demand ultra-precise placement accuracy.

What's perplexing is that while component sizes continue to decrease, PCB densities are increasing even faster. Thus, the machines need to place more components in less space at higher speeds, stretching their limits. The margin for error is almost negligible.

Therefore, advanced placement systems with high-precision pneumatic nozzles, servo-motor-driven mechanisms, machine learning, and microscopic optics for pattern recognition are essential to achieve reliable miniaturized component placement. However, these solutions also raise the costs and slow the assembly process. It's a difficult tradeoff.

Solder joint reliability is important as shrinking component sizes and higher densities make these joints increasingly fragile and prone to failure in miniaturized PCB assemblies. Factors like coefficient of thermal expansion (CTE) mismatches, mechanical shocks, vibrations, and flexing introduce strains on delicate solder joints. Flaws like cracks, voids, and cold solder joints commonly arise, weakening the interconnects mechanically and electrically.

Also, during thermal excursions or temperature cycling, these defects can progress quickly into catastrophic solder failures, opening up electrical connections and disrupting functionality.

The root causes are more complex to diagnose and correct on densely packed PCBs. Further, smaller joints have a lower melting point, making them more susceptible to hot spots. Traditional soldering methods must be adapted to achieve robust and reliable solder bonds with miniaturized components.

Solder alloys with blending additives help create more flexible joints. Similarly, advanced solder masks limit bridging risks. In addition, spot soldering and laser soldering allow for localized heating. Overall, enhancing solder joint reliability requires significant process changes.

4. Unremitting Pursuit of Advanced PCB Materials and Smaller Components

Advanced PCB base laminates are needed because smaller circuit boards require improved electrical and mechanical processing performance, high TG, high frequency, high speed, and other high-tech materials that are widely used. For example, reinforced FR4 material can reach a Tg of 200, while PTFE material can reach a Tg of 350.

Ceramic materials are also used to meet the high-frequency or microwave requirements of electronic products. Flexible and rigid-flexible circuit boards employ polyimide materials to meet the requirements of lightweight and bendable products *(Fig. 2)*. Products with high thermal conductivity within small sizes will often turn to alumina ceramic materials.

Smaller components are needed because numerous functions and computing capabilities must be implemented on a very-small-sized circuit board, and that means more electronic components. However, the size of the circuit board is fixed, so only smaller components can be selected. For example, most passive components are 0201 or the smaller 01005. And the main chips come in space-saving packages, such as STQFP, VQFP, TQFN, VQFN, BGA, and UBGA.

The requirement for miniaturization of electronic components brings great challenges to the design and manufacturing of electronic components. It also increases the difficulty of PCB assembly.

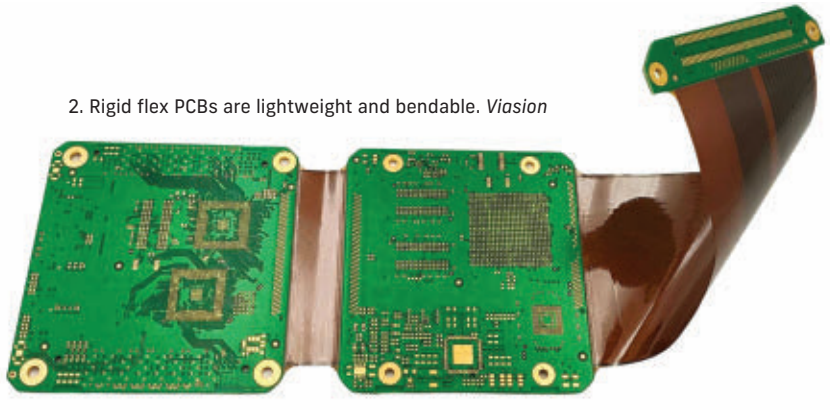
5. Rework and Repair Difficulties

Once assembled, carrying out any necessary rework or repairing the miniaturized PCB becomes challenging. The components are densely packed together with little space between them, leaving little room for error. A minor slip or overheating during manual rework can permanently damage adjacent components or traces.

Furthermore, the integrated nature of assemblies on multilayer boards makes access to repair points difficult. Reworking solder connections increases the risk of thermal damage to surrounding components. Using adhesives or underfill material to separate components makes removal and replacement time-consuming. It's also more difficult to realign components and secure new mechanical joints.

When attempting rework or repairs on densely packed miniaturized assemblies, extreme caution must be taken to avoid making matters worse and deteriorating workmanship quality. The costs of scrapping and replacing faulty PCBs are also higher. As a result, quality control prior to repair is critical.

In Part 2, we look at practical strategies to address PCB miniaturization challenges. ed

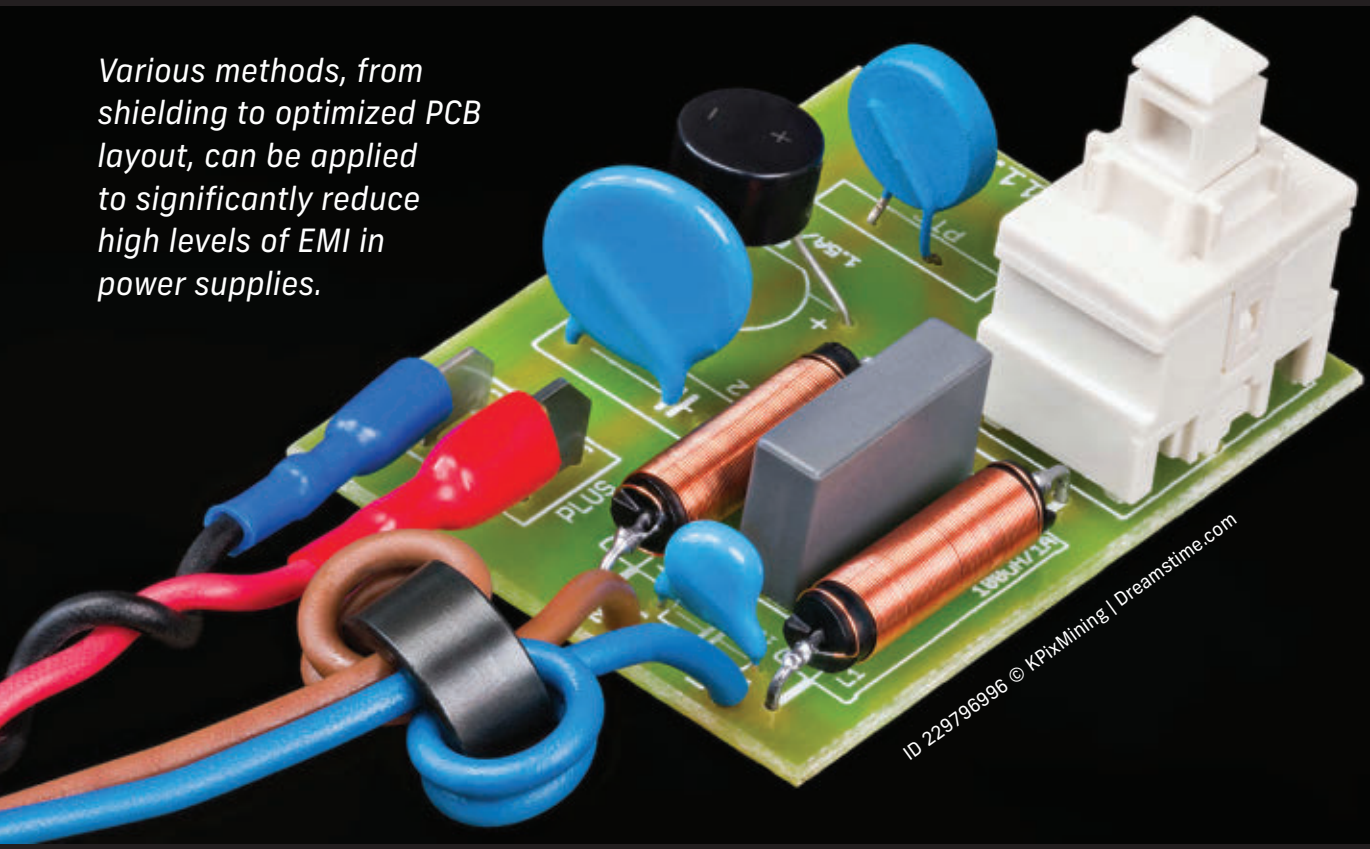


2. Rigid flex PCBs are lightweight and bendable. *Viasion*

STEVE TARANOVICH | Contributing Editor

Minimize the EMI in Your Power Supplies

Various methods, from shielding to optimized PCB layout, can be applied to significantly reduce high levels of EMI in power supplies.



MODERN ELECTRONIC SYSTEMS are becoming progressively denser with a high level of integration. This article will present some tried and true methods to reduce electromagnetic-interference (EMI) levels in power-supply system designs. Designers must be aware of serious EMI setbacks when they're in the late stages of the design phase, which could otherwise lead to excessive costs in money and time.

This article discusses how to improve EMI in terms of filter size and cost while reducing design time and complexity, especially in switch-mode power supplies (SMPS).

The switching effect in power metal-oxide semiconductor field-effect transistors (MOSFETs) leads to a significant source of EMI in the system. This effect will ultimately impact system reliability.

EMI mostly appears from discontinuous input currents, high slew rates on switching nodes, and more ringing on switching edges that's caused by parasitic inductances within the power loop.

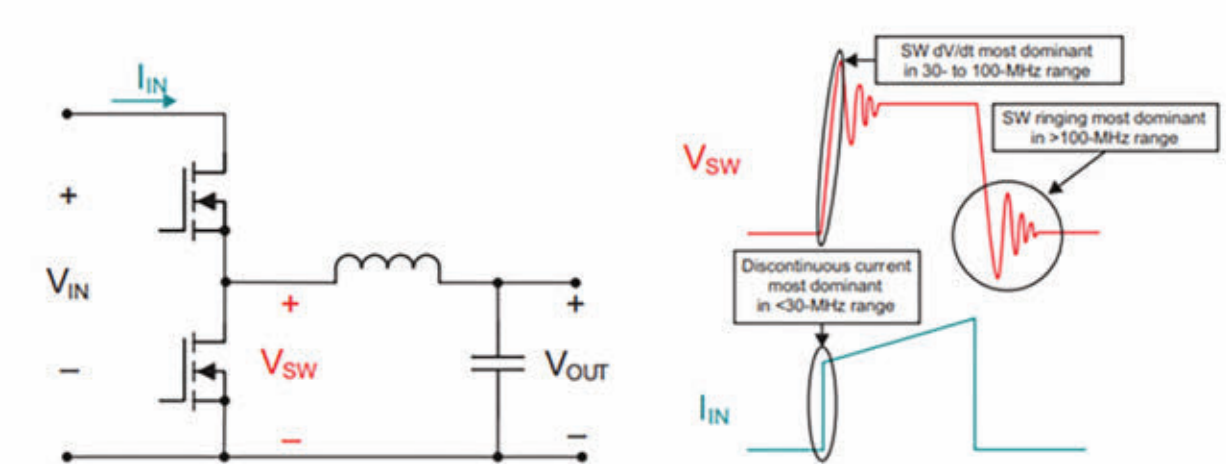
Sources of EMI in an SMPS

EMI can't be addressed late in the circuit design phase, because it could lead to setbacks in cost and time.

For example, consider the buck converter in *Figure 1*. It demonstrates how each element reveals itself within various frequency bands.

To reduce the cost and size of the SMPS, designers are presently trying to increase switching frequencies, which will also enhance efficiency. However, this shift to higher switching frequencies will lead to more EMI problems. Now designers will need to freely integrate EMI mitigation methods that will not compromise the power-supply design.

The above rules are well established in industry-standard specifications like Comité International Spécial des Pertur-



1. Shown is a prime example of EMI sources in an SMPS. *Images courtesy of Texas Instruments*

bations Radioélectriques (CISPR) 25 for the automotive industry, and CISPR 32 for multimedia equipment. Interference will be limited to a particular level, and susceptible circuits will be capable of handling that level of interference.

Approaches for Reducing Interference

Designers must know the applicable standard for each given application. Also important is to understand how to measure EMI, since this knowledge will give engineers better insight into reducing EMI.

In automotive design that involves long wire harnesses, conducted EMI relates to their increasing number in the latest vehicles. Some of the best ways to prevent or mitigate EMI:

Shielding

This is likely the best means to contain coupling or radiation EMI. Shielded metal housings and coatings can be used. Also, cables should be shielded to prevent external EMI from affecting sensitive components.

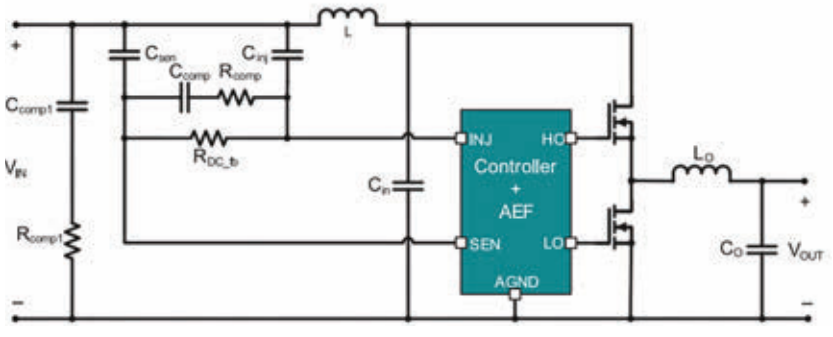
Filtering

Employ filters to eliminate unwanted signals. Passive filters may be frequently used to minimize EMI. Also, an AC line filter may prevent undesirable signals from entering the power supply or other powered circuitry. An integrated active EMI filter will help lower differential-mode (DM) conducted emissions at the input to a system, because it can serve as a very effective low-impedance shunt *(Fig. 2)*.

Ferrite beads can also suppress high-frequency noise.

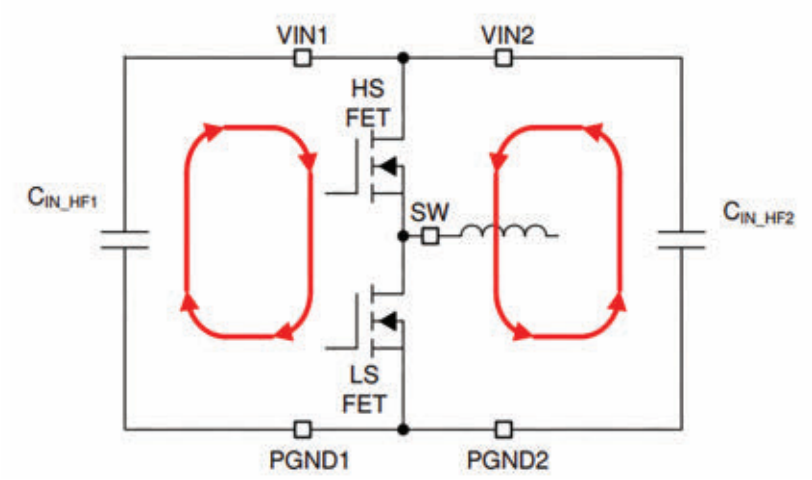
Grounding

Grounding typically provides a low-impedance path for EMI. When a sys-



2. This is an active EMI filter with sense components for compensation, and inject capacitors (Cinj).

To reduce the cost and size of the SMPS, designers are presently trying to increase switching frequencies, which will also enhance efficiency. However, this shift to higher switching frequencies will lead to more EMI problems. Now designers will need to freely integrate EMI mitigation methods that will not compromise the power-supply design.



3. Traces in the input current loop must be wide and short. The loop area should also be as small as possible to reduce parasitic inductance.

tem is properly grounded, EMI is diverted from critical equipment, improving power quality. Be sure to use proper grounding on a printed circuit board (PCB) and keep trace lengths short and away from PCB edges if possible. Also, minimize loop areas on the PCB to reduce radiated emissions.

Twisted-pair cables can help to reduce common-mode noise, too.

More Layout Tips

Let's look at the PCB layout for a typical DC-DC buck converter, which is crucial to optimal performance. The PCB layout is a key factor in achieving optimum EMI performance of the converter. In the buck converter, the loop formed by the input capacitor(s) and power ground is the most critical area. This loop will have large transient currents that lead to high transient voltages when they react with trace inductance.

Designers must be aware of the traces in this loop, which must be wide and short. The loop area also needs to be as small as possible to reduce parasitic inductance *(Fig. 3)*. Complete layout guidelines are given in Reference 2.

Avoiding EMI Disruption

EMI in a design can ruin a designer's day. It crops up when electromagnetic fields, which are generated by electrical/electronic systems, interfere with one another. This may lead to serious disruptions in circuitry, thus causing interruptions that can affect nearby electronic devices. A variety of methods can be applied to minimize EMI, as discussed in this article. ed

EMI in a design can ruin a designer's day. It crops up when electromagnetic fields, which are generated by electrical/electronic systems, interfere with one another.

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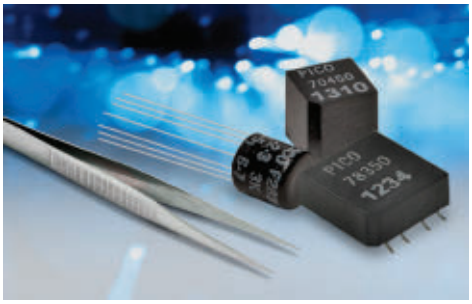

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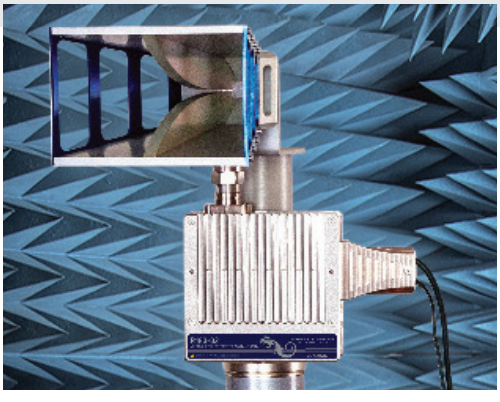

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Peripheral Connections for Prototyping

Rapid prototyping requires quick access to new peripherals—de facto standards can help.

PROTOTYPING HAS NEVER been easier with a range of standard modules like Standardization Group for Embedded Technologies' (SGeT) form factors such as SMARC, Qseven, OSM, and Embedded NUC. These plug into carrier boards that may contain peripherals or have connections for some of the peripheral standards noted here.

Another source of de facto board standards includes open-source ecosystems like Arduino, BeagleBoard, and Raspberry Pi. The ecosystems, which actually encompass a range of boards from companies built around them, have spawned a plethora of vendors using these open-source hardware form factors. The layouts are usually based around the expansion headers. The Arduino has a set of 18- and 14-pin single row headers while the Raspberry Pi has a single 40-pin header. BeagleBoard uses a pair of 46-pin headers.

The headers and module interfaces sport a collection of digital and analog interfaces that often include 1-wire, 2-wire (I2C), and serial interfaces with newer I3C, CAN, and Ethernet popping up, although not usually on the standard header.

Chip vendors typically deliver new processors on boards using one of these form factors to take advantage of third-party expansion headers. Likewise, sensor and other hardware vendors often provide expansion boards using the same form factors.

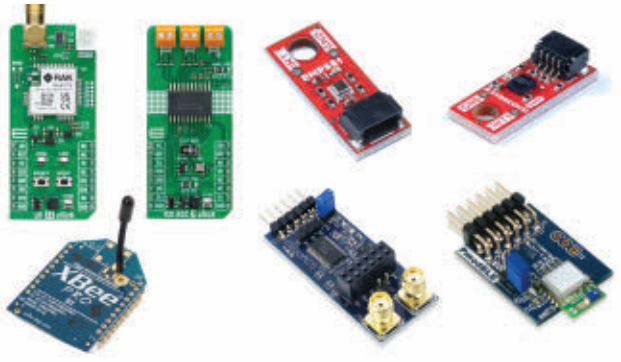
Other Peripheral Module Form Factors

Peripheral modules that plug into the board form factors are popular but less flexible, since they're locked into a particular host form factor. Luckily, a number of form factors are popular and don't conform to these requirements, including SparkFun's Qwiic, MIKROE's mikroBUS, Digilent's PMOD, and Digi International's XBee *(see figure)*.

SparkFun's Qwiic is a 2-wire I2C system that allows for modules to be daisy-chained. This is handy if one wants to put the peripheral module distant from the host. Some modules have a pair of connectors to facilitate daisy-chaining.

MIKROE's mikroBUS pinout has a number of interfaces—I2C, SPI, serial, and an interrupt pin with 3.3- and 5-V supplies. There are five 6- or 12-pin PMOD connector definitions that address digital IO, serial ports, I2C, and SPI with a 3.3-V power source. However, there's only a single interface type for each. Digi International's XBee uses a serial interface.

What these form factors have in common is a wide range of devices and often a growing number of third-party solutions, including vendors of sensors and other devices that they want developers to try out.



Starting from the top left, there are the MIKROE wireless and ADC mikroBUS modules, a pair of SparkFun Qwiic sensors, Digi International's XBee, and some Digilent ADC and Bluetooth PMODs. *Sparkfun, MIKROE, Digilent, Digi International*

Standard Module Form Factors

Not to be overlooked are two standard form factors designed for deployment: M.2 peripherals and Mini-PCIe devices. Designed to go into rugged devices, both sport higher-speed interfaces like PCI Express (PCIe) and SATA.

Whereas the other form factors are typically used for a range of sensors and control systems, M.2 and Mini-PCIe include high-capacity, non-volatile storage as well as wireless devices that work with operating systems such as Windows and Linux. They have also found a home in some mobile devices like laptops.

Lately, M.2 modules have offered artificial-intelligence and machine-learning (AI/ML) accelerator support. These typically use PCIe interfaces and target low-power, edge-computing solutions.

Interface Challenges and Use in End Products

While 5 V was once the norm for interface boards, 3.3 V dominates these days, with some 1.8-V boards available as well. Matching the voltages of the processors and modules can be a challenge, depending on whether a developer is looking for a general interface or a specific chip.

Deciding whether to use a peripheral module in a product is another matter. Many of the interfaces like PMOD and Qwiic tend to be used strictly for prototyping and aren't designed for rugged mounting. Some, like XBee, have a solid set of header pins that enable devices to be employed in products targeting many deployment environments. Form factors such as M.2 and Mini-PCIe are designed for deployment. These are often found in commercial single-board computers with form factors like PC/104.

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