Electronic Design

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Mitigating and Measuring EMI Disturbances at IC Inputs

Learn to measure electromagnetic emissions in integrated circuits caused by EMI disruptions, as well as the effect of power-supply interference on immunity and emissions.

In these modern times, electronic systems are usually operating within an electromagnetic-interference (EMI) environment that contains many other electronic systems. These systems need to exist and fully operate undisturbed while meeting electromagnetic compatibility (EMC).

Overview of Electromagnetic Compatibility

EMC requirements are separated into two main parts:

- Electromagnetic immunity—a system must not be disturbed by any other systems.
- The electromagnetic interference in a system can't disturb any other system.

Then, if immunity and emission requirements are individually met, the electronic product, such as an integrated circuit (IC), may be marketed from an EMC point of view.

Standard Measurement Techniques for ICs

Measurement methods for EMI and electromagnetic emission (EME) are fully described for ICs in the IEC62132-4 (immunity) and IEC61967-4 (emission) standards.[1]

Now let's characterize the EME at one of the IC pins while injecting a radio-frequency (RF) disturbance signal into another IC pin. To do this, we can use a combination of two widely used IC measurement techniques:

The 150-Ω method (IEC 61967-4)

The 150-Ω technique is a generally adopted approach selected to measure conducted electromagnetic emissions. It uses an impedance-matching network that consists of a 6.8-nF decoupling capacitor in series with a 120-Ω resistor and one 51-Ω resistor in parallel to the input of the EMI receiver. This will lead to an approximate impedance of 150 Ω for the device under test (DUT), in addition to a good matching for the input impedance of the EMI receiver.

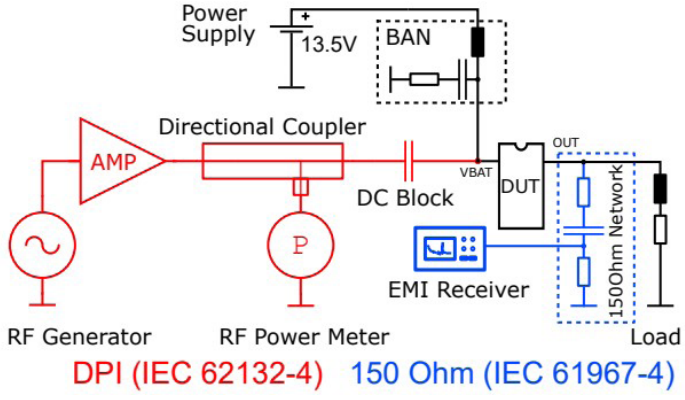
The deep packet inspection (DPI) method (IEC 62132-4)

The DPI method is an accepted approach chosen to simulate EMI caused by field coupling in antenna structures such as printed-circuit-board (PCB) traces or cables. This method involves the injection of a disturbance signal directly into an IC pin. The DPI is performed via an RF signal generator, which is generating the disturbance signal, and a power amplifier that will increase the power levels to meet the requirements of automotive test standards.

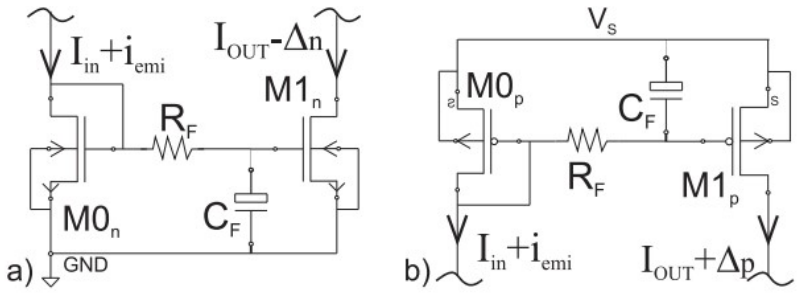
Both techniques offer highly reproducible and easy-to-use methods. Readers can see the complete setup as shown in *Figure 1*, with the DPI in red and the 150-Ω network in blue. By combining the two stages of the test procedure, it's conceivable to measure the EME at its output along with injecting a disturbance signal into the battery pin.

Moreover, the use of coupling networks, which are based on standards, assures that the test procedure is comparatively easy to perform while displaying excellent reproducibility.

The DUT in *Figure 1* is an automotive smart-power high-side switch. These types of components are typically used to



1. This image shows the measurement setup to perform interference induced electromagnetic emission measurements. The setup combines the DPI and 150-Ω methods. (Image courtesy of Reference 1, Daniel Kircher, Nikolaus Czepl, Dominik Zupan)



2. Shown are N-type (a) and P-type (b) current mirrors. (Image courtesy of Reference 5, Orazio Aiello)

control the vehicle headlights or switch the indicator lights. The device is operated in the switching mode via a switching frequency of 100 Hz along with a 50 % duty cycle. As a substitute for a car headlight, designers may choose to use a simple resistive load at the output. The disturbance is injected into the supply (VBAT) pin of the DUT.

Challenges of EMI in Modern ICs

A novel CMOS ultra-low-voltage (ULV) current bias solution offers a way to properly source ICs that are operating in subthreshold regions even in the presence of EMI.[7]

Power-supply reduction and scaling heightens susceptibility to EMI in ICs. The presence of disturbance can influence the behavior of analog building blocks—an issue that's become increasingly critical. The nominal IC behavior must be guaranteed in every operating condition; EMI filters can't be used since their presence may affect nominal circuit operation.

Among the fundamental IC building blocks, the susceptibility of current sources of ULV ICs creates quite a difficult task due to their reduced noise margin. However, a new current bias method presented below delivers higher EMI immunity with respect to existing current-mirror schemes.

Innovations in Low-Voltage ICs for Improved EMI Immunity

Technology trends in scaling and power-supply reduction have led to increased EMI susceptibility of ICs.[5]

Addressing this issue, a new CMOS ULV current bias solution for properly sourcing ICs that operate in subthreshold, even in the presence of EMI. The susceptibility of the current source of ULV ICs, including building blocks like the current splitter and current correlator, is a daunting task due to their reduced noise margin.

The robustness of the proposed EMI solution may be compared to conventional current mirrors. It's evaluated via analytic methods and time-domain simulation, with reference to the AMS C35 0.35-µm CMOS technology process, to prove the solution's higher EMI immunity to EMI.

Figure 2 represents the N- and P-type current mirrors, which include a low-pass filter (R_FC_F), to highlight the EMI-induced current. The DC offset is named Δn *(Fig. 2a)* and Δp *(Fig. 2b)*.

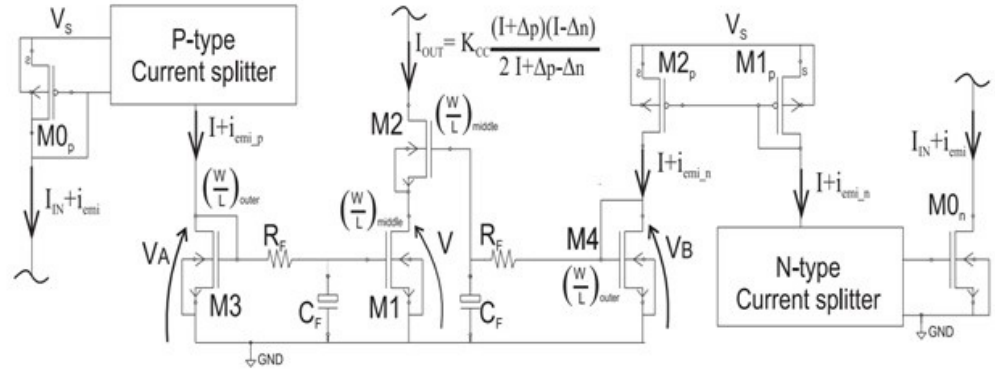
The above-mentioned circuitry, operating in subthreshold, are selected as building blocks for a new current biasing circuit depicted in *Figure 3*. The circuit provides an output current I_{OUT} (in the range of hundreds of nanoamperes and below) that's suitable for an EMI-robust, ultra-low-power IC. This is the case even if the input current I_{IN} is affected by EMI (i_{emi}).

The presence of complementary N- and P-type current splitters in *Figure 3* support the rapid scaling of the input current. They offer the significant benefit of an EMI-induced offset compensation based on an N-P offset compensation, which is performed through the current correlator.

The scaled currents coming from N- and P-type current splitters will flow to the respective current correlator that balances the opposite offset trend according to Equation 1:

$$I_{OUT} = K_{CC} \cdot I/2 \qquad (1)$$

If we assume that the aspect ratio of the current correlator



3. This is the proposed schematic block diagram of the new current biasing circuitry. (Image courtesy of Reference 5, Orazio Aiello)

equal to $K_{CC} = 2$, then:

$$I = I_{IN}/K_{CS} \quad (2)$$

Equation 2 acts as a current mirror-like function that's exceedingly immune to EMI for low-power-consumption ICs operating within the nanoampere region.

RFI Susceptibility

To verify the EMI strength of the proposed circuit solution, time-domain simulations were performed with reference to the AMS C35 0.35-µm CMOS technology.

Analyses were required referring to a traditional current mirror in *Figure 2a* and the proposed solution in *Figure 3*. For both current bias methods, the output current I_{OUT} = 200 nA is carried out by an input current I_{IN} = 10 µA affected by a continuous-wave (CW) RF current i_{emi}. The interference current i_{emi} is overlapping the input current I_{IN} and the DC offset on the output current I_{OUT} is treated equivalently to immunity tests.

Summary: Saving Time and Cost with Low-EMI Solutions

Engineers creating low-EMI designs will be able to shorten development cycle time, lower the cost of the solution, as well as the design board area. Some tried-and-true techniques developed by Texas Instruments use the company's EMI-optimized power-management devices. This helps certify that designs using TI components will pass industry standards with a minimum of rework.

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