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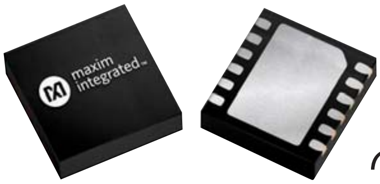

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EDITORIAL MISSION:
To provide the most current, accurate, and in-depth technical coverage of the key emerging technologies that engineers need to design tomorrow's products today.

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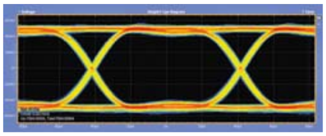

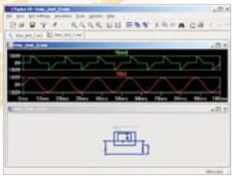

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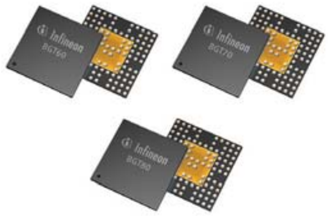

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SILICON LABS CEO DISCUSSES THE MIXED-SIGNAL IC BUSINESS

Tyson Tuttle reviews the Internet of Things, recent acquisitions, engineering education, and more.

SMARTWATCHES COMPARISON: THE TOP 10 ON THE MARKET

Today's watches can answer your phone calls, monitor your heart rate, provide a weather report, and even tell time.

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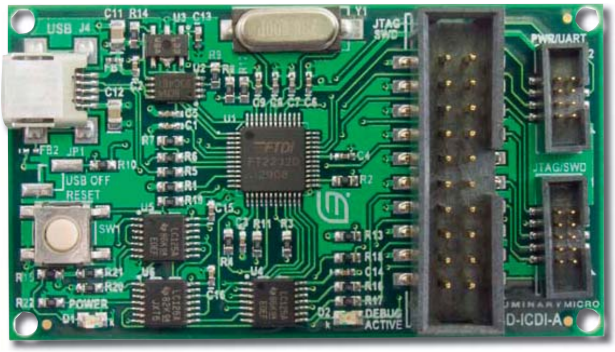

RUNNING EMBEDDED LUA ON MICROCONTROLLERS

The use of scripting languages in embedded systems helps perform a wide range of tasks.

FOUR TECHNOLOGIES CONVERGE IN HARDWARE EMULATION

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Developing The Secure Cloud

Edward Snowden's revelations exposed National Security Agency activities that have given many people and corporations second thoughts about taking advantage of the cloud, which is the latest term for the Internet. It was bad enough when developers had to worry about spammers, virus writers, and criminals bent on gaining access to private information. Companies also worried about losing information to corporate espionage.

Infrastructure as a Service (IaaS) and Platform as a Service (PaaS) platforms like Amazon Web Services (AWS) have allowed users to flock to the cloud to host everything from Web servers to corporate data storage. Most have been built on standard PC enterprise hardware that has hardware security support like TPM. But much of the communication between systems, including storage, moves over the network where software is used to control access.

Verizon's Terremark service recently announced that it will be using AMD's SeaMicro platforms, which employ a hardware hypercube communication fabric that can manage partitions that feature computing, communications, and storage *(see the figure)*. Also, its nearest neighbors won't affect performance, and their communication load will be isolated. It will allow cloud services to be compliant with the likes of the Health Insurance Portability and Accountability Act (HIPAA) and the Federal Information Security Management Act (FISMA).

AMD's SeaMicro SM15000 is the basis for Verizon's move into supply cloud compute and storage services.

Still, security is only as strong as its weakest link. Any system that utilizes the cloud for some aspect of its communication is susceptible to attack that can be silent and costly or noticeable and costly. We need to ask who holds the locks and keys.

Lavabit, a secure e-mail service company that Snowden and many others had used, recently shut itself down after the NSA first obtained a court order to put in a backdoor—and then for the key to the door. The problem with backdoors is that they are designed to be hidden, as is their use. Unfortunately, the security of the system comes down to who has the keys.

The latest design buzzword is Internet of Things (IoT). IoT usually means connecting anything that sends data to the cloud, where the cloud servers are often running on one of the PaaS or IaaS platforms. IoT gateway tools and reference designs of various types have been rolling by my desk for months, and most have some level of hardware security included.

Most companies with these products are providing the tools to secure a system but are leaving the actual implementation up to you, the developers. Hopefully you will educate yourself about the different aspects and tools for creating a secure system because it is more than just using tools like secure boot and AES encryption. ed

KAREN BARTLESON | Contributing Technical Expert

Standard-Essential Patents: Innovation's Boon Or Bane?

An interesting and powerful device known as the standard-essential patent (SEP) is in the spotlight. SEPs can bring wonderful inventions to people all over the world. They also can bring trouble. Big businesses are using them to wage war. Small businesses may be hit by them. The U.S. government is taking a closer look at what they mean to innovation and how they impact consumers. SEPs are the most intriguing element of the standards domain.

WHAT IS A SEP?

A SEP is no ordinary patent. It has special properties that can cause it to have even more widespread ramifications than a typical patent. Of course, a typical patent grants rights and privileges to its owner, who isn't necessarily the inventor. An entity can acquire a patent in several ways, such as through an acquisition or an outright purchase.

The owner can use it to prevent others from making, using, and selling the patented invention without permission. A patent owner can decide to keep the patent to itself, or it can choose to license the invention to any or all, at any price it desires. Thus, a patent can bring a distinct advantage, both monetarily and through market control.

A patent becomes even more interesting when it enters the standards arena. If a patent owner contributes the invention to become part of a technical standard, then everyone who implements the standard—and the goal of every good standard is to be widely implemented—will infringe upon the patent! Unless the patent's owner permits everyone to use the patent when they implement the standard, that is.

Because a patented invention that is part of a standard will have to be used by anyone who creates a product compliant to the standard, the patent is called a standard-essential patent. In most cases, the SEP's owner is allowed to charge a licensing fee to everyone, as long as it's not unreasonable.

There's no doubt that standards and patents have served and continue to serve humanity well. From the patent owner protecting its intellectual property to the companies that come together to create a standard that grows the market, as well as to the consumer who has greater choice and value in innovative products, standards and patents are key in a knowledge-based economy. And SEPs can provide the foundation.

For an implementer of a standard, access to a patented invention at a reasonable cost can be quite valuable. Being allowed to make, use, and sell a unique invention, without the high cost of inventing it, can expedite a vendor's entry into a marketplace. Startups and large competitors alike can be anxious to be allowed to implement a prized patented invention. A SEP can be a catalyst to a vibrant, growing market.

The holder of a SEP may have a powerful tool at its disposal as well. If the patented invention is really good and there's a demand in the marketplace for products that use the invention, the holder might realize a solid revenue stream through licensing for years. (Again, the cost of a license must not be unreasonable.) Having numerous vendors implement the SEP and pay a fee to the owner can be an extra benefit to the owner over keeping the patent out of the standard.

Indirectly, even the consumer can get value from a SEP that is contributed to a standard. Standards bring product quality, interoperability, and reliability. They also facilitate consumer choice. The availability of multiple high-quality, innovative products to choose from makes buyers happier. Everybody can benefit when SEPs are intertwined with standards.

The base requirement for SEPs to be constructive is licensing under FRAND conditions. Without FRAND, SEPs can cause costly conflicts. FRAND is the acronym for fair, reasonable, and non-discriminatory. It's also known as RAND—reasonable and non-discriminatory. According to the principles of FRAND licensing, the patent owner must allow anyone to take a license, the license terms must not be illegal or anti-competitive, and the cost of the license must not be too high.

When a patent owner licenses a SEP with FRAND terms, it can be a win-win. The owner makes money from the patent as well as the invention itself, if the owner is also selling products that use the invention. Competing vendors pay a small price for access to a big invention. The market can grow more rapidly when a standard is combined with a patent.

THE SEP CONTROVERSY

However, SEPs have created so much contention that even the U.S. government is scrutinizing them. Several aspects to SEPs can make them hazardous and complicated to the patent owner, standard implementers, innovators, and consumers.

A patent owner should be very careful when participating in standards-development activities that are associated with the patented technology. It is nothing short of cheating to contribute patented technology to a standard and later file a lawsuit for patent infringement on everyone who has implemented the standard. This bad practice can result in the loss of patent rights for the owner, as happened in the famous case in 1996 of Dell and the VESA VL-bus standard. Very recently—demonstrating a good practice—as Google acquired Motorola Mobility, it negotiated with the U.S. Federal Trade Commission (FTC) and agreed to honor Motorola's (F)RAND obligations.

When a SEP owner agrees to license it under FRAND terms, who determines what exactly is fair and reasonable? The owner may think it's fair to charge a royalty of a few pennies per part. But if a product contains hundreds of the part, the product developer may see the cost as exorbitant. The owner may believe it's reasonable to obtain non-SEP patent licenses from others in exchange for its own, but other patent holders may see this as an attempt to steal their intellectual property.

What happens if a SEP owner offers a FRAND license to everyone, but a vendor chooses not to take a license? Should that vendor be allowed to implement the publicly available standard anyway? Or should injunctions be imposed on the vendor? Some people fear that SEPs could stifle innovation if a SEP owner cannot assert its rights.

An interesting twist these days is that patents, and especially SEPs because their impact can spread so broadly, can bring in a healthy revenue stream for companies that purchase patents for the sole purpose of suing potential infringers. These companies are known as patent assertion entities (PAEs), non-practicing entities (NPEs), or, less kindly, patent trolls. A SEP in the hands of a troll can be a potentially explosive device, giving standards a bad name and harming businesses.

A fundamental risk of a SEP is that the patent might not be essential after all. The SEP owner can claim it is essential, and others may claim it is not. Fear and threats may stall or halt the standardization process. Or, the process can continue until the standard is widely adopted when it becomes clear that the patent was indeed essential to implementing the standard and an epic clash begins.

Disputes over SEPs are settled in courts of law, one case at a time. This can be very costly to an entire industry, not to mention a burden on the judicial system. Because FRAND is an indeterminate concept at present, every case can be different and yield a different remedy, often after years of debate and appeals.

SEP HORROR STORIES

Standards in general bring goodness. Many of them work so well, they're taken for granted. They promote the next level of innovation, giving advantages to companies and entire industries. But when there are problems, there can be serious ramifications, and SEPs become even more interesting. Many horror stories involving SEPs can be found with a simple search for "standard-essential patents."

Currently one of the most prominent is within the colossal battle between Apple and Samsung. After a complaint by Samsung that Apple had infringed on a Samsung-owned SEP, the U.S. International Trade Commission placed a ban on importing Apple's iPhones (before the 4S) and cellular iPads (before the third-generation iPad 4G) into the U.S. Immediately, Apple protested and soon the ban was overturned by the White House (the first time in 26 years that a President overturned a ruling by the ITC). Now there are cries of U.S. protectionism and threats of mobile phone shortages for consumers.

A less prominent story revolves around IEEE 802.11, or Wi-Fi. In Australia, the Commonwealth Scientific and Industrial Research Organization (CSIRO) asserted that it owned a SEP connected with Wi-Fi. In 2012, CSIRO demanded payment from six large companies who coughed up $229 million to stay out of court and risk having to pay more. In 2009, CSIRO did the same thing to 14 other companies and raked in $200 million.

WHAT SHOULD BE DONE?

When licensed under FRAND terms and without controversy, SEPs can be a boon to the industry and consumers. With their ability to distribute innovations widely and promote competition, SEPs are beneficial to society. But when things go wrong, SEPs can be at the heart of big, ugly, expensive conflicts.

Some say these conflicts are few and far between, corner cases that are dealt with by the courts. Nothing needs to be done about controversial SEPs as the industry is healthy, innovation is continuing, and consumers have more choice now than ever.

Others believe the problems with SEPs are escalating and affecting companies, innovators, and society. They say that too many SEPs turn out to be non-essential after wasting time and resources. They are asking for governmental intervention and policies that provide remedies or prevent injunctions. There is also growing concern over patent trolls with SEPs. As the U.S. Department of Justice continues its investigation into SEPs, new legislation could be put in place to temper the increasing strife.

Another possibility is to improve the quality of patents, and SEPs in particular, from the outset. This could help ensure that SEPs are valid and lawsuits that are filed are more appropriate. Standards-developing organizations could work more closely with patent offices toward this goal.

Standards-developing organizations have patent policies that usually include SEPs and FRAND requirements. These policies could be enhanced to refine the definition of FRAND and state the consequences of SEP misuse.

There may be additional creative solutions to the problems caused by SEP abuse. All interested parties are invited to contribute. In the meantime, SEPs will continue simultaneously to benefit and frustrate the world. ed

KAREN BARTLESON is the senior director of community marketing at Synopsys Inc. She also is president of the IEEE Standards Association for the 2013-2014 term. She holds a BSEE from California Polytechnic University, San Luis Obispo, Calif.

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News & Analysis

Surveillance Surge Drives New Data Management Technologies

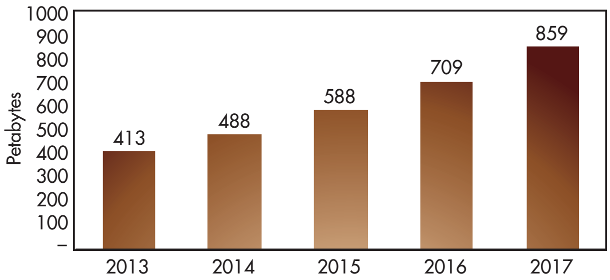
If you think Big Brother can see you better than ever before, you aren't wrong. Each day, surveillance cameras around the world produce 413 petabytes of data, according to IHS Inc. That's enough information to fill 92.1 million single-sided, single-layer DVDs.

New high-definition video cameras now entering the marketing are driving this total, which IHS expects to double in four years to 859 petabytes by 2017. In turn, technologies that can handle and process big data will grow as well, the company predicts.

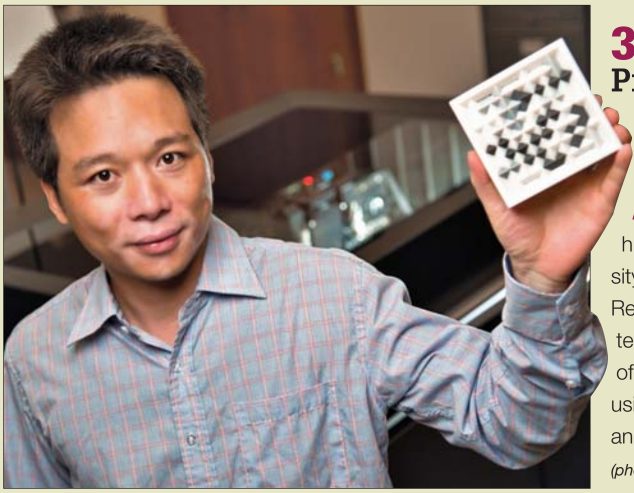
"These cameras are gaining acceptance because the quality of their video can be superior to standard-resolution products that formerly dominated the market," said Sam Grinter, senior surveillance analyst at IHS. "But because each HD camera produces far more data than each standard-definition camera, the quantity of data generated by the surveillance market is growing to massive proportions."

Innovative technologies such as new compression algorithms will accommodate and mitigate this huge data increase. Also known as H.265, the High Efficiency Video Coding (HEVC) standard doubles the data compression ratio compared to H.264, reducing the amount of data produced per camera.

Also, video content analysis (VCA) can reduce the time a video camera records by using virtual tripwires and no-entry zones. These technologies can trigger cameras to record only when a predefined event has occurred, such as someone entering a parking lot, reducing the amount of data produced as well.



The worldwide body of video surveillance data will double between now and 2017 to 859 petabytes, driven by high-definition cameras and driving new data management solutions. *(courtesy of IHS)*



3D PRINTING Produces Parts For Military Field Repairs

POSTDOCTORAL RESEARCH ASSOCIATE Yuezhong Feng and his colleagues at Purdue University are working with the U.S. Army Research Laboratory to develop a technology for creating parts out of interlocking segments produced using 3D printing to repair vehicles and other equipment in the field.

(photo by Steven Yang, Purdue University)

Finally, IHS expects hard-disk drives (HDDs) to play a role in data management since their capacities continue to increase. While the amount of data produced per camera is expanding, so is the capacity to record that data, either on site or via networked systems.

For details, see the IHS report, "Enterprise and IP Storage used for Video Surveillance—World—2014" at www.imsresearch.com/report/enterprise_and_ip_storage_used_for_video_surveillance_world_2014.

ELECTRONIC DESIGN STAFF

Wi-Fi Riding High And Reaching Higher

WI-FI HAS BECOME THE go-to wireless service to meet our demands for ever-faster Internet access and multiple demanding applications like video. Our laptops, tablets, and even smart phones would be next to worthless without Wi-Fi. And Wi-Fi keeps getting better with faster versions like the new 802.11ac standard, which delivers up to 1.3-Gbit/s service in the 5-GHz unlicensed band. The Wi-Fi Alliance's Hotspot 2.0 (Passpoint) also greatly enhances the use of Wi-Fi for roaming and automatic connections.

As the number of Wi-Fi hotspots increases, many of them are part of a growing system of carrier Wi-Fi networks. Carrier Wi-Fi generally refers to high-quality hotspots supported by the cellular carriers hoping to offload some of their high-speed video traffic from the cellular network, easing the burden and slowing the need for the rollout of even faster LTE and LTE-Advanced 4G services. While Wi-Fi offload is not common yet, it is coming as the cellular providers add Wi-Fi networking capability.

Cable TV operators also are enthusiastically adopting Wi-Fi as their entrance into the lucrative wireless market. Five of the biggest U.S. cable operators—Bright House Networks, Comcast, Cablevision, Cox, and Time Warner Cable—have formed an alliance called Cable WiFi to take advantage of their growing Wi-Fi use. Customers of any of the alliance members can roam seamlessly in the largest Wi-Fi network in the U.S. with more than 150,000 hotspots.

ABI Research says this marketing strategy will allow cable operators to better retain their customers and enhance their service while providing a way to monetize the roaming feature. Carrier Wi-Fi access point shipments will reach 9.7 million users by 2018, ABI predicts. This is positive news, but is there a downside? "Seamless access to high-data-rate Wi-Fi is helping to shape user expectations and behavior in the cellular network, creating a traffic onload effect counter to offload benefits," says Ahmed Ali, a research analyst at ABI.

The cable companies are also battling the carmakers over Wi-Fi spectrum issues. The cable companies want more Wi-Fi spectrum to expand their services. This expansion is encroaching on the car companies, who are working to use Wi-Fi in the forthcoming Intelligent Transportation System (ITS). The auto companies want to implement vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) systems in cars and trucks to greatly reduce accidents and traffic congestion. The conflict centers on valuable space in the 5-GHz unlicensed spectrum. The Federal Communications Commission (FCC) will have its hands full resolving this one as these giant industries battle.

For details, contact ABI Research for its latest report, "Carrier Wi-Fi Operator Activity: North America, Japan, Korea and Europe," at www.abiresearch.com. Contact the WBA for a look at its NGH report at www.wballiance.com. For more information on Passpoint, see the Wi-Fi Alliance at www.wi-fi.org.

LOUIS E. FRENZEL

GEORGIA TECH DEVELOPS ORIGAMI ANTENNAS

RESEARCHERS AT GEORGIA Tech are using origami techniques to develop antennas that can fold themselves into different shapes in response to incoming signals using self-activation mechanisms. Sophisticated inkjet printing techniques will deposit conductive materials onto the antenna elements. The researchers hope to achieve powerful, ultra-broadband capabilities in a device that measures just a couple of centimeters when folded up. *(courtesy of Rob Felt, Georgia Tech)*

BILL WONG | Embedded/Systems/Software Editor
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Creative's Senz3D 3D camera utilizes SoftKinetic's time-of-flight 3D imaging technology.

CONSUMER CTRONICS Take User Interfaces Beyond Your Fingertips

You don't need keyboards and mice to interact with your devices anymore. Now you can use haptics, 3D imaging, and more.

Remember when you had to push a button or turn a handle to make something happen? It seems like a long time ago, but control via touch, swipe, wave, and voice really have been recent developments. Still, the trends are clear.

When I walk up to my Toyota Prius, I unlock the door by pulling the handle. The car recognizes me via the key fob in my pocket. The same technology lets me start the car by pressing a button. Our other car requires a key. I only drive it occasionally, but I usually forget to pull out the key, and I look silly trying to start the car by pressing a non-existent button.

The Prius is the newer vehicle. Its voice-activated navigation system requires a button press on the steering wheel. But from then on, it's all voice interaction for everything from making a call to changing a navigation point. My version is keyword-oriented, so it is not a matter of speaking naturally.

These features have been standard on higher-end models for years, but there have been big improvements in functionality, performance, and reliability. The same is true for mobile devices and appliances, from tablets to washing machines.

A TOUCH ON GLASS

Mechanical buttons used to be cheap. They still are for many applications, but touch sensors are more the norm now where microcontrollers and microprocessors are involved. Touch interfaces are built into many microprocessors. Creating the custom sensor layouts for multiple controls has assembly, reliability, and cost advantages.

Gesture recognition is common on smart phones and tablets courtesy of touch support. Gesture recognition can even be built into a chip. A few gestures tend to be commonly supported such as point and press as well as dials and sliders that usually have a displayed representation on a dynamic screen or a static layout.

The Apple iPhone popularized the pinch and zoom and swipe gestures. More advanced gestures, however, tend to be application-specific or device-specific, making them look more like magic. This can lead to user confusion when users don't know what types of interaction the devices support.

Capacitive touch technology can also support 3D sensing. The Z-axis typically has less accuracy but is more than sufficient for 3D gestures. 3D gesture sensing can be used to provide additional feedback such as highlighting a button

1. Strategic Polymer's Awake keyboard prototype employs polymer-based feedback for each key.

before it is pressed in the same fashion as when a cursor hovers over a button or menu item and a help bubble appears.

Feedback mechanisms can be divided into motorized, piezoelectric, and polymer actuators. Rotating and linear motorized systems have been very common, but some of the latest controller chips can provide sophisticated feedback mechanisms that are easy to coordinate. Piezoelectric systems can be very compact, allowing them to be employed in places where it would be difficult to place a motorized actuator.

Polymer-based systems are even more compact, so they can be used for localized feedback. Strategic Polymer's Awake keyboard prototype *(Fig. 1)* implements feedback for each key using electromechanical polymer actuators (EMPs). The technology allows extremely thin systems.

Pen interfaces complement touch interfaces. They can be implemented using the same technology used for finger touch recognition, although controller chips tend to specialize in stylus and multi-touch support.

Pens are more precise than fingers. This is useful for many applications including drawing. Pens can take advantage of the high accuracy of their sensing systems. They also can have buttons that improve their functionality once the user understands what the buttons can be used for.

Keyboards, both physical and now virtual, unfortunately have reduced cursive penmanship to a dying art. The new pen interfaces probably won't change this trend, but the interface is likely to remain useful. At this point the challenge is actually more on the application side rather than the hardware, though there is little demand for more stylish pens as there has been.

GAMING THE MOTION SYSTEM

More mobile devices like smart phones and tablets are incorporating microelectromechanical systems (MEMS) like 3D accelerometers and gyroscopes. These components can determine their orientation so smart phones and tablets, then, can do tricks like automatically switching from portrait to landscape mode. Smart phones and tablets also then can be used as game controllers and remote control devices.

Android phones and iPhones can be used to fly Parrot's AR.Drone electric quadrotor UAV. The interface takes advantage of these sensors as well as the touchscreen, which also displays the output from the UAV's on-board cameras. This provides a better control mechanism than a touch interface alone.

Sensor fusion crops up with multiple sensors. It enables the creation of virtual sensors. For example, a 3D virtual position sensor could be based on inputs from a GPS, an inertial navigation system (INS), plus 3D accelerometers and gyroscopes. The virtual sensor would use the information from all of these sources, but sometimes some may not be available.

For instance, GPS will not work in certain areas where radio reception is poor. INS systems tend to be power-hungry, whereas accelerometers tend to use very little power. A low-power device may not provide high accuracy, but it may be sufficient in many instances. It may also be the only one that is available in a particular location or time frame.

2. Sahas Katta's Glass Tesla application enables Google Glass users to control some of their Tesla car functionality.

Non-traditional control systems with multiple sensors and sensor fusion abound these days. Google Glass is one example *(Fig. 2)*. Users simply look up to see a large screen that's really a fraction of an inch. There is also a camera, 3D accelerometers, and audio feedback.

3. The Oculus Rift 3D virtual reality personal display from Oculus VR uses 3D gyroscopes to track head movement.

Voice commands and phone calls can be made using the device when it's linked via Bluetooth to a smart phone. Audio feedback uses bone conduction technology rather than an earbud.

One needs to experience Google Glass to understand how it changes the way one deals with a hands-free system. Speech recognition is important since it is used to initiate functions such as taking a picture or asking for directions. Imagine looking at a 3D map of your current location and turning your head to see what is nearby.

Sahas Katta's Glass Tesla application runs on Google Glass. It is designed to work with a Tesla electric car, providing location and charging information as well as limited control of the vehicle. Glass Tesla provides a way to wear sensors and a display, which is a conventional 2D display for one eye.

Oculus Rift is a 1080p, 3D, virtual reality headset from Oculus VR *(Fig. 3)*. Built-in 3D gyroscopes track head movement so the images presented to the displays in the headset can provide a virtual reality environment.

The head isn't the only thing to track with the absolute 3D positioning technology from Sixense. It uses a rotating magnetic field to track multiple sensors, which can deliver high-precision, absolute position information under 1 mm. The STEM System is a successful Kickstarter project that provides 3D hand controllers and clip-on sensors to more accurately track body movement *(Fig. 4)*.

The ultimate is a combination of Oculus Rift, Sixense's STEM System, and Virtuix's Omni *(Fig. 5)*. The Omni is a platform as well as an interface device. The combination is probably the closest thing to a holodeck that can be achieved today.

Users stand in the middle of the Virtuix Omni platform. It has a low-friction, grooved surface with a low-angle, bowl-like architecture. Users wear a special set of pinned shoes that slide easily along the groves. This stabilizes the feet and prevents sliding sideways. Users slide back to the center even when walking in any direction.

Users also wear a belt that is connected to the stabilizing ring. They can then walk, run, jump, and slide in place. It is very good but not perfect.

4. The Sixense STEM System uses magnetics to provide absolute 3D positioning information for multiple wireless sensors including hand control units.

The system translates general movements into actions that a game can take advantage of so the display presented on the virtual reality headset will replicate these actions in the virtual world. Virtuix Omni will work with other controllers as well.

Gaming is not the only place where virtual reality will make a difference. In fact, non-gaming applications will likely be more important as the technology becomes more available such as Sixense's MakeVR software, an easy to use 3D CAD system.

3D VIDEO IMAGE RECOGNITION

3D video playback has not been successful in the HDTV market, but 3D image recognition has. Microsoft's original Kinect, based on PrimeSense 3D imaging technology, has been a huge hit for Microsoft's XBox. It has also been a boon for robotics developers.

The second incarnation of the Kinect utilizes a different time-of-flight technology developed by SoftKinetic. In this case, a simple infrared emitter is used and a special image sensor can detect the timing associated with the light pulses.

SoftKinetic provides development platforms that work in near-field configurations like that found in front of a laptop or far-field that would be needed for a stand-up gaming system like the Kinect. The primary difference between near-field and far-field operation is the intensity of the infrared diode. Far-field operation requires more power that would blind the sensor in near-field operation.

The Creative Senz3D looks like a typical HD clip-on USB camera, but it incorporates the near-field version of SoftKinetic's engine *(Fig. 6)*. Like HD cameras, the 3D systems could be built into mobile devices like laptops and tablets.

Microsoft provided a software development kit (SDK) for its Kinect platform after hackers turned the initially closed device into a practical tool. Now gesture recognition can be achieved using the Kinect for applications like robotics. The SDK does the heavy lifting, including support for skeletal tracking and 3D gesture recognition.

Intel's Perceptual Computing SDK is another framework for working with 3D imaging and more because it also addresses other sensor inputs including audio. Creative's Senz3D is the 3D imaging hardware reference platform for the SDK.

Yet another 3D imaging technology is available from LeapMotion. Like the aforementioned platforms, it is available as a USB-based device and supported

5. Users of Virtuix's Omni walk on a low-friction surface while wearing 3D virtual reality goggles like the Oculus Rift.

by gesture recognition software. LeapMotion's approach also uses a set of infrared emitters and a sensor packaged in a small dongle that sits in front of a laptop so it can see a user's fingers and hands when gestures are performed in front of the device.

LeapMotion's technology is built into HP's Envy notebook. It is integrated with Microsoft Windows, which enables the user to control the interface without touching the screen. The advantages of integration are significant since placement is fixed with respect to the screen and the sensor is hidden within the case.

3D is not a requirement for a useful image recognition tool. Sufficient resolution and processing power are all that are needed. Processing power can be significant so an Arduino platform might be impractical, but heftier compute platforms like a Tegra 3 or 4 do have the horsepower for this type of analysis. For example, the Vital Sign Camera application from Philips can detect heart and breathing rates using the video stream from a conventional camera on most mobile devices.

PointGrab provides Microsoft Windows-based 3D gesture recognition using the typical built-in camera found on notebooks and tablets. Pinch and zoom hand gestures can be used to interact with applications without a touchscreen interface. Its 3D precision is not as high as the 3D devices already mentioned, but that is often unnecessary for analyzing gestures and relative motion where visual biofeedback is sufficient.

Systems like the Kinect that use infrared imaging do not work well in many environments, such as in daylight where sunlight can overpower and blind the sensors. PointGrab's system will be limited by the camera as well.

Dual-camera 3D imaging systems are also available, but they have yet to scale to consumer level products. They also have high computational requirements. Camera-only solutions can suffer from aliasing issues in the analysis software as well.

BIOMETRIC RECOGNITION

Voice recognition and control has been around for decades with significant improvement. It only requires a microphone and a speaker for feedback, so it is even lower in cost than imaging systems.

Wading through automated voice call centers is no fun, but you might find the latest interactive voice response (IVR) systems to be rather fluent and understanding. IVR is a combination of steady voice recognition improvements and the ability to apply more processing power to the problem. Improved audio processing also removes background noise and improves the starting point for voice recognition software.

Voice recognition has become more common in addition to IVR systems. It can be found on most automotive navigation systems, and Apple's Siri brought the world's attention to voice recognition on smart phones.

The challenge with voice recognition compared to image processing is that the expectations for voice recognition are much higher. Most people expect a system to understand the meaning of a statement they issue and have the computer act accordingly, whereas the current state of affairs with image recognition is more basic with pinch and zoom gestures activating a limited set of actions.

Fingerprint recognition is used for identification purposes, but its cost and reliability have improved greatly. Various forms of the technology have been available for years, though it has become more common.

Apple's iPhone 5 is notable because its single button doubles as a fingerprint sensor. The first swipe likely will identify the user. An entire article could be written about the issues surrounding the iPhone 5's sensor and security.

Fingerprint sensors are standard fare on other devices like laptops and desktop keyboards. They can even be found on secure external hard drives like those from Apricorn.

Biometric identification is not necessarily restricted to fingerprints. Face recognition using cameras is already available. Applications like Visidon AppLock use the forward-looking camera on smart phones. In the future, biometric sensor fusion with other methodologies such as voice recognition may provide faster, more secure recognition. ed

6. Creative's Senz3D utilizes SoftKinetic's time-of-flight 3D imaging technology.

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ADC MAKERS CHALLENGE CONVENTIONAL WISDOM About SAR Speed And Resolution

Texas Instruments, Analog Devices, Maxim Integrated, and Linear Technology have launched 18-bit and even 20-bit resolution SARs at sampling rates of 500 to 5000 ksamples/s.

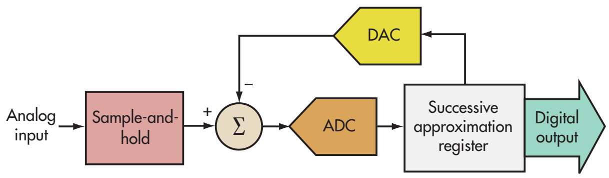
2013 has been a remarkable year for performance improvements in successive-approximation architecture (SAR) analog-to-digital converters (ADCs). While there were a few announcements about new delta-sigma (ΔΣ) and pipeline-architecture ADCs, SARs dominated *(see "Only TI Added New Pipeline And ΔΣ ADCs In 2013," p. 32)*.

The conventional wisdom about ADCs used to say that if circuit designers wanted high resolution, they had to look to the ΔΣ architecture. If designers wanted to look at more rapidly changing data, they had to use a converter built on the SAR architecture. As of 2013, that's only partly true. The newest ΔΣs still offer the very highest precision.

If you're searching for oil reserves out on the patch, for example, Texas Instruments' ADS1282 will give you 31-bit precision at 4 ksamples/s. (It is, in fact, marketed "for seismic and energy exploration.") To run at faster rates than that, even the latest ΔΣs must sacrifice resolution. A useful document, "Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs," from Maxim Integrated noted that some high-bandwidth ΔΣ converters have reached bandwidths of 1 to 2 MHz, but they are limited to 12 to 16 bits of resolution.[1]

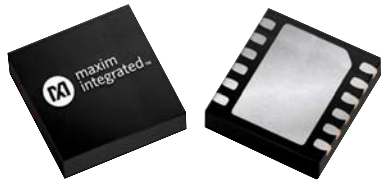
If, however, you want to look at higher-frequency data, say for industrial control, robotics, automotive, or instrumentation applications, and you want both precision and high conversion rates, several new SAR ADCs are exhibiting remarkably high precision performance—18 and even 20 bits—and sampling rates from 0.5 to 5 Msamples/s.

That's with zero latency. The data on the output bus represents the voltage on the sample-and-hold right now. This year, there have been five new SARs in that performance range *(see the table)*. That's not counting the members of each family that bin out just a little slower or less precise.



1. SAR converters compare the analog input voltage against a descending series of voltages (1, 1/2, 1/4, 1/8, 1/16... 1/2N times the reference, up to the resolution of the ADC) and accumulate the results.

2. Linear Technology's LTC2378-20-1 SAR ADC boasts 20-bit precision at 1 Msample/s.



3. The Maxim Integrated MAX11156 SAR ADC offers 18-bit performance with no missing codes at 500 ksamples/s.

SAR REFRESHER

To digitize the voltage on a sample-and-hold circuit, SAR converters compare the sampled input voltage against a series of successively smaller voltages *(Fig. 1)*. Each voltage represents one of the bits in the digital output code. These voltages are fractions of the full-scale input voltage (1/2, 1/4, 1/8, 1/16... 1/2N, where N = number of bits).

The first comparison is made between the analog input voltage and a voltage representing the most significant bit (MSB). If that analog input voltage is greater than the MSB voltage, the value of the MSB is set to 1. If it isn't greater than the MSB voltage, it's set to 0.

The second comparison is made between the analog input voltage and a voltage representing the sum of the MSB and the next MSB. The value of the second MSB is then set accordingly. The third comparison is made between the analog input voltage and the voltage representing the sum of the three MSBs. The process repeats until the value of the least significant bit (LSB) is established.

THE LATEST SAR LINEUP

These SAR ADCs began to appear in late May. At that time, Linear Technology announced the highest-precision device of the lot: its no-latency, 20-bit, 1-Msample/s LTC2378-20-1 *(Fig. 2)*. The SAR ADC has an internal clock, but it requires external references, which can range from 2.5 to 5.1 V. Normally, it operates from a single 5.5-V supply.

For power-critical applications, though, it can be operated down to 2.5 V, where it consumes a maximum of 21 mW. To minimize power consumption, the converter automatically powers down between conversions. The power reduction scales with sampling rate.

Another approach to power reduction is to use the device's differential input with single-ended signals. For circuit designers who choose this digital gain compression (DGC) on the LTC2378 and other Linear Technology SARs, the first amplifier is configured as a unity gain buffer and the single-ended input signal directly drives the high-impedance input of the amplifier.

DGC requires the full-scale input swing to be limited between 10% and 90% of the $\pm V_{Ref}$ analog input range. The internal driver then can be powered off a single positive supply. The LTC2378's data output is serial via a daisy-chainable, SPI-compatible (serial peripheral interface) bus that supports 1.8-, 2.5-, 3.3-, and 5-V logic levels.

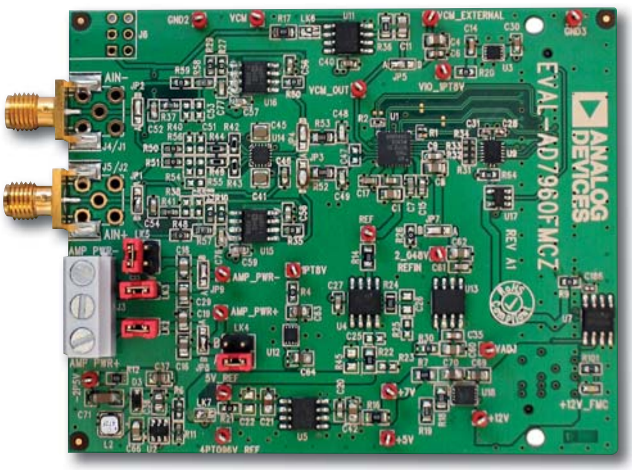
At roughly the same time that Linear brought out the LTC2378, Maxim Integrated announced product availability for the MAX11156 *(Fig. 3)*. This 18-bit, no-missing-codes SAR ADC samples at 500 ksamples/s with its reference and reference buffer built in, but still squeezes into a 3- by 3-mm thin dual-inline flat package (TDFN). "No missing codes" implies that as the input voltage is swept over its range, all output code combinations will appear at the converter output.

The tiny package saves at least 70% board space over competing solutions, according to Maxim. The company also notes its "Beyond-the-Rails" technology, meaning it can handle a ±5-V input signal while operating from a single positive 5-V power rail.

Beyond these specs, Maxim touted the MAX11156's monotonic transfer characteristic, fast settling time, and lack of latency. The ADC's typical dc performance is ±0.5-LSB differential non-linearity (DNL) and ±2.5-LSB integral non-

HIGHEST-PERFORMANCE SAR ADCs INTRODUCED IN 2013

Supplier	Linear Technology		Maxim Integrated	Texas Instruments	Analog Devices
Part number	LTC7378-20	LTC2338-18	MAX1156	ADS8881	AD7960
Resolution (bits)	20	18	18	18	18
Maximum sample rate (kbits/s)	1000	1000	500	1000	5000
I/O type	SPI	SPI	SPI	SPI	Serial LVDS
Differential nonlinearity (± LSB)	–0.5, +0.5	–1, +1	0.5 (typical)	–0.99, +1.5	–0.99, +0.00
Integral nonlinearity (± LSB)	–2, +2	–4, +4	2.5 (typical)	–3, +3	–2, +2
SNR (dB)	101 (minimum)	93.5 (mininum)	91.5 (mininum depends on reference mode)	98.5 (mininum)	95
SINAD (dB)	101 (mininum)	93 (mininum)	93 (mininum depends on reference mode)	98 (mininum)	94.5
Power (mW)	25 mW (maximum)	56 (maximum at 1 Msample/s)	38.5 or 26.5 depending on reference mode	7.2 (maximum at 1 Msample/s)	76.4 (maximum)
Unit price (per/1000)	$29.50	$29.10	$16.90	$19.95	$31.00



4. The Analog Devices AD7960 PulSAR ADC supports the company's high-precision, 18-bit, 5-Msample/s, low-power, data-acquisition signal chain.

linearity INL. Its ac performance is 94.6-dB signal-to-noise ratio (SNR) and –105-dB total-harmonic distortion (THD). For multichannel applications, multiple devices can be paralleled via its SPI-compatible serial interface. Pricing for the MAX11156 starts at $16.90.

Later, in September, Linear Technology also introduced its 18-bit, 1-Msample/s, no latency LTC2338-18 ADC with conversion speeds from 250 ksamples/s to 1 Msample/s. Operating from a single 5-V supply, it has a wider (±10.24 V), fully differential, bipolar input range. Its data sheet SNR is 100 dB, and its THD is –110 dB There also is an internal 2.048-V (20 ppm/°C max) reference and reference buffer. An input divider network scales and level shifts the input signal, eliminating complicated circuitry required to directly interface true bipolar signals. I/O is via a SPI bus.

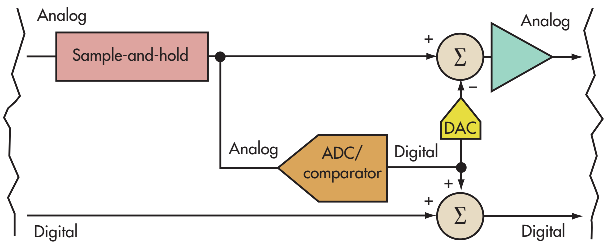
Linear anticipates a pin-compatible 16-bit and 18-bit family with pseudo-differential true bipolar inputs (LTC2328-18). The proprietary internal reference buffer maintains less than 1-LSB error during sudden bursts of conversions, enabling true one-shot operation after lengthy idle periods. These ADCs operate from a single 5-V supply and consume just 50 mW at 1 Msample/s. Power further reduces linearly at slower sample rates. A shutdown mode dissipates only 300 μW when idle.

Supporting the new part, Linear's DC1908A demonstration board enables easy evaluation of the LTC2338 family in con-

ONLY TI ADDED NEW PIPLEINE AND ΔΣ ADCS IN 2013

WHILE NEW SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) popped up all year with remarkable new levels of precision and conversion rates, there was less activity in the world of pipeline and delta-sigma (ΔΣ) architectures. In fact, up to the middle of October, only Texas Instruments was announcing new non-SAR devices.

In the first stage of a pipelined ADC, the sample-and-hold (S/H) samples the analog signal, and the flash ADC converts it to an M-bit digital code *(Fig. 1)*. This code represents the most significant bits (MSBs) of the ADC's final output. The same code is fed to the digital-to-analog converter (DAC), which converts code to an analog voltage. This voltage is subtracted from the voltage held by the S/H. The next stage in the pipeline samples and converts the resulting voltage. The number of stages depends on the required resolution and the resolution of the flash ADCs used in each stage.



1. In the first stage of a pipelined ADC, the S/H samples the analog signal, and the flash ADC converts it to an M-bit digital code. The same code is also fed to the DAC, which converts it to a voltage that is subtracted from the voltage on the S/H. This process is repeated down the pipeline.

ΔΣ ADCs feature a ΔΣ modulator and a 1-bit DAC *(Fig. 2)*. The ΔΣ modulator consists of an analog integrator and a comparator, with feedback through the DAC. After the DAC's output is subtracted from the analog input signal voltage, the resulting difference voltage is fed to the integrator and the comparator. The other input to the comparator is a reference voltage. The output of the comparator drives the DAC.

The process is clocked at a very fast oversampled rate, although the actual quantization time is comparatively long because the binary output stream from the comparator is a serial succession of ones and zeros. The ratio of ones to zeros is a function of the input signal's amplitude. In the final step, a binary output representing the value of the analog input is obtained by digitally filtering and decimating this stream of ones and zeroes.

In early January, TI announced a new pipeline-architecture device, the eight-channel, 12-bit, 100-Msample/s ADS5295. Target applications include

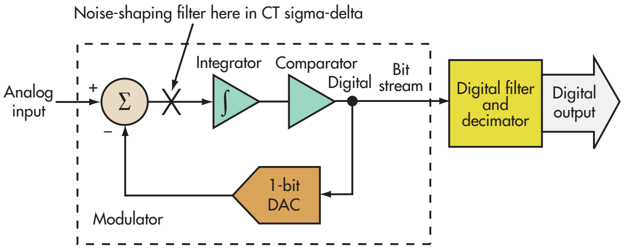
junction with the DC590B (QuikEval) or DC718C (PScope) data collection boards. The fully differential LTC2338-18 and pseudo-differential LTC2328-18 families are available in small MSOP-16 packages in commercial, industrial, and automotive temperature grades. Pricing begins at $29.10 in 1000-piece quantities.

Also in September, Analog Devices introduced its 18-bit AD7960 PulSAR ADC with 5-Msample/s throughput *(Fig. 4)*. ADI says the device targets low-power signal chains, multiplexed systems such as digital X-ray, and oversampling applications including spectroscopy, MRI gradient control, and gas chromatography. The AD7960 also achieves its 5-Msample/s performance while consuming only 39 mW. It boasts ±0.8-LSB INL and (99-dB SNR) at full throughput and a noise floor (22.4 nV/√Hz) relative to full scale.

Meanwhile, ADI's AD7961 16-bit PulSAR ADC achieves excellent SNR performance (95.5 dB) and INL (±0.2-LSB INL) at 5 Msamples/s. I/O is not via a SPI bus but by means of a 300-MHz, low-noise low-voltage differential signaling (LVDS) interface.

Finally, Texas Instruments launched its 18-bit SAR ADS888 over the summer. The unipolar, no-latency ADC available operates with a 2.5-V to 5-V external reference, which can be higher than the supply voltage, offering a wide selection of signal ranges without additional input signal scaling. The reference voltage setting is independent of, and can exceed, the analog supply voltage.

REFERENCE
"Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs," Maxim Integrated, www.maximintegrated.com/app-notes/index.mvp/id/1080



2. Sigma-delta ADCs employ a sigma-delta modulator and a 1-bit DAC. The DAC's output is subtracted from the analog input signal voltage, and the resulting difference voltage is fed to the integrator and the comparator, which relates the difference to a reference voltage. The binary output stream from the comparator is a serial succession of ones and zeros whose ratio is a function of the input signal's amplitude. In the final step, this stream is digitally filtered and output.

ultrasound, instrumentation, and communications. Its low power consumption and integrated multiple channels in a compact package make it attractive for very high-channel-count data acquisition systems. Output is via one or two wires of low-voltage differential signaling (LVDS) pins per channel.

At high sample rates, the two-wire interface helps keep the serial data rate low, allowing the use of low-cost FPGA-based receivers. Tight channel matching is accomplished by an internal reference. A low-frequency suppression mode, digital filtering options, and programmable mapping functions are also provided internally. There are low-pass, high-pass, and band-pass digital filter options too, as well as filters to remove dc-offset. Unit pricing is $70 in quantities of 1000.

In May, TI announced the ADS4449, a four-channel, 250-Msample/s pipeline device that enables receiver systems to support up to 125 MHz of instantaneous bandwidth in applications that must accommodate extremely small footprints such as multiple-input multiple-output (MIMO) basestations and munitions guidance devices *(Fig. 3)*. TI also expects the ADC to find application in electrically scanned array (AESA) and other phased-array radars. Unit pricing is $199.85.

On the ΔΣ side, last March, TI introduced a converter for automotive applications such as battery monitoring systems in hybrid electric/electric vehicles (HEV/EVs) and for fuel or oil-pressure sensing. The 16-bit, 860-sample/s ADS1115-Q1 integrates a voltage reference, a programmable gain amplifier (PGA), a multiplexer, and an oscillator. It also has the industry's only integrated programmable comparator, which makes it easy to implement over-voltage or under-voltage threshold monitoring. Unit pricing is $2.60.

And yes, you read that correctly. Three different ICs were reported with at-introduction "budgetary" pricing for 1000-unit quantities of, respectively, $70, $200, and $2.60 per unit. All devices came from the same supplier. The variation takes some getting used to. Consider budgetary pricing values to be indices of development costs versus potential sales volume. ■

3. The Texas Instruments ADS4449 four-channel, 250-Msample/s pipeline device enables receiver systems to support up to 125 MHz of instantaneous bandwidth in applications that must accommodate very small footprints such as MIMO basestations and munitions guidance devices.

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VICTORIA FRAZA KICKHAM | DISTRIBUTION EDITOR | victoria.kickham@penton.com NOVEMBER 7, 2013

Cost Reduction Still Reigns In Supply Chain Circles

Buyers still want it all from distributors—global support, inventory optimization, supply chain visibility, and more. But partnership is playing a key role in delivering those services to manufacturing customers.

ENGINEERS AND PROCUREMENT professionals at manufacturing organizations increasingly rely on distributor services to get their jobs done. Getting the parts and solutions they need on time, every time, is vital in the effort to bring end products to market faster. As a result, many customers agree they will rely on distributors for a more mutually supportive relationship in the years ahead.

Connie Wan, vice president global procurement and Asia supply chain for electronics manufacturing services (EMS) provider SMTC, says she will rely on her company's top-tier distributors for more over the next few years, pointing to service, delivery, cost, and quality as "givens" in today's

Continued on Page 38

Smaller And Faster Components Fuel The IP&E Market

The interconnect, passive, and electromechanical market remains solid. Avnet's Dave Jakubowski talks about Avnet's strategy for delivering IP&E capabilities to its customers.

AS PRICING AND lead times for interconnect, passive, and electromechanical (IP&E) components remain stable, distributors are focused on high-demand markets such as automotive and medical equipment manufacturing as they look for growth into 2014. Avnet Electronics Marketing is honing its focus on IP&E, playing up its strengths in both design and supply chain services to meet customer needs.

Avnet EM's Dave Jakubowski, vice president of IP&E supplier management, sat down

Continued on Page 40

As an example of the miniaturization trend occurring in IP&E today, ITT's Nano Miniature NDD series high-density connectors are designed to meet new requirements in high-reliability and harsh environments.

Cost Reduction

Continued from Page 37

economic climate. Looking ahead, she says those distributors that partner with customers to provide inventory management solutions, global support, and supply chain visibility tools aimed at promoting efficiency and cost reduction will be the winners in the fast-paced world of contract manufacturing, in particular.

This year, SMTC will focus 80% of its materials spend on electronic components, with about a 50-50 split between distributor and original component manufacturer (OCM) purchases. SMTC provides contract manufacturing services to customers in the industrial, medical, computing, and communications markets.

"Our first requirement is that we are looking for a partner with global support and regional support," says Wan, pointing to SMTC's manufacturing operations in North America and Asia. "In terms of service, delivery, cost—all of this is equally important to us because I believe all these factors come together. I just can't look at cost without considering delivery, for example. We look at what [distributors] can offer us in terms of service, programs, and supply chain solutions."

PARTNERS IN SUCCESS

As evidence that the word "partner" is becoming more important in this equation, a 2012 survey by international consulting group KPMG found that manufacturing organizations are more likely than their peers in other industries to focus on supplier relationship management and other tasks that get at the heart of the customer-supplier partnership.

The survey of 585 procurement leaders from across industry sectors showed that 76% of manufacturing and consumer packaged goods companies displayed high maturity levels in supplier performance management and that 82% led in supplier relationship management. Both functions point to how active organizations are in evaluating, managing, and maintaining relationships with their suppliers.

"In the past, [EMS companies and distributors] have always worked as two separate organizations," adds Tom Reilly, SMTC's director of marketing. "As time's gone on and demand for flexibility has played a key role, these two organizations have intertwined and now operate within each other's organizations to support each other and to be more flexible and more responsive to the customer. Customers really benefit from that synergy that the distributors and contract manufacturers provide."

"We look at what [distributors] can offer us in terms of service, programs, and supply chain solutions," says Connie Wan, vice president global procurement and Asia supply chain for EMS provider SMTC.

Wan points to inventory as a case in point. Helping customers optimize their inventory, improve working capital, and order materials just-in-time are key distributor services that can help make manufacturers more nimble in serving their customers' needs. There's no one-size-fits-all solution when it comes to providing such services, however, which is why customization is becoming a key attribute among leading distributors.

"Many distributors can tailor a model to fit your operation," she explains, noting that in China, in particular, it's common practice for distributors to place a third party on the customer's site to manage inventory and ensure a seamless flow of product to the plant floor. "This is something distributors can do—especially global providers."

COST REDUCTION

For many distributors, cost-reduction remains an underlying theme behind the many services they provide. The idea is that they bring important strategies to the table that help customers produce products as efficiently and cost-effectively as possible. A 2013 study by the Hackett Group, a consulting firm, underscores the importance of cost reduction strategies, noting that among procurement organizations, reducing purchased costs remains at the top of the list of performance-related concerns.

The issue has escalated in the last year, the researchers say: "for better or worse, cost reduction is king," according to the firm's *2013 Key Issues Study—Procurement*. Seventy-seven percent of companies surveyed by the Hackett Group listed "reducing supply chain costs" as either an "important" or "extremely important" issue this year, for instance.

SMTC's Wan agrees with the emphasis on cost reduction strategies and says this is a place where supplier partnership takes on a crucial role. Distributors can bring much to the table, including a strong line card, solid vendor relationships, and negotiating power all wrapped up into their service offering. But she says it's also incumbent upon the manufacturing organization to do its part to make cost-savings a reality.

"This is something we have to work together on," she says, pointing to SMTC's efforts to measure and manage distributors as a key part of the process. "We have to do our work. I rely on my global procurement team because they are experts in the marketplace. Our procurement teams in North America and Hong Kong work very closely with our suppliers to bring in cost-reduction actions.

"Usually when you talk about [reducing costs], we develop a plan with our


EXIT

partners. Once a plan is in place, our experience is that we have a pretty good outcome."

Saving time is important, too. More distributors are investing in technology tools that provide customers greater visibility into the ordering and purchasing process. Wan says this is especially useful when it comes to new product introductions.

"This is very helpful, especially in the design stage," she explains, pointing to how quickly new products are introduced into the market today. "Visibility is important. If you can log on, refresh your parts, find inventory and pricing, and place your order online—that's an important tool. It's definitely an important investment for [distributors]."

Smaller And Faster

Continued from Page 37

with *Global Purchasing* to discuss market trends and Avnet's strategy to build business in a steady marketplace:

GLOBAL PURCHASING: What is your outlook for the IP&E market for the rest of 2013 and into 2014?

DAVE JAKUBOWSKI: The analysts have really been [predicting] a flat to slightly up market, and that's consistent with what we're seeing. I don't see anything coming down the pike that would change our opinion of that.

GLOBAL PURCHASING: Are particular segments of this market performing better than others?

JAKUBOWSKI: Yes. The automotive market is quite healthy. Auto sales in the Americas have been pretty strong. Across the portfolio of IP&E, it's strong. That's because the infotainment involved in cars today, with GPS, Bluetooth, etc., lends itself toward IP&E products. As I speak to each of our suppliers, that's typically the first thing I hear—that the automotive space [continues to show strong demand].

Medical markets continue to be very consistent, and lighting markets continue to be encouraging, as well.

We also see opportunities in commercial air. There is a lot of investment going on in that space. What we see that ties into the IP&E space is the density [and] miniaturization [trends] from an interconnect perspective. In this business, they are always trying to take weight out of the airplane. A number of our suppliers have content [that can address that issue].

GLOBAL PURCHASING: What are customers in this segment demanding most from their distributors today?

JAKUBOWSKI: Design chain and supply chain solutions. We have an opportunity to see a lot of designs early on because of the semiconductors on our line card, so we're using that leverage to

"Everything has to be faster and smaller today, and we're also seeing that in high-reliability and military applications as well," Avnet EM's Dave Jakubowski says of today's IP&E market.

get an in to the IP&E products early in the cycle. [Customers] are looking for engineering support, for suggestions on design, and our line card is very rich. We have an opportunity to show customers two or three options to solve a problem. That's really very consistent with what we do every day.

[Customers are also looking for] new technologies and supplier training, so it's important to be well versed on the new solutions that are out there. We have specific resources to help with this. We have some dedicated medical resources, lighting resources, and we've invested in a lighting lab in Arizona that offers value-add for that product segment.

As products get into production we're asked to provide an array of value-added services, including managing and forecasting, inventorying product ahead of forecast, and so forth. And again, that's consistent with what we do every day for customers.

GLOBAL PURCHASING: What are you seeing in terms of product innovation?

JAKUBOWSKI: We love it when innovation comes out in IP&E. We're excited when the new widget comes out and we can promote that. Speed is really [driving much of the innovation]. From an interconnect perspective, think about some of the high-end data communication, storage, and networking applications. It's the high-speed data transfer that's required from an interconnect perspective, whether you're talking about board to board or board to chassis. That's pretty exciting, and there are some decent ASPs [average selling prices] in that space. Again, this gets back to early involvement in the design chain, where you can get rewarded from suppliers by identifying that opportunity early on. Everything has to be faster and smaller today, and we're also seeing that in high-reliability and military applications as well.

GLOBAL PURCHASING: Are you seeing any supply chain challenges in this product category?

JAKUBOWSKI: Lead times have been very manageable over the course of a number of months. For a whole year there has been very little disruption in the supply chain. It has been very consistent.

Distributors Look To Medical Markets For Growth In 2014

As the world market for consumer medical devices grows, distributors are sharpening their focus on medical electronics customers.

MOMENTUM IS BUILDING IN the medical electronics market, especially the drive to develop portable medical equipment for consumers. Future Electronics is one distributor poised to capitalize on that growth, with 10% of its roughly $7 billion in sales going to medical market customers today. Company leaders say that figure will rise considerably in the years ahead.

"There's a significant opportunity in this marketplace," says Future's executive vice president Lindsley Ruth. "It's still an area where there's a lot of innovation going on."

BY THE NUMBERS

Such observations are in line with new data showing that the market for consumer medical devices is poised for steady growth through 2017.

According to an October report from market researcher IHS Inc., global revenue for consumer medical devices will rise 4% this year to $8.2 billion, followed by 5% to 9% increases over the next five years *(see the table)*. Most of that revenue will stem from growing demand for hearing aids, but other equipment such as blood glucose meters and blood pressure monitors will also play a role, IHS says.

Distributors and analysts agree that an aging population and a rise in lifestyle-related diseases such as high blood pressure and diabetes are fueling market demand. All of those factors increase the need for health monitoring devices that can give patients and care givers greater flexibility and control over a wide range of conditions—a boon to distributors that specialize in providing electronic components and systems to power the devices.

"In a [relatively] flat overall market, we've seen better than average growth" in medical electronics, explains Faris Aruri, vice president of corporate marketing for Massachusetts-based Sager Electronics. He points to portability as a key factor driving innovation in the market.

"There's a significant opportunity in this marketplace," says Future's executive vice president Lindsley Ruth. "It's still an area where there's a lot of innovation going on."

"You see people wearing [medical devices] to test their blood after every meal, for example," explains Aruri, adding that medical markets represent about 16% of Sager's sales. "I just don't see this [market] slowing down."

REGIONAL DEMAND VARIES

As with other industries, time-to-market is accelerating in medical electronics, so customers are looking for supplier partners that can help them develop better products even faster than in the past. As a result, they are placing greater dependence on distributors for design assistance, inventory management, and product lifecycle management, Ruth says. These global trends reflect increased medical electronics business in just about every region, with design innovation concentrated in the Americas, Germany, Switzerland, and China, he adds.

GROWTH IN CONSUMER MEDICAL DEVICES	
2012	$7.9 billion
2013	$8.2 billion
2017	$10.6 billion

Courtesy of IHS Inc.

End-market demand for specific products varies by region, though portable medical devices of all kinds are in demand everywhere. The IHS study points to China, India, Russia, and Africa as regions experiencing high growth in hypertension and other lifestyle-related diseases, for instance, which is creating greater demand for monitoring devices in those populations.

Asia-Pacific is leading the way for growth in personal care devices such as activity monitors, body composition analyzers, and heart-rate monitors, the study shows. And among countries, Denmark and the United Kingdom are leaders in implementing telehealth—the remote supervision of health conditions via monitors and compatible devices.

Ruth agrees that demand is widespread, calling the portable medical devices market "a massive market that's still in its infancy." He points to a growing desire for in-home care in developed countries, for example, and increasing need for a wide range of products in under-developed regions.

"Third-world demand is enormous for even the most basic devices," Ruth explains. ■

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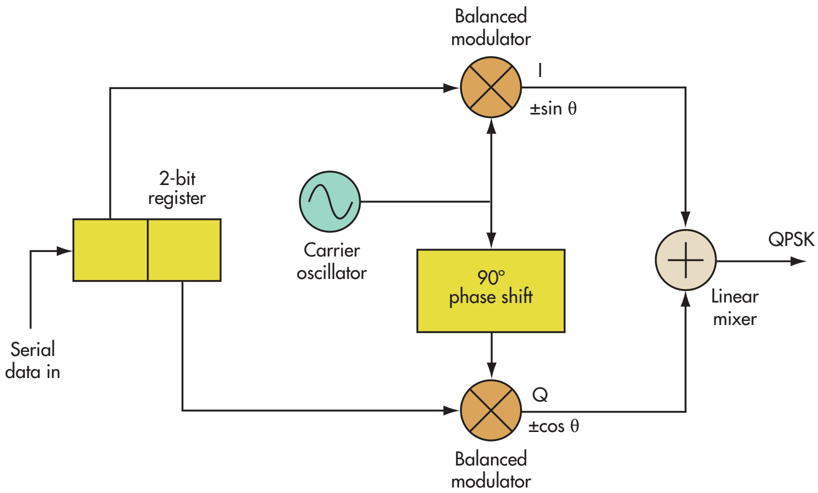
Understanding Error Vector Magnitude

This measure of modulation quality may be a better predictor of wireless reliability than BER.

Error vector magnitude (EVM) is a measure of modulation quality and error performance in complex wireless systems. It provides a method to evaluate the performance of software-defined radios (SDRs), both transmitters and receivers. It also is widely used as an alternative to bit error rate (BER) measurements to determine impairments that affect signal reliability. (BER is the percentage of bit errors that occur for a given number of bits transmitted.) EVM provides an improved picture of the modulation quality as well.

EVM measurements are normally used with multi-symbol modulation methods like multi-level phase-shift keying (M-PSK), quadrature phase-shift keying (QPSK), and multi-level quadrature amplitude modulation (M-QAM). These methods are widely used in wireless local-area networks (WLANs), broadband wireless, and 4G cellular radio systems like Long-Term Evolution (LTE) where M-QAM is combined with orthogonal frequency division multiplexing (OFDM) modulation.



1. This QSPK modulator uses the 2-bit input words to switch phases in the balanced modulators to produce both ±sinθ and ±cosθ signals that are summed to create the output.

DIGITAL MODULATION OVERVIEW

Digital modulation methods convert bit voltage level transitions and patterns into sine wave carrier variations. The most basic forms of digital modulation are amplitude shift keying (ASK), frequency shift keying (FSK), and phase shift keying (PSK). ASK represents bit variations as different carrier amplitude levels. FSK represents bit variations as two different carrier frequencies. PSK translates the bit variations into two different carrier phases, usually 180° apart.

These basic methods are widely used in simple wireless systems. However, most modern wireless systems use multi-level modulation schemes to transmit higher data speeds into limited bandwidth channels. These methods use more two or more different carrier conditions called symbols to represent multiple bits that deliver more bits/Hz of bandwidth. The most common examples are M-PSK and M-QAM.

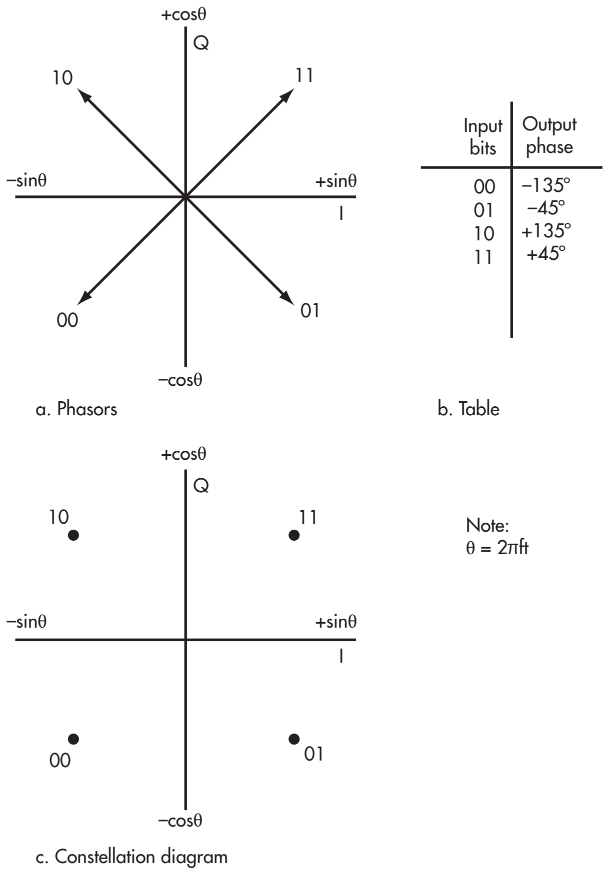
M-QAM uses a combination of both amplitude and phase to represent multiple-bit words. One popular modulation scheme, QPSK, transmits two bits per symbol. This is also known as 4-QAM. With 2 bits, four symbols are can be generated. Each 2-bit code modulates a sine or cosine carrier in a balanced modulator or mixer to produce an in-phase (I) or quadrature (Q) signal *(Fig. 1)*.

These analog I and Q signals (+sinθ, –sinθ, +cosθ, and –cosθ) are combined in a linear mixer to produce the final output. Mixing these I and Q signals produces four possible outputs, represented as phasors *(Fig. 2)*. The constellation diagram sums up all the necessary characteristics of a QPSK signal and is the primary graphic used in presenting and analyzing M-QAM signals.

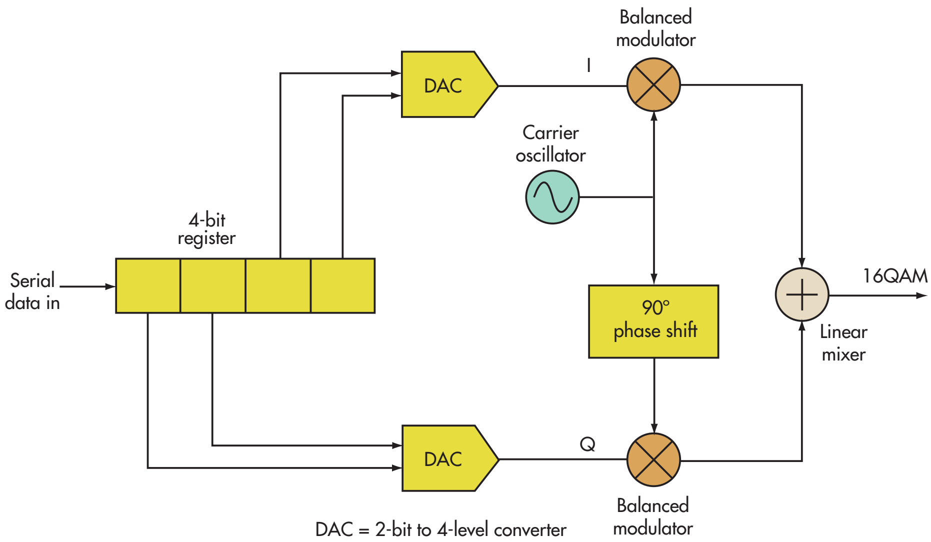
This technique can also be used to produce even higher levels of modulation like 16-QAM where each 4-bit code group generates one of 16 different symbols *(Fig. 3)*. A specific carrier amplitude and phase represents each 4-bit word *(Fig. 4)*. This technique is readily extended to even higher levels such as 64-QAM, 256-QAM, and 2048-QAM. All of these methods increase the data rate in a given channel bandwidth with higher spectral efficiency.

8-PSK uses eight different phase shifts 45° apart to represent 3-bit code groups from 000 to 111 *(Fig. 5)*. Each specific phase corresponds to an assigned 3-bit code group. A 16-PSK system is similar but uses 16 phases 22.5° apart, each phase representing a 4-bit code group. These methods provide spectral efficiency in that more bits of data can be transmitted in a limited bandwidth.

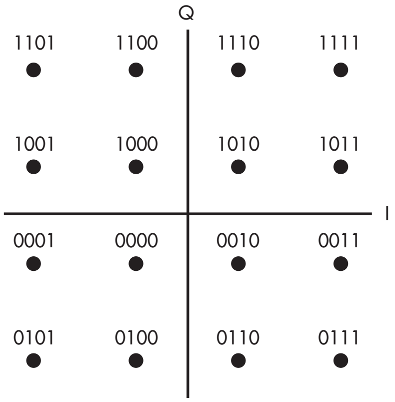
The main problem with such multi-phase, multi-level systems is that circuit imbalances, unintended phase shifts, amplitude differences, and noise distort the signal and therefore introduce errors. A phase shift and/or amplitude error means that the signal is interpreted incorrectly leading to bit errors and an increase in the BER. The greater the number of phase shifts or phase-amplitude symbols used, the more likely there will be errors due to sig-



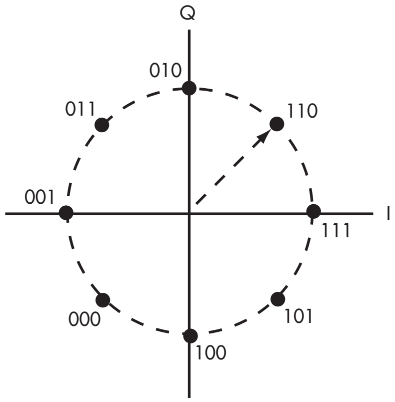
2. The QPSK signal can be expressed in several ways including phasors (a), a table (b), or a constellation diagram (c).



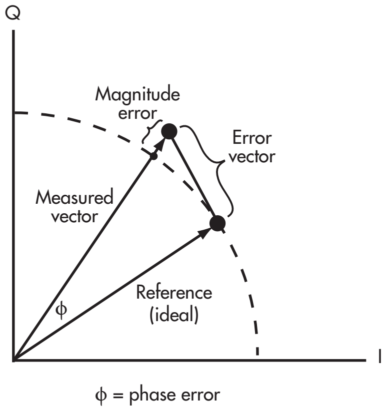
3. The 16QAM modulator uses digital-to-analog converters (DACs) to translate 2 bits of the four input bits into four amplitude levels. The four amplitude levels produce multiple amplitude and phase shifts in the balanced modulators that are summed to produce the output.



4. The constellation diagram shows the end points of the invisible phasors. Sixteen different phase and amplitude combinations are produced, one for each 4-bit code.



5. All phasors in an 8PSK signal have the same amplitude as defined by the circle in the constellation diagram. The phase position represents the codes.



6. The difference between the positions of the ideal or reference phasor and the actual generated or received phasor is the EVM.

nal impairments. For instance, 8-PSK is less susceptible to errors and thus more reliable than 16-PSK. QPSK is less susceptible to errors than 64-QAM under the same conditions.

EVM DEFINITION

EVM is a figure of merit for modulation accuracy. It provides a way to measure and evaluate multi-level, multi-phase modulation methods like M-QAM and M-PSK. EVM considers all of the potential phase and amplitude distortions as well as noise and provides a single comprehensive measurement figure for determining the quality of a circuit or product. Using phasors in the I/Q plane, EVM also illustrates the reference or ideal symbol vector location and size compared to the actual measured vector *(Fig. 6)*. The difference between the two is the EVM, which can be measured on transmitter modulator or receiver demodulator circuits.

EVM is the ratio of the average of the error vector power (P_{error}) to the average ideal reference vector power (P_{ref}) expressed in decibels. The averages are taken over multiple symbol periods:

$$\text{EVM (dB)} = 10 \log (P_{error}/P_{ref})$$

You will also see it expressed as a percentage:

$$\text{EVM (\%)} = \sqrt{(P_{error}/P_{ref})} \times 100$$

7. National Instruments' PXIe 5665 VSA performs EVM measurements automatically on transmitter or receiver circuits. A VSG is needed to produce the test signal in the case of a receiver test.

EVM MEASUREMENTS

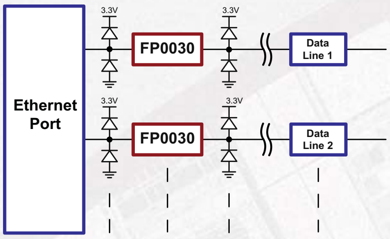
A vector signal analyzer (VSA) makes the measurements *(Fig. 7)*. A vector signal generator (VSG) is used to generate a test signal if needed. The VSA samples the signal multiple times and stores the measurements. EVM calculation software then provides the actual measurement results.

The signal to be measured is carefully demodulated and compared to the ideal or reference signal that is produced mathematically from the received signal. The difference between the reference signal and the demodulated signal is the error. The VSA will display a

Supertex Fault Protection Switches

AC low side switches with current fold-back protection that protect components from short circuit conditions

FP0030



The Supertex FP0030 is a 20V current limiting protection device. It is designed to protect Internet devices from high transient voltages.

Applications:

- *Ethernet system protection*
- *Resettable fuses*
- *High side switches*
- *Data acquisition*

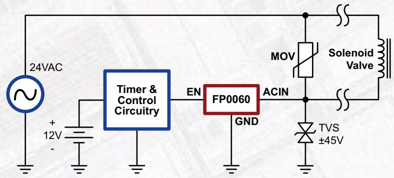
Features:

- *Low on-resistance: 4.5Ω typical*
- *Fast switching speed*
- *No external power supplies needed*
- *Simple, 3-Lead SOT-23 package*

Benefits:

- *Minimizes voltage drop to save power and maintain functionality*
- *Protects against abrupt short circuit conditions*
- *Simplifies board design*
- *Saves space, easier PCB layout*

FP0060



The Supertex FP0060 is a low voltage AC switch with current fold-back protection. It is designed to be used as an AC low side switch.

Applications:

- *Solenoid valve control*
- *AC relay control*
- *Relay replacement*
- *Resettable fuses*

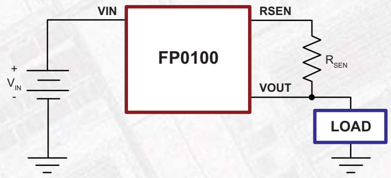
Features:

- *Low on-resistance: 4.5Ω typical*
- *Current fold-back protection*
- *Fast current fold-back response*
- *No external power supplies needed*
- *Simple, 3-Lead SOT-89 package*

Benefits:

- *Lowers power dissipation*
- *Protects against permanent damage*
- *Protects against abrupt short circuit conditions*
- *Simplifies board design*
- *Saves space, easier PCB layout*
- *Eliminates the need to replace blown fuses*

FP0100



The Supertex FP0100 is a high voltage fault protection switch with current fold-back. It is designed to protect system output power supplies against over-current or short circuit conditions.

Applications:

- *Power Supplies*
- *Fast, resettable fuses*
- *High side switches*
- *Data acquisition*

Features:

- *Up to 100V input voltage protection*
- *Low on-resistance: 4.5Ω typical*
- *Fast switching speed*
- *No external supplies needed*
- *Simple, 3-Lead SOT-89 package*

Benefits:

- *Guards downstream circuitry against overcurrent or short circuit conditions*
- *Minimizes voltage drop to save power and maintain functionality*
- *Protects against abrupt short circuit conditions*
- *Ease of use and minimized board space*
- *Eliminates the need to replace blown fuses*

constellation diagram of the modulation and multiple phasor points for each measurement. A single point is ideal, but in practice there will be a cluster of actual points around the ideal point. The more widespread the points, the poorer the EVM.

It is important to point out that the higher decibel values represent the best error-free modulation results. For example, an EVM of –40 dB is better than one of –25 dB. In terms of percentage, –40 dB converts to 1% error while 25 dB translates to 5.6% error.

EVM testing is applicable in any case where phase modulation is used, especially variants of M-PSK and M-QAM. The most common use of EVM is in testing Wi-Fi products that routinely use QPSK, 16QAM, 64QAM, and today 256QAM. Such modulation schemes are also used in WiMAX. Furthermore, QAM is the main modulation scheme used in cable TV systems based on the DOCSIS 3.1 specifications. Cellular standards like WCDMA and HSPA can benefit for EVM testing. LTE, the 4G cellular system, uses QAM extensively as well.

SIGNAL IMPAIRMENTS

A wide range of potential problems can cause poor modulation quality and the resulting bit errors. Some of these include IQ mismatch in the modulator or demodulator circuits resulting from gain and phase differences and dc offset. Frequency offset and phase noise also result in misplaced points in the constellation. AM-AM and AM-PM distortion, noise and multipath fading, and signal interference are other factors. EVM measurement does not locate the cause of the poor EVM measurement, so some troubleshooting and analysis are required.

SUMMARY

EVM is basically defined as the square root of the ratio of the mean error vector power to the mean reference power expressed as a percentage. It is a useful measurement in determining the performance and reliability of both wired and wireless systems using QAM and phase modulation. For many cases it is just as good if not better than a BER test. ed

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DAVID A. HALL | Contributing Technical Expert

Understanding Intermodulation Distortion Measurements

Don't be deterred by the theory. With a working knowledge of RF signal analyzer architectures, anyone can accurately measure IMD.

Intermodulation distortion is one of the most interesting signal analyzer measurements. Often abbreviated IMD, it is an important metric of linearity for a wide range of RF and microwave components. Fundamentally, IMD describes the ratio (in dB) between the power of fundamental tones and third-order distortion products.

THIRD-ORDER DISTORTION PRODUCTS

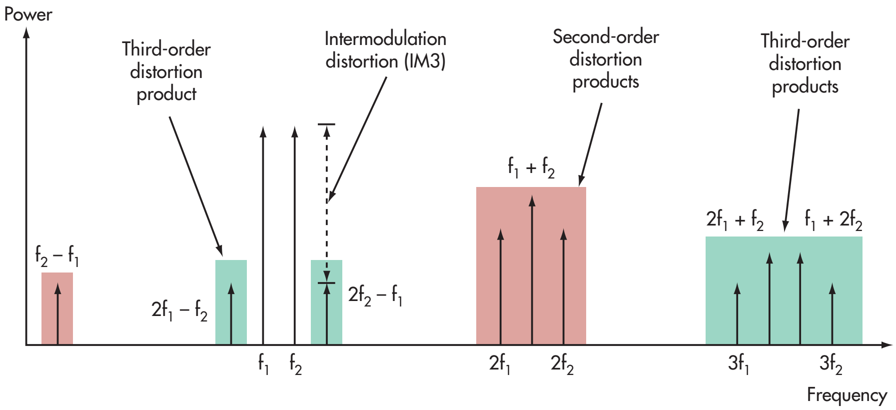
IMD measurements start with injecting a two-tone signal into a device under test (DUT). As an example, we'll consider the behavior of an RF power amplifier. A perfectly linear amplifier would produce an output signal that includes two tones at the exact same frequencies as the input signal, but at the amplified output power. By contrast, a more realistic amplifier (i.e., one with some level of nonlinearity) will produce additional signal content at frequencies other than the two input tones at its output.

For instance, it's well known that nonlinearity leads to harmonics that occur at multiples of each input tone. What's interesting in the two-tone case is that a nonlinear device will produce frequency content at an even wider range of frequencies *(Fig. 1)*.

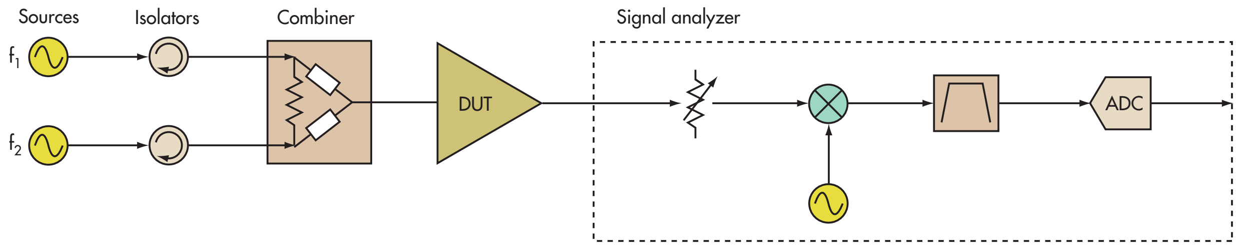
Second harmonics occur at multiples of the fundamental tones, and we can observe them at frequencies such as $2f_1$ and $2f_2$. Of course, we'll find third harmonics at $3f_1$ and $3f_2$. In addition, the system will produce second-order and third-order distortion products at every combination of first-order and second-order products. Thus, in addition to harmonics, second-order distortion products will occur at $f_2 - f_1$ and $f_1 + f_2$.

Two of the most challenging distortion products are the signal content due to third-order distortion that occurs directly adjacent to the two input tones at $2f_1 - f_2$ and $2f_2 - f_1$. IMD measurement, then, describes the power ratio between the power level of output fundamental tones (f_2 and f_1) and third-order distortion products ($2f_1 - f_2$ and $2f_2 - f_1$).

Note that IMD is problematic in RF and microwave systems for a range of reasons. In modulated signals, third-order distortion creates additional frequency content often called "spectral regrowth" in bands adjacent to the modulated signal. In a transmitter, spectral regrowth resulting from poor linearity can



1. A realistic amplifier will produce additional signal content at frequencies other than the two input tones at its output. In these two-tone cases, nonlinear devices will produce frequency content at an even wider range of frequencies.



2. Most IMD measurement setups use two signal generators that are combined with an RF power combiner. The best setups include an isolator between each signal generator and the combiner to produce the cleanest possible two-tone source.

interfere with other wireless channels. In a receiver, by contrast, it can cause out-of-band signals to obscure the signal of interest.

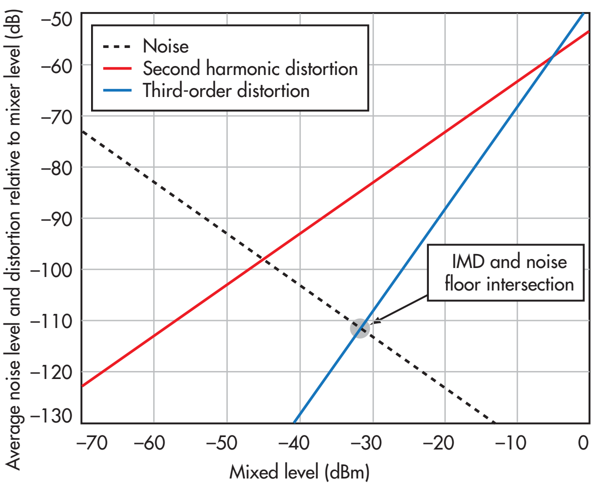
THIRD-ORDER INTERCEPT

It is important to understand that the IMD ratio greatly depends on the power level of the fundamental input tones. As a result, a related measurement known as third-order intercept (TOI) is also used to specify device characteristics. The fundamental principle of TOI is that for every 1-dB increase in the power of the input tones, the third-order products will increase by 3 dB.

So as one continues to increase the power level of a two-tone stimulus, the IMD ratio will decrease as a function of input power. At some arbitrarily high input power level, the third-order distortion products would theoretically be equal in power to the fundamental tones. This theoretical power level at which first-order and third-order products are equal in power is called the third-order intercept.

TOI, called IP3 (intercept point of the third order), is a useful specification that combines the notion of IMD with the power level at which it was measured. TOI is always calculated as a function of IMD:

$$\text{TOI} = (\text{IMD}/2) + \text{power}$$



3. The dynamic range chart is one of the most critical guides to RF signal analyzer performance. Using it, one can identify exactly how much attenuation to use to ensure the highest quality measurement.

MAKING ACCURATE IMD MEASUREMENTS

Today, many RF signal analyzers come with an IMD measurement mode that automatically detects the fundamental and third-order distortion signals and calculates both their ratio and the resulting TOI. However, the hardware configuration for the IMD measurement setup requires the most attention.

While we'll mainly focus on the signal analyzer side here, recognize that configuring the two-tone source is often a complex element of measuring IMD. Most IMD measurement setups use two signal generators that are combined with an RF power combiner. The best setups include an isolator between each signal generator and the combiner to produce the cleanest possible two-tone source *(Fig. 2)*.

For the most difficult IMD measurements, where the third-order distortion products are extremely small and the IMD ratio is high, careful attention to the RF signal analyzer settings is essential. The RF signal analyzer includes a mixer directly after its programmable attenuator. This mixer, while being an essential element to downconversion, will behave nonlinearly at higher power levels *(see "Understanding Signal Analyzer Architectures" at electronicdesign.com)*.

One might think that a simple approach to preserving the linearity of the RF signal analyzer would be to increase the amount of programmable attenuation before the mixer. Since IMD is directly correlated to input power level and attenuators reduce power level, this would allow the mixer to operate in a more linear region of operation.

While increasing attenuation would certainly reduce the IMD contribution of the RF signal analyzer, it would also affect its noise floor. If one applies too much attenuation, the third-order distortion products one is trying to measure will be undetectable because they will fall below the noise floor of the instrument.

PRACTICAL TIPS

As a result of these characteristics, the dynamic range chart is one of the most critical guides to RF signal analyzer performance *(Fig. 3)*. Using this chart, one can identify exactly how much attenuation one should use to ensure the highest quality measurement.

The inherent third-order distortion of an RF signal analyzer and its noise floor are directly related to the mixer level of the instrument. Mixer level, defined as the signal power present at the input of the first mixer, is determined by the input power at the RF connector and the amount of attenuation being used.

At the intersection of IMD and noise floor, the instrument's own inherent third-order distortion products are equal in power to the noise floor. When configuring the instrument to have a mixer level that is lower than this intersection, the results will be noise limited. By contrast, configuring the instrument to have a mixer level that is higher than the intersection point, IMD measurements will be linearity limited. Thus, maximizing an instrument's dynamic range for IMD measurements requires us to configure a mixer level that is right at this intersection point.

Note that if one doesn't have access to the instrument's dynamic range chart, identifying the ideal operating point manually is fairly straightforward. With the test signal connected to the signal analyzer, slowly begin to increase the amount of attenuation. If the power of the third-order intermodulation (IM3) products decreases with an increase in attenuation, then you know the instrument is operating in a linearity-limited region.

By contrast, if the power of the IM3 products does not change, then you know the instrument is likely in the noise-limited region of its operating range. Generally, the ideal instrument configuration is such that the configured attenuation is a few dB higher than the attenuation level where IM3 no longer changes as a function of attenuation.

PARTING THOUGHTS

Distortion measurements such as IMD and the related TOI result are some of the most interesting and important measurements that one can make with an RF signal analyzer. While the theory of these measurements might seem complex at first, one can perform accurate IMD measurements with a working knowledge of RF signal analyzer architectures. For more detailed on measurement best practices using RF signal analyzers, visit www.ni.com/rf-academy/. ed

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W. Gordon Kruberg
Explains How To Kickstart A Gumstix

Gumstix makes a range of products based around small modules called, of course, Gumstix *(Fig. 1)*. The modules speed time-to-market for designers who can now choose what processor platform and peripherals they need. The modules also use Texas Instruments' OMAP systems-on-chip (SoCs) with Arm Cortex processor cores.

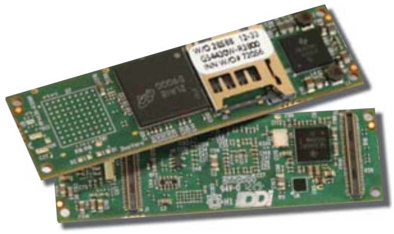
Designers can take advantage of existing carrier boards for their Gumstix module or design their own. Most design their own boards when creating new products, but Gumstix can help there too with a design and delivery tool for carrier boards called Geppetto *(see "Game Changing Geppetto Builds ARM-Based Systems" at electronicdesign.com)*.

W. Gordon Kruberg, president and CEO of Gumstix, recently discussed how his company is taking advantage of crowdsourcing and Gepetto to deliver open-source hardware designs to a wide range of users.

WONG: What is Gumstix Geppetto?

KRUBERG: Geppetto is a Web app for building custom embedded computers *(Fig. 2)*. Users can create devices by dragging and dropping the parts they need (USB ports, network connectors, or even whole computers-on-modules) onto a board. Geppetto takes care of the low-level routing while users control how all parts of the system connect. Completed designs are built at the touch of a button and ship in 15 business days.

Beginning with either a template or a blank workspace, designers drag and drop from a library of parts to create a board design. That design can be shared in a limited or completely open fashion before the decision to purchase is made. Purchasing itself can be done as an individual or by a group, or by a crowd. There are no project costs until boards are shipped. There are no engineering charges.



1. Gumstix compact modules have an SoC that runs Linux and is surrounded by a collection of peripherals that can range from Wi-Fi to Ethernet.

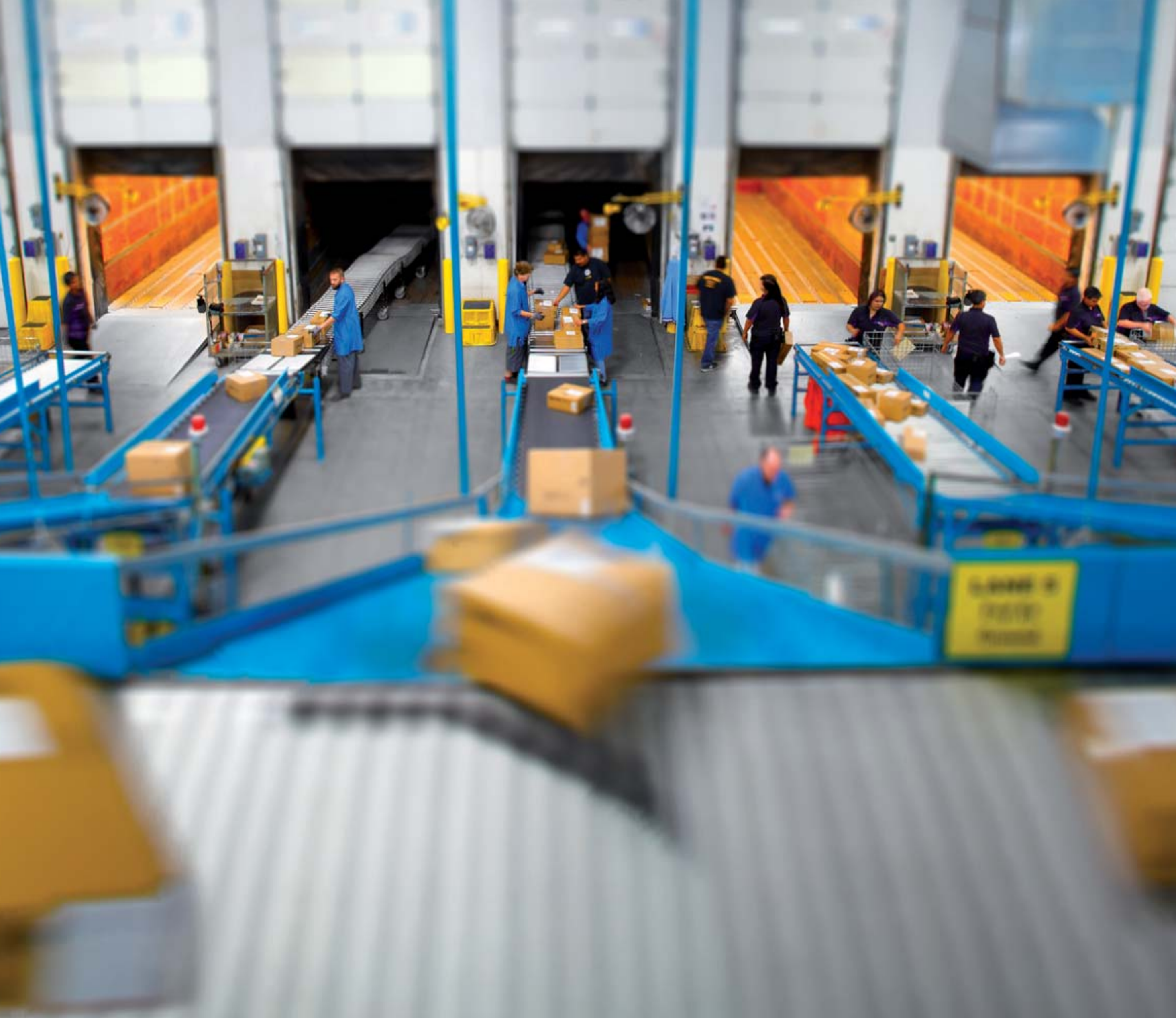
For example, to build a custom computer with an accelerometer and a touchscreen, the designer places a touchscreen and an accelerometer onto the board. The board turns red to let the user know of missing requirements, which also appear as flags. Clicking the flags identifies the next pieces of the puzzle.

A drag-and-drop later, that flag turns green to let the designer know it's done. A yellow flag means the requirement can be met by something on the board, but still need connecting. Clicking it will give flags on other parts, and users can connect them in the way that best suits their design. Repeating this process until the board turns completely green finishes the design stage of a project.

This touchscreen and accelerometer design above only took 10 minutes to complete from start to finish. If this board is ordered by the designer, the manufacturing setup cost is $1999, charged when the order is shipped. The board itself costs a little under $40 per unit ordered.

WONG: How does crowdfunding come into play?

KRUBERG: Gumstix's philosophy has always revolved around the importance of sharing, especially with open-source hardware and software. When we developed Geppetto, we gave users the option to share their designs with other users, making development faster and stronger. We also wanted to take it one step further, giving users greater advantages in sharing their designs. Now, we are offering them easier access by sharing manufacturing costs and scale. Any designer can choose to share the manufacturing costs with a limited number of users (say, the 40 other members of a robotics club) or with an undefined number of members in a crowd.



Crowdfunding has exploded in recent years as an extremely effective way to get unique ideas to a target group that may not be able to afford them. The model has been successful for everything from original series on YouTube to 3D printers to almost anything else imaginable. Crowdfunding is the perfect way for Geppetto community members, especially hobbyists, to create and share a practical idea with other interested users and to make it a reality by sharing the associated costs.

WONG: How does a Geppetto crowdfunded project get started and how do boards get distributed?

KRUBERG: Getting started on a crowdfunding campaign is almost as easy as buying any other Gumstix product. After a design is complete and added to the Gumstix catalog (as either a private, shared, or public board), a user has the option to create a community campaign instead of just purchasing it outright. A creator sets the number of days the campaign can run for, as well as the minimum number of boards needed to make the campaign successful.

Campaigns can be made public or shared only with users of the creator's choosing. Users then have the option to pledge the number of boards they want to a community campaign. Campaigns continue until their end date, even if they pass the designated threshold. Pledges are only charged if a campaign is successful, and each user pays their proportion of the setup fee, based on the number of boards they order out of the total, as well as the unit cost for their quantity of boards. All boards are manufactured and shipped within 15 business days of the campaign's completion.

WONG: What impact do you expect crowdfunding for Geppetto designs to have on the Linux, electronic design, and hobbyist communities?

KRUBERG: Crowdfunding gives Geppetto users a new and effective way to make their designs a reality while

2. Geppetto is a Web app for building custom embedded computers.

benefitting everyone in the community. The embedded Linux community will have an easy way to implement software solutions on custom hardware, without needing the typical hardware expertise, by designing in Geppetto and crowdfunding. Electronic design professionals too can get started on their designs faster and minimize their time-to-market all while building their own community around their designs.

Last, but certainly not least, we expect hobbyists to see tremendous cost savings benefits in crowdfunding. While the costs associated with a Geppetto design are a fraction of those in conventional electronic design, they might still be prohibitive for a hobbyist who has a great idea. By sharing their completed idea with the community, finding other interested hobbyists and receiving pledges, many members of the hobbyist community will now be able to distribute the engineering cost and receive a professional quality board at an incredible price.

We're so excited about the new possibilities community campaign crowdfunding brings to our users that, for a limited time, Gumstix will waive the setup fee on any campaigns that reach more than 50 pledges. Users can get started on a Geppetto design and campaign at http://geppetto.gumstix.com. ed

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W. GORDON KRUBERG, president and CEO of Gumstix, founded the company in 2003. He holds an AB degree in human biology, an MS degree in industrial engineering from Stanford University, and an MD degree from Northwestern University.

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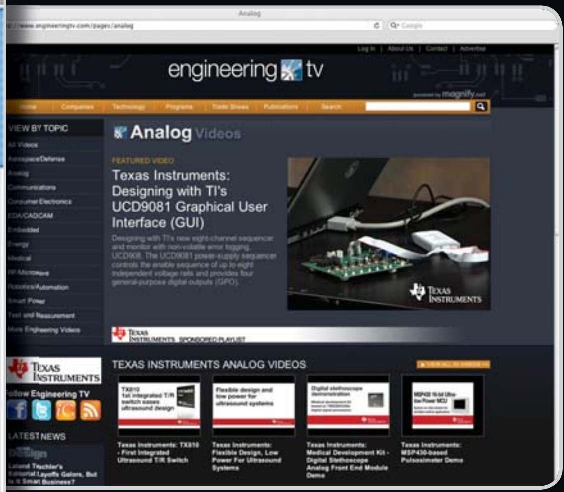

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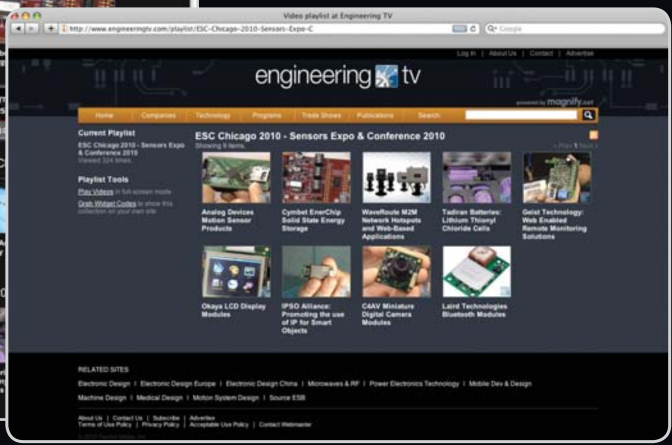

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Plan Ahead For A Successful SoC-Based PCB Design

Addressing the key factors that can affect the ability to manufacture SoC-based PCBs efficiently early in the design process will ensure that fabrication, assembly, and testing will proceed with few problems and high yield.

In the development of SoC-based (system-on-chip) circuit boards, the SoC's additional capabilities will provide abundant functional benefits. But at the same time, these capabilities can introduce additional challenges to the circuit board manufacturing process. Therefore, developing an effective plan for designing, developing, testing, and producing the final printed-circuit boards (PCBs) is good business practice.

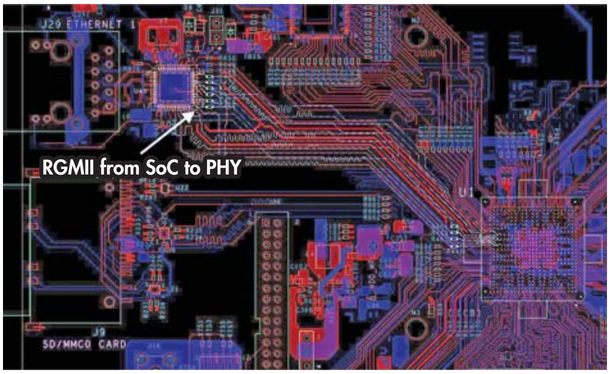
Several steps in the PCB development process include areas that allow enhancements that can improve the ease of board manufacturing and the yield rate of the production circuit boards. Many elements of the process, from the SoC itself to the design process to the end board tests, should be reviewed for improvements that can affect the PCB's final manufacturability.

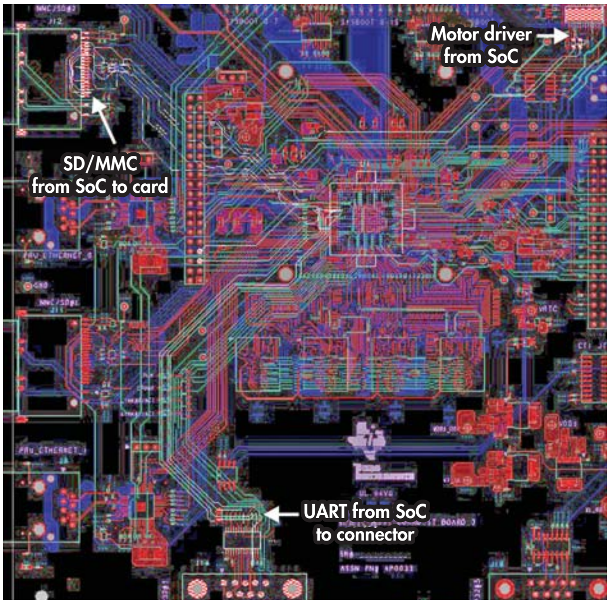
SIZE DOES MATTER

SoC devices have a certain inherent complex nature. An entire system is packed into a single silicon package the size of your thumbnail. There are many interfaces, clocks, signals, protocols, and power connections within a small physical structure.

The reduction in the size of the system does not guarantee a reduction in PCB implementation issues. In some cases, this physical reduction increases the number of challenges that will be encountered when designing the underlying PCB.

To fit so many combinations of function within the same small package, the chip's designers usually use a clever method of assigning multiple combinations of function to the same pin. On the Texas Instruments (TI) Sitara AM3358 processor,





1. The ability of the SoC to connect different sets of functional signals from the same sets of pins can create quite a difference in a board layout. These layouts show examples of the diverse differences in routing between two different implementations of the same SoC. In the example on the right, the pins are used for a UART, SD/MMC card, GPIO, and motor control. In the example above, the same pins are used for an RGMII Ethernet PHY connection.

for example, the same pin can be assigned UART, I^2C, general-purpose I/O (GPIO), Reduced Gigabit Media Independent Interface (RGMII) Ethernet, or motor drive pulse-width modulation (PWM) functions, representing only a few of the available interfaces.[1]

This use of temporal assignment of multiple interfaces on the same physical structure, the I/O cell, is a great way of developing a low-cost system solution. In many ways this can help reduce the overall system cost and take advantage of ever-shrinking silicon processes. Using I/O pin multiplexing like this can present some challenges at the PCB level, though.

Implementing a system using an SoC with a complex I/O pin multiplexing scheme presents a challenge in that the same PCB layout is not optimal for all the possible I/O pin definition combinations. Figure 1 shows the PCB layout for two different I/O selections from the same SoC. In one circuit design, a set of pins is configured for a UART, an SD/MMC card, GPIO, and motor control. In the other circuit design, the same set of pins is configured for an Ethernet bus using the RGMII type of interface.

Note that at a schematic level, there does not seem to be much difficulty changing between the two designs since it's simply replacing the end devices/circuits with the appropriate choices (such as an RS-232 transceiver versus the Ethernet physical layer, or PHY). However, when the PCB layout implementation is reviewed, a dramatic change in the requirements for the different interfaces reveals what major changes must be made to the PCB placement and subsequent routing to develop a robust circuit board. The UART, SD/MMC card, GPIO, and motor control will be routed to multiple devices that may be placed at spatially diverse positions on the PCB. In contrast, the Ethernet bus will be routed to a single device, the Ethernet PHY, which will probably be placed fairly close to the SoC.

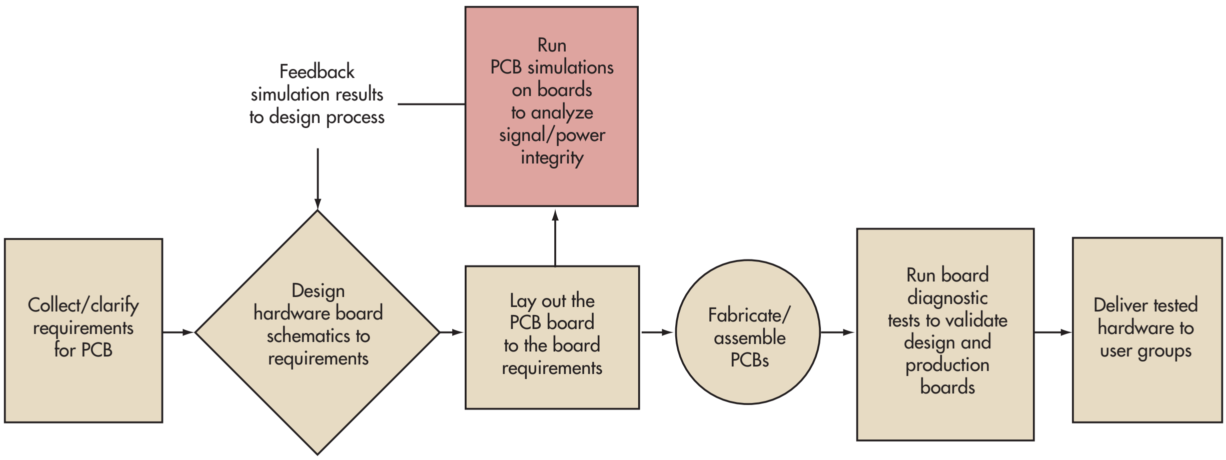
This difference in the routing of the same SoC pins depending on the interface connection reveals why there is not a single global correct way to lay out an SoC-based PCB that works for all designs. Instead, each design needs attention to such details to minimize the risk of manufacturability issues. Reference designs from the SoC manufacturer can help show pragmatic implementations of common circuit designs.

PLANNING AHEAD

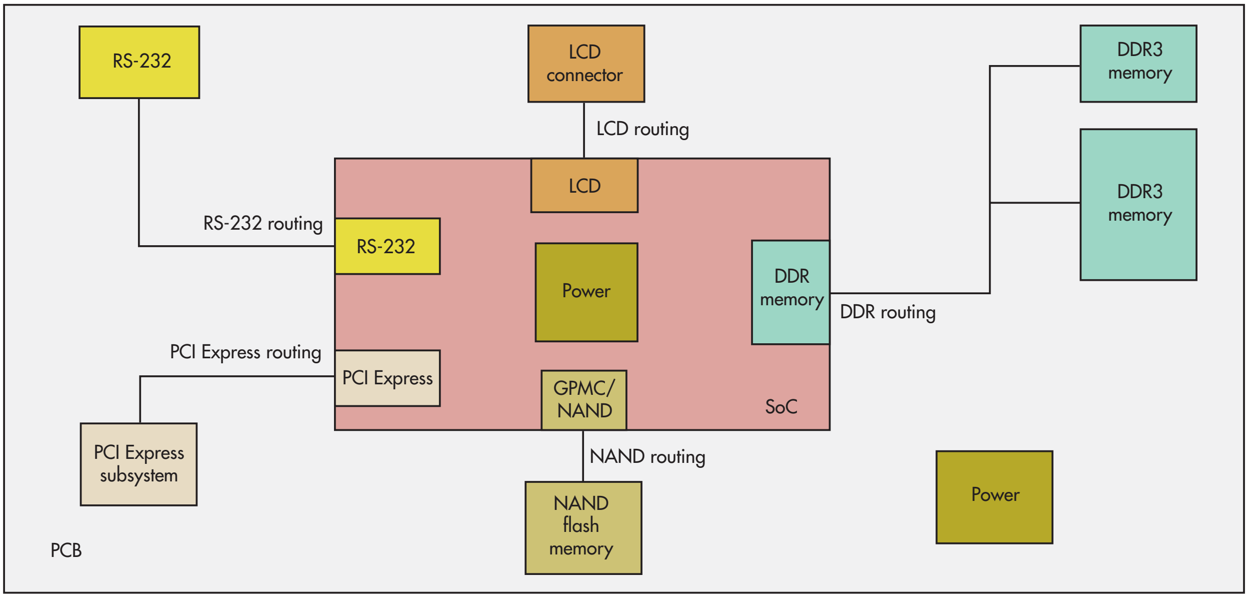
By the time the first PCBs arrive, many design issues can be checked. The process of designing the PCB in an efficient way has much to do with what items can be verified early in the design. The steps in the process can help move the high-risk items earlier in the process to give you more time to recover from possible errors in the design or implementation. However, some of the PCB design process must be carefully thought out to meet the pre-requisites of each step *(Fig. 2)*.

In a common PCB build environment, the main goal, of course, is to use the schematic design to build a tangible real PCB. Several different materials can be used to generate the circuit board. For this discussion, rigid FR-4 material is assumed to be used. The intricate physical and material characteristics of the FR-4 copper-clad glass epoxy board are beyond the scope of this article. However, these very details of the PCB material can contribute to important design decisions, starting with the requirements of the board all the way through testing and production manufacturing. As a part of the PCB requirements and design steps, it helps to understand these details because details such as copper weight and board stock insulation thickness will determine the stackup and steer the routing constraints for the board.

In some instances, it may seem easy to leave the board physical parameters to the layout person. But maintaining even a cursory knowledge of the underlying board substrate



2. This diagram shows a simplified graphical example of the type of flow in a standard PCB development process. The main steps within the process are encapsulated as the major blocks within the design flow.



3. This example shows a placement that supports optimal routing with regards to signal trace locations.

can allow better decisions that affect many items going back to certain characteristics such as how big the board can be and what devices can be placed on the PCB.

For example, FR4 material has a certain amount of flexibility across its lateral and longitudinal dimensions. If this is not addressed, then a ball grid array (BGA) the size of an SoC could result in solder ball bond failure if unforeseen mechanical stress is placed on the board. In a different way, mounting the PCB can add to issues of thermal failure and board twist/mechanical flexing depending on the enclosure/rack assembly.

Though at first view of the PCB design process, the end production board is the key metric to be seen, the use of and actual need for early prototype circuit boards is an important step in the overall PCB flow. Despite a careful view of the design activity and checklists that verify that design constraints have been met, errors in the design can slip through and show up in the final board. Therefore, early prototype boards are important for flushing out errors and misjudgments in a SoC board design.

What errors can happen when there has been due diligence during the design of a circuit board? Several things can go wrong with even the best-intentioned SoC-based circuit board design:

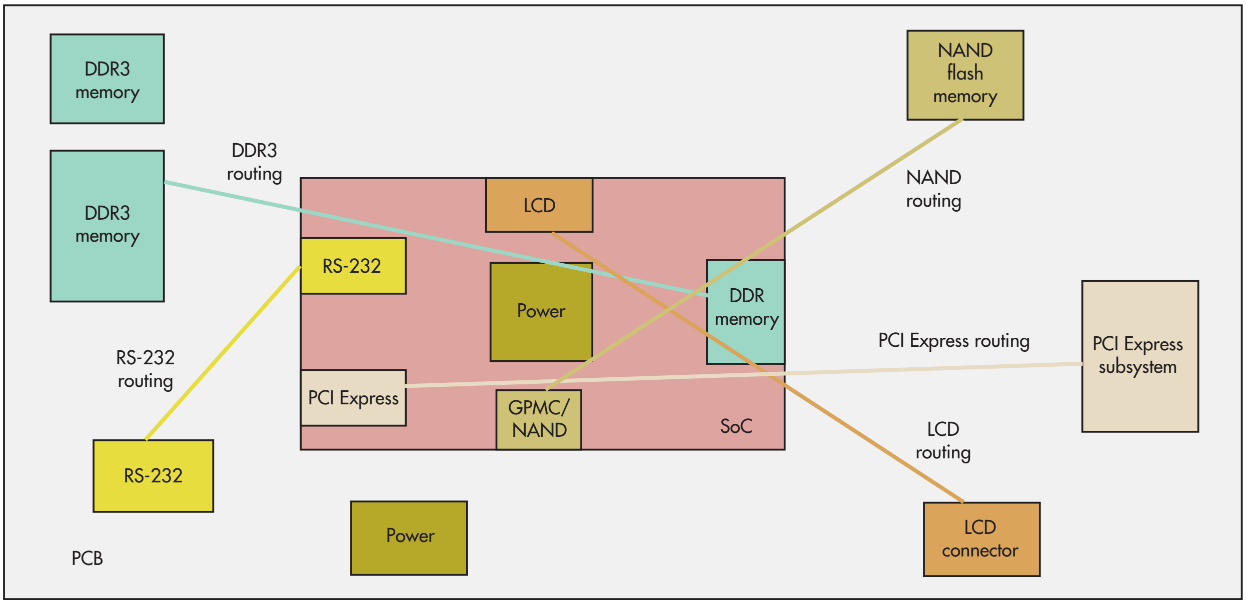
- Communication mistakes between the board designer, requirements team, layout person, or board manufacturing partner
- Too large a scope of the design leaving unhandled requirements
- Component footprint errors
- Mechanical placement errors (connector/cable clearance issues, display mounting problems, etc.)
- Misunderstanding of the board requirements
- Electrical design mistakes
- Power supply problems
- Interface signal noise problems
- Orientation of device/daughterboard connectors
- Error in the address assignment of devices
- Board configuration option functional issues
- Component availability problems
- Component revision changes by the manufacturer

ESTABLISHING GOALS

Simulation technology has improved noticeably in recent years, and tools employing it can be used to try to catch some of these types of problems. While a large effort to simulate the design, verify mechanical clearance, confirm design requirements, and think through how configuration options can minimize potential errors (and all these activities are good design practices), the increase of the design schedule to accomplish all of these steps realistically can be more than the board development constraints will allow.

It is very important to drive to clear and succinct design goals as an early part of the PCB design process. These design goals can seem general and nebulous before expounding on them during the design phase. Goals that are left vague leave an opportunity for misunderstanding, which will manifest as PCB faults that can affect the straightforward build schedule of the final PCBs.

For instance, if a particular NAND flash memory must be used, but the I/O voltage level is not clear, then the circuit may



4. This placement/floorplan will make routing more difficult and costly since it requires more physical locations for the signal traces.

be designed for supporting both 1.8 V and 3.3 V or it may be designed for a single voltage value. For seamless connection to the SoC, this I/O voltage level must be matched on the corresponding supply rail on the SoC. This can add unneeded complexity and risk to the board. When there is any doubt about requirements, reviews can clarify these questions.

Component placement upon the circuit board has huge effects on the manufacturability of the final PCB. The optimal placement of the components affects inter-device clearance, manufacturing pick and place efficiency, cable access and clearance, and soldering profile differences. This is different than the I/O multiplexing issues explained earlier, although they are often related.

Issues such as lead versus lead-free components placed next to each other can make it more difficult to set the proper soldering profile for the board. (This is less of a problem now with improvements in soldering technology.) Typically, lead-free components require a higher solder such as 250°C while lead components may require 220°C.[2] Placing these components right next to each other could affect manufacturability due to differential thermal convection. This is especially true for ultra-small BGA components (such as single gates in discrete packages) that have only a few balls for attachment and lower thermal mass.

If one particular component has rigid routing constraints, this may limit the placement of other components within a certain region. For instance, high-speed interfaces such as DDR3 require constant reference planes and effective isolation from other interfaces. This will limit placement of other devices within a certain distance of the DDR3 memory devices.

In a SoC type of design, many heterogeneous peripheral devices often must function on the same PCB. Preparing a priority-based placement analysis can help ensure a proper functioning final circuit board. Floor-planning the PCB prior to component placement helps to reveal potential routing, power, and mechanical problems.

Usually a circuit board has certain physical constraints for connector placement based on the planned uses of the PCB and the end product that it is in. Sometimes the SoC has multiple sets of I/O to which a particular interface can be mapped. Using a floor plan of the PCB can reveal better combinations of I/O mapping of the SoC pins that will provide better mechanical structures on the circuit board.

ON THE BOARD

In Figure 3, one placement will clearly provide a better board that is easier to lay out and build than the other board. The floor plan has the devices spatially optimal for routing since the locations of the appropriate SoC balls for each interface are oriented near the position of the external device on the board. In Figure 4, placement B is a floor plan that has the components placed away from the corresponding interface balls on the SoC processor. This will require routing lanes that cross each other and consume valuable board power and signal routing area. Remember, there are only so many layers to route signals and power and cost increases to gain more layers for routing.

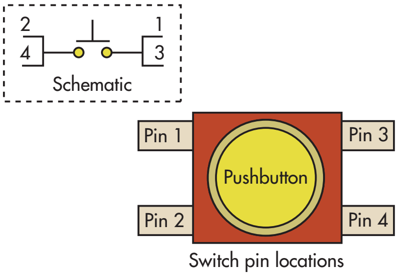
While this may seem obvious when looking at the design at this level, sometimes other board requirements such as connector placement will force non-optimal placements to occur.

Looking at the floor plan of the board can show issues that may not be intuitive when considering only the electrical connections of the schematic.

As a general rule in an SoC-based design, escaping the SoC's ball array is of primary concern, not just for signals but also for power and ground connections. If a low-cost PCB is an important constraint, then there are limitations to how the signals can be routed from all the balls on the SoC package. For instance, in a 15- by 15- by 0.8-mm package with most of the ball array populated, routing escape can be more difficult if the supporting components are placed in poor locations or at distances from the SoC that are not conducive to the planned board size.

Splitting the design into multiple boards for whatever reason can increase the complexity. If the board constraints require multiple boards, extra planning and verification are necessary to maintain signal integrity on critical interfaces as well as to ensure mechanical clearances are correct.

This is another example of using early prototypes to bolster the spatial component analysis and verify that there will not be production problems. The introduction of the second (or additional) boards to the physical construction adds another dimension where components may interfere with each other where they wouldn't on a single PCB solution.



5. This diagram shows how the pin locations of a component can be counterintuitive to the pin definitions.

PREPARING FOR CONTINGENCIES

As foolproof as modern components have gotten, it is still important to investigate the planned components for a PCB design to help minimize impact to the end board build. Some components have less than apparent packaging details. While standard packages exist for many ICs and discrete components, some packages have peculiar attributes that make them susceptible to soldering errors and other assembly errors such as non-standard pin pad geometries or assignments.

For instance, in Figure 5, the momentary pushbutton switch would appear at first glance to have pins 1 and 2 shorted together and pins 3 and 4 shorted together based on the proximity of each pair of pins. But the device schematic from the datasheet indicates that the other sets of pins are actually connected.

Using components with these types of irregularities introduces more risk into the overall PCB design flow. While the irregularity can be compensated for, it is easy to miss these details when there are so many other details to verify and check prior to pattern generation for PCB fabrication.

A major concern for manufacturability of a board rests with the component selection. As hardware board designers, we usually concentrate on the board details. But the simple details about the components such as the product lifetime of the chosen components for the design can spell disaster for a board build schedule if the availability of the chosen devices is a problem.

A worse case is if the component is no longer available with no alternative device or second sources available. The PCB then usually must be redesigned to accommodate a replacement component. Added to this redesign is the obvious concern about checking whether the new component will cause any new problems that had already been answered for the old component. An SoC-based design may have additional requirements if there is a close coupling of the SoC to some external devices.

As discussed earlier, the PCB material can also have major implications for the manufacturability of a SoC-based design. The construction of the PCB itself will be dictated by some of the overall design requirements such as cost, size, board outline, and more. Normal board constraints call for "smaller is better" when it relates to overall PCB physical size. Smaller physical size decreases the amount of space for routing traces and placing components. When considering solutions to placement and routing issues caused by any reason, simple changes such as just adding more layers to the PCB might at first seem attractive but may not be the correct answer.

Consider a 120- by 95-mm PCB with a central SoC processor that is in a 17- by 17-mm package with a 625-ball array in a 0.65-mm pitch. There will be other devices on the board, and some of them may be BGA-type packages. The major challenge in proper layout of the PCB will be the routing escape from the SoC. Depending on the number of signals actually used on the SoC for the design, routing each SoC pin to the target on the PCB may be challenging.

While the signals are one aspect to the routing job, the power distribution network (PDN) is just as important. In today's modern SoC processors, the power delivery is very important to minimize erratic runtime failures, which are difficult to diagnose. This is where one solution does not work for all implementations. If cost and schedule were no issue, then a common solution would be just to increase the layer count and use more complex and smaller via types *(Fig. 6)*.

This approach effectively compensates for the reduction in gross spatially X&Y routable area and volume (remember, routing is in 3D) when the overall board size is shrunk by reducing the physical volume of the signal and power vertical transition zones (vias) and increasing the routable Z-axis area. The downside to this is that each additional layer pair added increases the PCB cost and time.

Furthermore, the use of anything other than through-hole vias of a particular diameter and pad size will increase the fabrication steps due to the requirement to drill before fabrication

adhesion of outer layers. Also, using non-mechanical drills due to the small diameter via physical size will increase the PCB fabrication cost. The industry has improved much in this area over the last decade, but 12-layer boards with micro-vias and blind/buried vias are still not equal in cost with four- or six-layer boards with through-hole vias only.

TESTING AND THE BIG PICTURE

Each design should be evaluated separately to determine the optimal solution. For instance, the SoC will typically have a massive amount of routing running to it, and it will also demand a decent amount of power network planes, partial planes, or wide traces. Adding layers will generally help in routing escape from the SoC, but the additional cost of the PCB with the extra layers may not be tolerated from an end-cost point of view.

It's important to specify and track the specific placement and signal design constraints for the board. The very process of specifying these constraints may flush out some competing requirements that can be resolved early on. At the very least, these constraints help to guide layout from a more proactive stance in a group-type organization. This really helps to show the critical signals such as DDR3, MIPI, Ethernet RGMII, and more, as well as how these signals need to be prioritized during placement and layout to improve their traces' signal integrity.

After all, due to certain signal integrity requirements of some interfaces, a PCB physical area will have certain prime routing locations that command short distance between specific components, great reference plane locations, and faster wavefront flight times due to layer characteristics. By targeting the critical nets to occupy these prime routing locations, the resulting PCB has a lower risk of board failure due to crosstalk issues, power supply noise issues, component tolerance problems, and beyond.

Even if a design is proven to function within specification, there is no guarantee that each production unit will function within that specification. Due to the many variables associated with building a modern SoC-based circuit board, items such as component tolerance, soldering mishaps, assembly errors, PCB fabrication mistakes, layout problems, and plain human error can cause yield problems in production PCBs.

Therefore, a proper board development process that seeks high yield of final circuit boards should include some type of diagnostic testing. These tests should be run on every single production board before it is packed and shipped. SoC processor-type boards include multiple heterogeneous interfaces that all have specific functional requirements. Therefore, the diagnostic tests should include a test or series of tests for each of these interfaces. Knowing and clearly defining the requirements of the board pays big benefits here by making it easy to understand, define, and write the tests that are necessary to qualify a board for pass/no-pass status at manufacturing time.

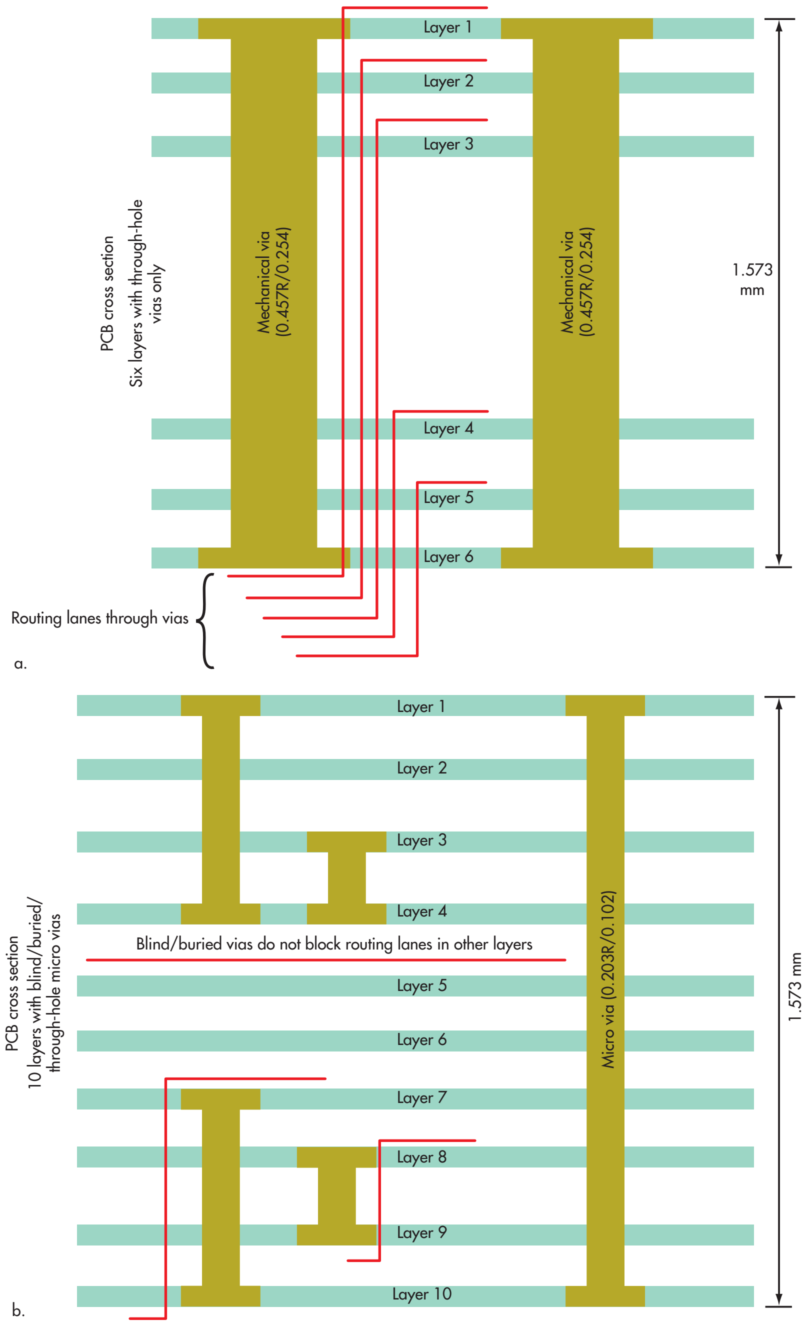
Usually the steps to developing these diagnostic tests include:

- Defining the important interfaces/power that need to be functionally tested.
- Prioritizing these tests based on circuit requirements.
- Deciding on test coverage required for each test.
- Developing the tests.
- Checking the tests on a prototype board.
- Generating the optimized run version of the diagnostic tests.

Test yield coverage can be tuned based on the known requirements and perceived risks for a particular board.

Typically, 100% test coverage of the hardware board is not fiscally feasible due to the test run time costs incurred at production time. Thus, if the design has been proven to work, seeking full hardware test coverage is not necessary at production testing due to lower inherent risk of the design.

It is best not to have the same software developers who will develop the board



6. The capability to use interior layers to route signals is an important benefit of using smaller blind and buried vias. However, this benefit should be weighed against the additional cost of the board.

SoC production software also write the diagnostic tests. At first this seems counterproductive. Since the software developers know the hardware from their work, surely this will save time and resources by using them to write the hardware board diagnostic tests. However, in reality the opposite is true.

The software designers who are very familiar with the hardware can sometimes be blinded into using the same software implementations that work in production software/firmware and placing it in the diagnostic test code. The point of the diagnostic tests is to flush out potential hardware problems. Therefore, having these tests written by someone other than the normal software development team will allow the test software to control the hardware in different ways that can and do show potential problems even before the production software is loaded and run.

This is another area where having early prototype boards is very important since they can be used for early diagnostic test development, which in turn improves the hardware design since the early tests can flush out early errors in the hardware design or incorrect implementations of the board requirements. The early prototype boards also give the diagnostic tests an additional benefit of being troubleshooting guides for the software team when they finally receive fully functional and tested circuit boards since they can refer to these tests if they run into problems during their development.

The tests are typically written with no operating system to make sure they have fewer dependencies and provide simpler hardware management techniques. The final step to the diagnostic test development is to optimize the tests into runtime executable code that can be run on each production board.

It is crucial not to skip this step since the per-unit test time should be minimized for production boards since each second of test time costs a certain amount. Nonetheless, diagnostic testing is worth the cost of development and execution because it improves board yield. Also, overall board manufacturability is improved since important test time data about the design can be observed and sent to the board designer for updates to the next version of the board.

CONCLUSION

As can be seen from these examples, several steps in the PCB development process will have more impact on the manufacturability of the PCB. Having the knowledge of these issues and developing a process for minimizing their potential impact can go a long way toward increasing the manufacturability of a circuit board during the design phase of the project. ed

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2. JEDEC Standard J-STD-020D.1

DAMON DOMKE is a senior hardware design engineer at Texas Instruments (TI), where he is currently designing evaluation modules and test boards for the Sitara processor platform. He is a member of the Group Technical Staff at TI. He has worked the past 24 years developing embedded processor-based circuit boards, FPGA development systems, and software/firmware technologies. He earned a master of science degree in electrical engineering and computer science from the University of California, Irvine.

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Don't Let Tin Whiskers Destroy Your Design

Restrictions on lead products have benefitted health and the environment, but substitute technologies that use tin present their own host of issues.

Tin whiskers is not a fanciful term for some obscure aspect of electronics manufacturing. Tin whiskers are real, microscopic conductive fibers emanating from pure tin surfaces, and they pose a serious problem to electronics of all types. Almost invisible to the human eye and 10 to 100 times thinner than a human hair, they can bridge fairly large distances between electrical device leads.

When a whisker grows between two conductors, it usually "fuses" (disappears), creating a momentary short circuit. In some cases it forms a conductive path, creating false signals at an incorrect location that can, in turn, cause improper operation of the device in question. They can grow fairly rapidly. Incubation can range from days to years, and there is no set timetable for when they commence growing. In very rare cases, rather than disappearing like a fuse link, the whisker can instead form conductive plasma capable of carrying over 200 A.

A tin whisker is generally a single crystalline filamentary surface eruption from a metal surface, though polycrystalline filamentary surface eruptions have been observed. Whiskers are usually thin, metal films, 0.5 to 50 µm, that have been deposited onto a substrate material.

A typical whisker is 1 to 5 µm in diameter and between 1 and 500 µm long. Whiskers can be straight, kinked, or even curved *(see the figure)*. Metallic film deposits have also shown other types of eruptions that are quite different in appearance from the whisker eruption. These eruptions are known as flowers, extrusions, and volcanoes.

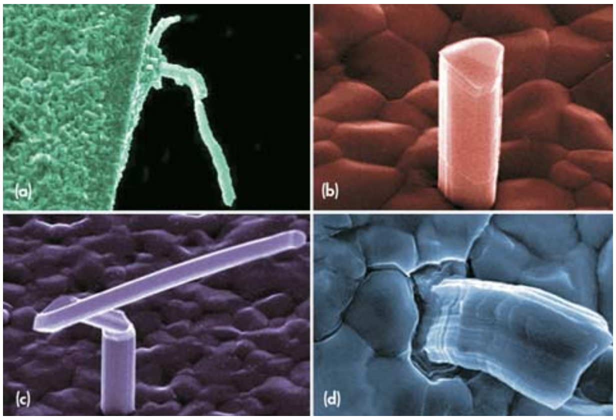
TIN WHISKERS AND ROHS

Tin whiskers are relevant to today's engineers and OEMs because they are a result of switching to lead-free electronics. The use of lead (Pb) has been banned in Europe since 2006 by the 2003 Restriction of Hazardous Substances Directive 2002/95/EC (RoHS). Although it originated in Europe, the directive now affects virtually every piece of electronics gear manufactured today or planned for the near future.

Connectors, passive and active components, switches, and relays all now must be lead-free. European safety agencies determined that it was necessary to prevent lead from entering landfill dumpsites because it is a hazardous substance. Lead is recognized as a neurotoxin known to inhibit hemoglobin production and affect brain development. Children are more at risk than adults. The removal of lead from paint and gasoline has measurably improved our environment.

As a result of RoHS, pure, tin-plated electronics have become ubiquitous in modern society over just the past five years. These electronic systems are the backbone of our communications and financial systems, our manufacturing and transportation systems, and our power plants. In these critical systems, tin whiskers have created conductive paths and other kinds of destruction in unintended places.

RoHS is not all-embracing. Because of the potentially dangerous and unpredictable risks of pure tin, it is not used in



Whiskers are usually thin, metal films, 0.5 µm to 50 µm, that have been deposited onto a substrate material. They often grow from nodules (a). A typical whisker is 1 to 5 µm in diameter and between 1 µm and 500 µm long, as seen in this cross-section (b). They can come in different shapes, including kinked (c) or with rings (d).

medical devices. Lead is allowed in external medical devices until 2014 and for internal medical devices until 2021.

Nevertheless, apart from the medical exemption, RoHS forced most electronic part manufacturers to replace their traditional tin-lead finishes with lead-free finishes. Since changing the finishing metallization on the components from tin-lead alloys, tin electroplating has become the most common method because of its good wettability, reliable solder joints, corrosion resistance, low cost, and ease of storage. But it soon became obvious that these platings form whiskers easily.

There have been several incidents relating to Boeing 787 airliner electrical systems. In December 2012, a short circuit and electrical arcing were caused by a fault in a module that controlled a generator and plugged into the power panel of the motherboard. It caused the cockpit instruments to indicate that one of the plane's six generators was down.

Subsequently, there were incidents involving lithium-ion (Li-ion) batteries in a backup power system and an emergency locator beacon on the Boeing 787. There is also speculation that the 2013 Super Bowl blackout was due to a blown underground transformer that had tin whisker shorts through the oil separating high-voltage bus bars in the transformer.

BEFORE ROHS

Metallic whisker formation first became of widespread interest to the scientific community immediately after World War II. In 1948, the Bell Telephone Corporation experienced failures on channel filters used to maintain frequency bands in multi-channel telephone transmission lines. Bell Laboratories quickly initiated a series of long-term investigations into whisker formation, the results of which were first reported in 1951 by K.G. Compton, A. Mendizza, and S.M. Arnold.[1]

This work established that whisker formation occurred spontaneously on cadmium, zinc, and tin electroplating. The experiments studied substrate materials including copper, copper alloys, steels, and nonmetallic substrates.

One reason why the problem of tin whiskers has not yet been solved is the lack of appropriate analytical tools to study the basic structure of the tin film. Only in recent years have tools like focused ion beam (FIB), synchrotron X-ray diffraction, and electron back scattering beam (EBSD) become available for researchers to use in investigating this problem.

INDUCED FAILURES

With circuit geometries now so much smaller than they have been even recently, adjacent whiskers can easily bridge spaces between leads. Alternatively, whiskers from adjacent areas can touch each other, causing short circuits. In addition to causing shorts, loose whiskers can bridge board traces, foul optics, or jam microelectromechanical systems (MEMS).

Previously, circuit voltage and current levels would almost instantaneously vaporize any whiskers, and the circuit would not even notice the event. But low voltage and current levels in modern circuits do not have the energy needed to melt the whiskers, so circuits stay shorted by the whiskers *(see the table)*.

No known test can accurately determine a plating technology's propensity to generate whiskers. The stratification of electronics manufacturing gives system integrators only limited insight into the materials that are being incorporated into their products.

Just-in-time (JIT) manufacturing and the use of commercial-off-the-shelf (COTS) parts are common practices. JIT allows parts to be directly incorporated into systems with little or no inspection. COTS parts typically have very few restrictions on materials. Suppliers may not even be required to provide any prior notice for changes in materials or processes.

HOW TIN WHISKERS FORM

There have been contradictory opinions about the formation of tin whiskers. According to the latest information, the lead-frame material or substrate has a major impact on whisker formation. This has been one of the factors causing confusion and inconsistent conclusions.

Another factor that seems to influence results is the use of matte versus bright tin finishes. (Matte tin films seem to be less prone to whisker formation and growth than so-called "bright" tin films.) Many current suppliers claim that a proprietary version of matte tin is whisker-free, but these claims may be premature and should be considered carefully before use. In reporting and analyzing results, all pertinent information should be noted including, but not limited to, the type of tin used, lead frame material, and any underlay material.

The driving force behind tin whisker formation is stress in the tin film. Such stress may come from the "as plated" (i.e., not reflowed) film with its associated texture. However, the stress can also come from inter-metallic formation or mechanical operations, such as bending, forming, thermo-mechanical stresses, or possibly oxygen diffusion and/or oxide formation on the surface. The corrosion of the tin itself is another possible source for the stress in the finish. Compressive stresses are fundamental to all whisker formation.

The driving force behind a reaction, e.g., a compressive stress, often an be eliminated or reduced by diffusion-based relaxation mechanisms. But sometimes the driving force is not relieved by diffusion or other solid-state mechanisms, and it is even possible that the driving force can be continuously regenerated or renewed. That is, inter-metallic formation, oxide reactions at the film surface, temperature cycling, and certain kinds of constant mechanical clamping are all conditions where the compressive stress is continually regenerated or is undiminished by solid-state mechanisms.

Stress, however, is a necessary but not in itself sufficient condition for whisker formation. It appears that there must also be a specific type of crystalline microstructure present.

DESIGN NOTES

Versatile Industrial Power Supply Takes High Voltage Input and Yields from Eight 1A to Two 4A Outputs – Design Note 520

Martin Merchant

Introduction

Today's industrial electronic systems contain many of the same components as consumer electronics—microcontrollers, FPGAs, system-on-chip ASICs and other electronics—requiring multiple low voltage rails at widely varied load currents. Industrial applications can also demand a pushbutton interface, an always-on supply for a real-time clock (RTC) or memory and the ability to take input power from a high voltage supply. Other required features may be a watchdog timer (WDT), a kill or reset button, software adjustable voltage levels and error reporting of low input/output voltages and high die temperature.

The LTC®3375 is a highly configurable multioutput step-down power converter that offers the features often required by industrial electronics while providing the flexibility to configure various outputs with maximum currents ranging from 1A to 4A.

Configurable Maximum Output Current

The LTC3375's eight 1A channels can be combined to produce various combinations of 1A, 2A, 3A and 4A buck regulators, as shown by the 15 different output current configurations in Table 1.

Connecting the feedback pin of a given channel to its V_{IN} pin configures that channel as a slave to the adjacent channel. The switch pins of the two channels are connected together to share a single inductor and output capacitor. Master/slave channels are enabled via the master's enable pin and regulate to the master's feedback network.

Output current can be increased to 3A or 4A by connecting additional adjacent channels. The circuit in Figure 1 shows the LTC3375 configured with a 3A output, a 1A output, two 2A outputs and an always-on LDO. It also illustrates how the LTC3375 can be connected to control the start-up of an upstream external buck controller via the on-chip pushbutton interface to supply input power to the LTC3375 buck regulators.

Table 1. LTC3375 Maximum Current Configurations

NUMBER OF BUCKS	OUTPUT CONFIGURATION
8	1A, 1A, 1A, 1A, 1A, 1A, 1A, 1A
7	1A, 1A, 1A, 1A, 1A, 1A, 2A
6	1A, 1A, 1A, 1A, 1A, 3A
6	1A, 1A, 1A, 1A, 2A, 2A
5	1A, 1A, 1A, 1A, 4A
5	1A, 1A, 1A, 2A, 3A
5	1A, 1A, 2A, 2A, 2A
4	1A, 1A, 2A, 4A
4	1A, 1A, 3A, 3A
4	1A, 2A, 2A, 3A
4	2A, 2A, 2A, 2A
3	1A, 3A, 4A
3	2A, 2A, 4A
3	2A, 3A, 3A
2	4A, 4A

External V_{CC} LDO and External Input Power Supply Start-Up Control

The LTC3375 can control an external LDO pass device to supply its V_{CC} power and any other low current electronics such as an RTC. The V_{CC} powers the internal pushbutton circuitry, WDT, internal registers and open-drain pull-ups. The external LDO in Figure 1 creates a 3.3V supply from the 24V rail.

When the pushbutton is pressed, the ON pin is released and the RUN pin is pulled high on the LTC3891, supplying input power to the buck regulators of the LTC3375. When the LTC3891 achieves regulation, the PGOOD pin is released, enabling EN1 of the LTC3375 and turning on the 2A regulator. The remaining regulators can be enabled with the precision threshold enable pins or via software-controlled I^2C commands. Pressing the pushbutton again for 10 seconds or more, or pulling $\overline{KILL}$ low for 50ms or more, causes the ON pin to be pulled low, disabling all of the buck regulators.

Unique Power Control and Features

The I^2C interface allows extensive control of regulator operation. Each regulator may be set to a high efficiency Burst Mode® operation to save power at light loads or set to forced continuous mode for lower output ripple voltage. Each regulator can also have the switching cycle phase shifted by 0°, 90°, 180°, or 270° with respect to the reference clock to allow a lower input ripple current when multiple outputs are supplying large loads. Another feature is the ability to manipulate each output voltage up or down by adjusting the feedback reference voltage from the default 725mV setting in 25mV steps (ranging from 425mV to 800mV). The I^2C interface is also used for reporting error conditions for each regulator.

The LTC3375 has a reset ($\overline{RST}$) pin and an interrupt request ($\overline{IRQ}$) pin, which can be programmed to report when any regulator's output voltage has dropped below 92.5% of the regulation point. The $\overline{IRQ}$ pin can also be programmed to report when the input voltage drops below the undervoltage lockout (UVLO) threshold or when the die temperature has reached a set temperature threshold. The regulator's PGOOD and UVLO status, the die temperature warning and the measured die temperature can be monitored by the microprocessor via the I^2C interface.

One problem with microprocessors is that a software bug can cause the program to hang. The LTC3375 includes a watchdog timer input (WDI) pin to monitor the SCL pin or some other pin to determine if the software is still running. If the software has stopped running, the watchdog timer output (WDO) pin can be used to reset the microprocessor or power down the HV buck and the LTC3375 buck regulators. Connecting the WDO pin to the $\overline{RST}$ pin of a microprocessor causes the microprocessor to reset when the WDT is not satisfied. Connecting the WDO pin to the $\overline{KILL}$ pin causes the ON pin to go low, disabling the HV buck and all LTC3375 regulators. The $\overline{KILL}$ pin can be pulled low by a pushbutton "paper clip" switch to power down all the regulators as a last resort.

Conclusion

The LTC3375 can be configured with multiple regulated 1A to 4A outputs totaling up to 8A, and includes many features required by today's industrial electronics.

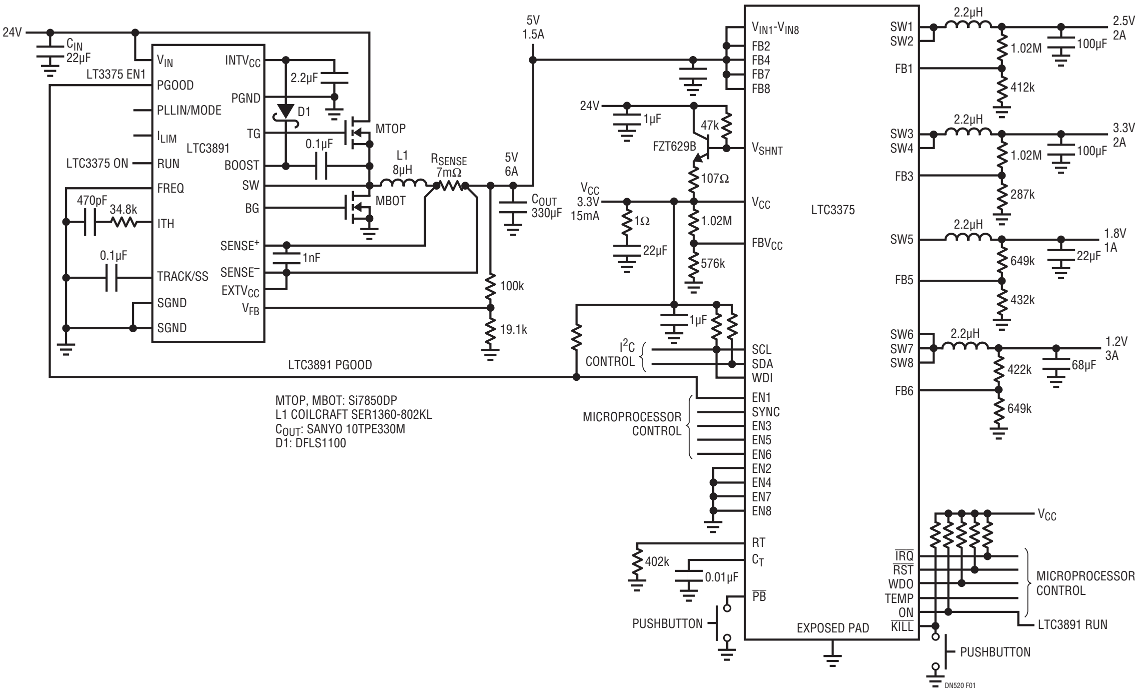


Figure 1. Low Voltage Power Supply with Pushbutton Control of Upstream HV Buck and Always-On LDO

Data Sheet Download

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TIN WHISKER-INDUCED FAILURE MECHANISMS
• Stable short circuits in low-voltage, high-impedance circuits where current is insufficient to fuse the whisker open
• Transient short circuits that persist until the whisker fuses open
• Plasma-arcing in a vacuum, where a whisker fuses open, but the vaporized tin results in plasma that is capable of conducting more than 200 A; This phenomenon is reported to have occurred on at least three commercial satellites and rendered the spacecraft non-operational
• Whiskers or pieces of whiskers that break loose and bridge conductors or interfere with optical surfaces or jam MEMS

Researchers have also noted variations in whisker "incubation times" that range from minutes to decades. This variation is believed to be due either to the mechanisms involved in nucleating these specialized crystalline microstructures and/or the time required to build up sufficient compressive stress in the tin films. If the film stress levels are maintained at a high enough compressive level for a long enough period of time, there will be a very high likelihood of a whisker being formed as a means of relaxing the stress levels within the film beyond what can be accomplished by simple diffusion.

Based on tests, another major cause of stress that may yield whisker formation is the irregular growth of the Cu_6Sn_5 intermetallic created when tin is plated on copper-based substrates. (Broadly speaking, Cu_6Sn_5 is a from of bronze, but in the context of tin whisker formation metallurgists refer to it as an intermetallic.) Cu_6Sn_5 forms readily in the tin layer on tin-plated copper surfaces at room ambient temperatures. In fact, it is the dominant intermetallic at temperatures below 60°C.

The growth of Cu_6Sn_5 creates compressive stress in the tin layer. There are two contributing factors. First, at any temperature, the diffusion of copper into tin proceeds through grain-boundary diffusion and forms intermetallics. At room temperature, the primary intermetallic is Cu_6Sn_5, and grain-boundary diffusion is significantly faster than bulk diffusion. This results in irregular growth of Cu_6Sn_5 in the grain boundaries of the tin. (At temperatures well above room ambient, generally at about two-thirds of the absolute melt temperature, bulk diffusion starts to become significant.)

Second, there are two schools of thought concerning the formation of compressive stresses in the tin film in and around the copper-tin intermetallic and the tin (copper-tin-to-tin interface). If six parts of copper are mixed with five parts of tin, the resultant Cu_6Sn_5 has a larger molar volume than the tin and copper from which it was formed. This in itself would lead to compressive stresses at the copper-tin-to-tin interface.

Or, considering that the copper infiltrates the tin lattice sites in the tin film leaving behind open space in the underlying copper, then the overall reaction will lead to an increase in volume in and around the copper-tin-to-tin interface. This also acts as a compressive layer of tin. Furthermore, grain-boundary diffusion dominates the growth of the Cu_6Sn_5 phase at lower temperatures. As such the interface between the tin grains and the Cu_6Sn_5 phase is non-planar. This can also act to increase the localized compressive stresses in the tin film.

At higher temperatures, the primary diffusion mechanism changes from grain-boundary diffusion to bulk diffusion. This results in changes in the intermetallic layer:

- Cu_6Sn_5 formation: Somewhere above 60°C (the exact temperature has not yet been established), Cu_3Sn will form from the Cu_6Sn_5 and will be found between the Cu_6Sn_5 and copper layer. Cu_3Sn_5 has a lower molar volume and will not add to stress in the tin layer.
- Bulk diffusion effects: Due to bulk diffusion at higher temperatures, a more regular intermetallic double layer (Cu_3Sn and Cu_6Sn_5) will form. (This forms the basis for a strategy of mitigation by heat treating at 150°C.)
- Plating bath impurities: Impurities in the plating bath and other defects may also enhance the possibility of whisker formation. It is not understood which impurities are the culprits and the levels to which they should be controlled. Both copper and carbon appear to be impurities that make the tin film stress increasingly compressive.
- Oxide formation and humidity: The role of oxide formation is not well understood. Humidity apparently introduces stresses from the diffusion of oxygen downward from the surface. By comparison, intermetallics introduce stresses from the substrate interface towards the surface. High humidity will affect the thickness of the oxide film on the tin layer, leading to compressive stress. Impurities or defects in the oxide film may also contribute to whisker formation. High humidity might lead to corrosion, which could introduce additional stress. The relation to actual field life of these test conditions is unknown. Serious consideration should be given to storage conditions. Additionally, the high humidity may affect the tin's surface diffusion rates.
- Condensation and corrosion: Condensed moisture exposure, either by water condensation during high-temperature humidity testing or via water droplet exposure, can lead to corrosion-assisted whisker growth. Excessive localized surface corrosion can produce non-uniform oxide growth that imposes additional differential stress states on the tin film. The combination of condensed moisture and higher temperatures has been shown to produce either localized clusters of whiskers or accelerated growth of an individual whisker. Often identified as lead termination "black spot corrosion," whiskers found to nucleate in the corroded regions will continue to grow even after removal of the condensed moisture. Corrosion has been identified as a confounding factor in extended duration, high-humidity testing.
- Incubation time: The incubation time before whiskers form has been very unpredictable. Under high-stress conditions,

whiskers have been shown to grow very rapidly. In other cases, years have passed before whisker growth has been seen at all. This may be due to the requirements for a recrystallization event to occur that creates an appropriate whisker grain, or whisker growth may be delayed due the length of time required to build sufficient stress to start the whisker formation process.

WHISKER MITIGATION

"Mitigation" refers to processes or materials that enhance resistance to whisker formation on tin-based films, but do not necessarily prevent their ultimate formation. Since compressive stresses are thought to be fundamental to whisker formation, mitigation approaches are aimed at altering the stress state within the tin.

The first and best option is to avoid using pure tin, but depending on suppliers, it is seldom possible. The mitigation techniques described below can be effective, but none of them have been proven to provide the degree of protection required by high-reliability equipment. With that caveat, here they are:

- Specify matte tin (tin with a dull low-gloss finish and larger grain size). It resists whiskers better than bright tin.
- Anneal the tin after plating. This can reduce the stresses created during plating that contribute to whisker growth.
- Robotic solder dipping with tin-lead solder is said to work for some, but not all, components. Obviously, the components must be handled carefully to avoid damage during the process.
- Conformal coatings can be applied, but their success depends on the coating material, thickness, and application process.
- Some testing has shown promise for surface chemical etching prior to plating of copper-based alloys. The etching depth is in the range of 3 to 4 µm.
- Conformal coatings on circuit board assemblies can be used to reduce electrical shorting risks. Thicker coatings (≥3.9 mils) can prevent or delay whisker penetration. Thinner coatings act as a dielectric layer for whiskers that may break off in an assembly. ed

REFERENCE
"Filamentary Growths on Metal Surfaces - Whiskers," K.G. Compton, A. Mendizza, and S.M. Arnold, 1951

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Maintain Signal Integrity From Bus To Scope At 30 GHz And Beyond

As output voltages shrink, serial signal margins are getting smaller, creating a need to boost the measurement system's performance and reduce noise.

With serial data rates continuing to climb, minimizing the effect of the measurement system's internal noise on the signal is increasingly important. As output voltages shrink to boost speeds, the margin between pass and fail has shrunk to the point where noise from the signal and the measurement system can combine to close the eye.

One of the most important elements in ensuring accurate measurements is the connection between the signal access point and the oscilloscope. This connection needs to be able to handle signals as fast as 30 GHz to ensure accurate results for compliance measurements, while adding very little noise. Fortunately, high-speed oscilloscope probes boost measurement accuracy at these higher data rates. They also help simplify what would otherwise be a daunting test and measurement challenge.

SIGNAL ACQUISITION REQUIREMENTS

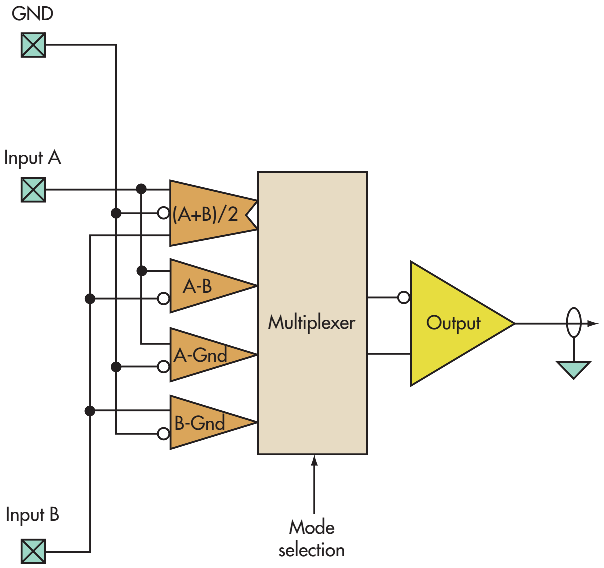
Data rates of third-generation serial bus standards continue to increase, moving the minimum bandwidth requirement for debugging many common buses beyond 16 GHz, and even 33 GHz *(see the table)*. To ensure accuracy, standards bodies typically specify the use of an oscilloscope with a bandwidth several times more than the fundamental frequency of the serial signal. Support for differential, single-ended, and common-mode measurements is equally important in oscilloscopes and probes.

HIGH-SPEED SERIAL STANDARDS

Standard	Data rate	Third harmonic	Fifth harmonic
10Gbase-KR/ Thunderbolt/SFP+	10.3125 Gbits/s	16 GHz	26 GHz
CEI-11	11 Gbits/s	17 GHz	28 GHz
SAS-3	12 Gbits/s	18 GHz	30 GHz
16G Fibre Channel	14.025 Gbits/s	21 GHz	35 GHz

Nearly all high-speed data buses use transmission lines that are differential pairs, which are used for upstream or downstream communication. They are also used as lanes if the bus uses multiple transmit and receive lanes. Acquiring and measuring these differential signals with a high common-mode rejection ratio (CMRR) requires an oscilloscope probe with a differential amplifier input stage. High CMRR is needed to reject signals common to both sides of a differential pair. The common-mode signals can show as distortion or added noise in the differential measurement.

Acquiring differential signals is critical, but measuring each side of a differential pair individually (single-ended) and the common-mode components of the signal is important as well. Many high-speed serial bus standards specify that compliance



1. This block diagram shows a probe that supports differential, common-mode, and single-ended voltage measurements with a single coax connection to the device under test.

testing must verify that a bus meets specifications for differential, single-ended, and common-mode voltage outputs.

Differential probes with high bandwidths are readily available for measuring differential voltage levels. Measuring single-ended or common-mode voltages requires multiple probes or moving a single probe from point to point. A significant advance in usability is a new generation of probes that allow measurement of differential, single-ended, and common-mode voltage levels with a single connection to the device under test (DUT) using a single probe setup *(Fig. 1)*.

COAXIAL CONNECTIONS

Connecting to high-speed buses often requires a controlled impedance board or fixture with coaxial connectors such as SMP or 2.92-mm/K-type connectors. An oscilloscope can be connected to the test fixture with coaxial cables with the appropriate connectors on each end. However, coaxial cables exhibit variable loss with respect to frequency *(Fig. 2)*. This loss needs to be addressed.

In addition, any two coaxial cables are not identical in length and therefore have different propagation times. Differences even as small as a few picoseconds show as skew between differential signal pairs and can degrade the quality of the measured signal. Timing skew between cables needs to be measured and adjusted out for an accurate differential measurement.

A probe with coaxial input connectors eliminates the need for a separate set of coaxial cables. With the latest 33-GHz probes, the system response is calibrated in level (±1 dB) and skew (±2 ps) at the probe's tip. This calibration eliminates the need to correct the measurement for loss or timing skew in a set of cables.

To further enhance the measurement, the signal acquired at the probe tip can be corrected based upon S-parameter models of the probe and S-parameters of the oscilloscope system stored in each device. The model is automatically downloaded to the oscilloscope when the probe is connected.

These S-parameters are used to correct the frequency response for the measurement system including any loss or gain in the probe. Connecting to the test fixture directly with the probe reduces the distance between the signal output and the measurement system input and improves the fidelity of the measurement.

Coaxial connections also present challenges when making the various mode measurements required. If the two inputs are used for a differential measurement, making single-ended measurements means the engineer must ensure that the unused input is correctly terminated. Measuring common-mode voltage is also more involved, requiring the test engineer to measure both sides of the differential pair (A and B), then inserting the two waveforms into:

Common-mode voltage = (A + B)/2 – the reference voltage (usually 0 V or ground)

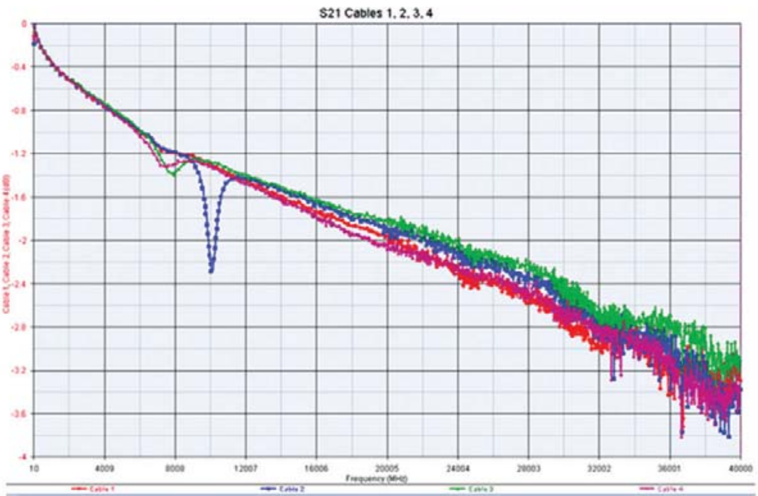
The math function on an oscilloscope makes this calculation possible, but using waveform math adds time and complexity to the measurement. In contrast, the latest probes incorporate a switch matrix that allows the user to switch the routing of the signal's differential pair.

Either side of the differential pair can be measured, as well as its differential and common-mode components. When making multiple differential, single-ended, and common-mode measurements, this eliminates the need to continually adjust and re-adjust the probe's connection to the DUT. As an added convenience, the probe offers automatic probe tip identification, which ensures the correct digital signal processing filters are used.

SYSTEM NOISE

High-speed data signals achieve some of their speed increase by lowering the differential output voltages, making lower noise in the system and in the measurement system important. As the output voltages shrink, the margin between pass and fail gets smaller. An eye diagram measurement of a 12-Gbit/s serial signal illustrates how noise from the signal and the measurement system can combine to close the eye *(Figures 3 and 4)*.

Measuring these lower voltage swings requires a probe and oscilloscope with a high signal-to-noise ratio (SNR) to mini-



2. This graph shows the varying loss for four different coaxial cables.

mize the effect of the measurement system's internal noise on the signal. The latest probes and high-performance oscilloscopes together provide a system noise specification of less than 1 mV rms. Previous probe and oscilloscope combinations can have as much as three times as much noise.

In addition, it's important to keep the cable length from the DUT to the probe or oscilloscope as short as possible to minimize added noise. Locating the probe's differential amplifier close to the DUT reduces the noise.

In addition to a high SNR, high sensitivity is desirable. Often access to the signal under test is at the end of a backplane or a compliance load board channel. The lower the serial signals' amplitude, the more sensitive the probe and oscilloscope need to be. High-performance oscilloscopes and probes offer high sensitivity at 3.48 mV/div at 30-GHz bandwidth compared to more typical sensitivities of 10 mV/div or higher.

PROBE MODELING

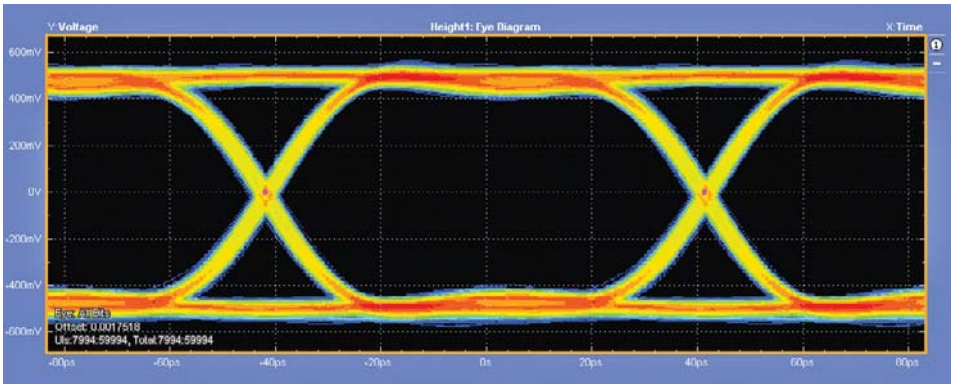
Design and implementation of serial data links often require many hours of simulation and modeling. Once hardware implementation begins, the serial links often require pre-emphasis/de-emphasis at the transmitter and equalization at the receiver. Engineers may wonder how the system will react when a probe is attached to their finely tuned link. As such, it is important to ensure that measurements reflect the true operation of the serial bus, with any effects of the probe removed.

One of the more innovative features now appearing in higher-speed probes is the ability to store S-parameter models directly in the probe. These models can then be read by the oscilloscope's software when the probe is attached to the scope. The oscilloscope then removes the effects of the probe from the measured signal and gives the engineer a view of the signal as it appears at the TX output or RX input.

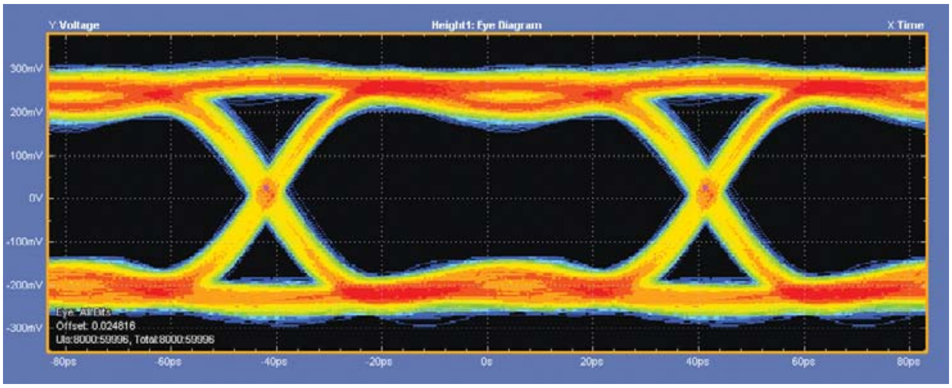
LOW-NOISE PROBES

As data communications standards move to higher and higher speeds, measurement systems must combine high bandwidth with low noise and high sensitivity. In addition to higher-bandwidth oscilloscopes and signal generators, engineers must consider the connection between the DUT and the oscilloscope's input. Many serial standards also require differential, single-ended, and common-mode measurements.

While coaxial cables can be used for making the connection, this approach considerably burdens the engineer to measure and remove channel effects and to move connections around to make the different measurements. New high-bandwidth probes with coaxial inputs offer up to 33-GHz bandwidth performance for acquiring today's high-speed serial bus signals with minimal added noise and smaller than 1X attenuation. Additionally, they provide the ability to measure differential, single-ended, and common-mode signals without changing physical connections.



3. When noise from the system and the measurement channel is minimized, the result is an "open" eye.



4. High noise levels can reduce the eye amplitude (the difference between logic 0 and 1), making it difficult to recover or analyze the data.

KEVIN CASSIDY is a marketing manager and product planner for Tektronix high-performance probes. He has a BSEE from the USAF Academy and more than 15 years of experience in the test and measurement industry.

Specialized Circuit Drives 150-V Piezoelectric Motor Using Low-Voltage Op Amp

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A PIEZOELECTRIC MOTOR is a linear motor with bidirectional motion. It uses friction to grip the armature while a voltage is ramped to warp the piezoelectric material and move the armature. The voltage then is quickly removed.

As the material springs back, it breaks away from the armature and returns to its zero position, leaving the armature a few micrometers further along its track. Repeat this at a kilohertz rate and for thousands of times.

While each of the motions is very small, after several seconds you may see that the armature has moved, if you look carefully. (Full disclosure: I had never heard of piezo motors before being asked to make a driver for one.)

There are two drive waveforms, one for forward and the other reverse: a sawtooth waveform with a slow linear rise followed by a fast fall, and its complement with a fast rise and slow linear fall. This was done using an op-amp triangle-wave oscillator at 1 kHz, with diodes switched in to speed up either the rising or falling edges to about 5% of the cycle. The driver's required bandwidth is only 10 to 15 kHz.

The problem is the voltage. Fortunately, it is unipolar. Unfortunately, it is +150 V (peak). The required current is quite small. It has to be only enough to charge and discharge the 20-nF piezo element. A calculation using charge transfer (Q) shows that during the ramp phase:

$$Q = It = CV$$

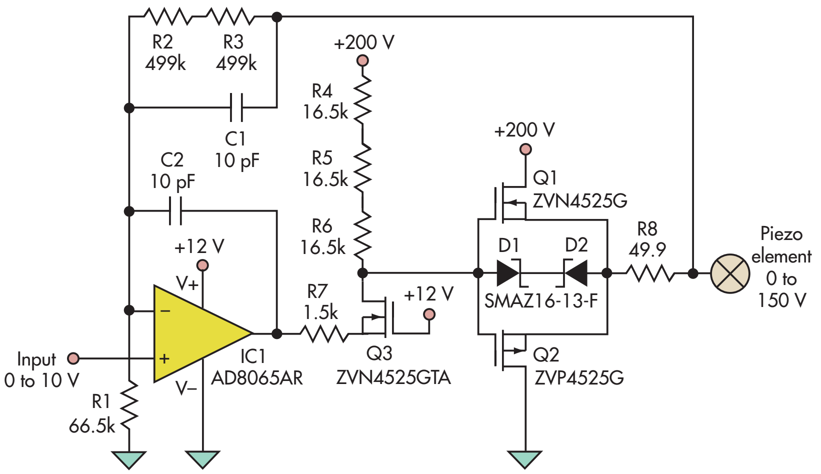
where:

$$t = 1\text{ ms}$$
$$C = 20\text{ nF}$$
$$V = 150\text{ V}$$

therefore:

$$I = CV/t = 3\text{ mA}.$$

A 600-mW boost converter can be used to switch the +12 V up to +200 V with a 3-mA load requirement. The most straightforward circuit uses an op amp rated to at least 200 V. Op amps are available with this voltage rating, but they are meant for high-current applications and are quite expensive.



A low-voltage op amp can be used to drive a higher-voltage piezoelectric motor. D1 and D2 protect the circuit against load shorts, while resistors in series strings are used to reduce individual resistor dissipation and minimize their voltage coefficient of resistance.

The circuit in the figure is much cheaper and based on a common op amp used as a non-inverting amplifier. The heart of the circuit is the current mirror of R7, N-channel FET Q3, and series-connected R4, R5, and R6. (The reason for using three resistors in series is explained below.)

With Q3 in a common-gate configuration and the gate at +12 V, its source voltage remains reasonably constant at +10 V (from +12 V less the $V_{gs(on)}$). Any output of op-amp IC1 less than that +10 V causes a voltage drop across R7, with the current coming from R4 to R6. Since R7 has the same current as R4 to R6, there is a voltage gain of the ratio of (R4 to R6)/R7 or 33. The voltage at the bottom of R4 to R6 (the Q3 drain) now has the required voltage swing but a high impedance.

A pair of complimentary FETs acts as followers to lower the output impedance and boost current output. Negative feedback is provided via R2 and R3, along with bandwidth limiting by C1. The overall closed-loop gain is set by (R2 + R3)/R1 + 1 = 16.

There are a few subtleties to the circuit. If something happened to the piezo motor, such as the user shorting it, Zener diodes D1 and D2 would protect the FET gates. The current-mirror high-side resistance provided by R4 through R6 is split into three distinct devices to handle the power levels so 0805/2012 surface-mount (SMT) resistors can be used. The feedback resistance composed of R2 and R3 is split into two devices to reduce the voltage coefficient of resistance. This is a somewhat obscure effect, where a component's resistance actually changes slightly at higher voltages.

There is a small feedback capacitor directly on the op amp to provide stability. Without it, the parasitic capacitances (most notably the Miller capacitances C_{dg} and the piezo's capacitance) would cause enough phase shift for the op amp to oscillate. Crossover distortion is not a problem because the piezo element could not react to that bandwidth and does not require a perfect waveform.

Another problem would be the infinite pole caused by a purely capacitive piezo element. By taking the feedback directly from the sources of Q1 and Q2, resistor R8 would add a more deterministic pole to the load and increase loop stability.

Once the somewhat finicky piezo motor was adjusted, the final circuit worked well. The armature would move back and forth with incredibly fine resolution.

ALAN STUMMER designs electronics for the University of Toronto's quantum optics and pulse laser research labs, after years working on analog controls for heavy industry and then telecom.

Model Diacs And Triacs For AC-Line Control

APPARAJAN GANESAN | CONSULTANT dg1@austin.rr.com

DIACS AND TRIACS often are used for line-voltage control. They also are getting additional interest as part of Internet- and cell-phone-controlled power-line switches such as the Belkin WeMo Home Automation Switch.

The traditional approach has been to model them using bipolar transistors and diodes.[1] Table-based models have been used with varying success.[2] The functional model approach shown here works well and has been used extensively with the LTspice simulator (free, from Linear Technology).

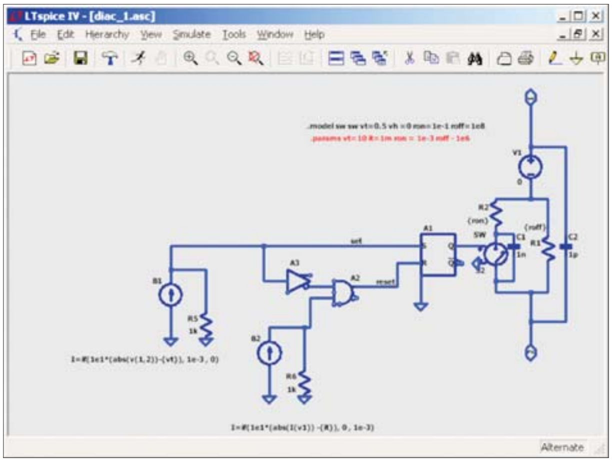
In the diac schematic of Figure 1 and associated Listing 1, there are four parameters *(Listing 1a is for the diac macromodel; Listing 1b is the diac symbol; listings are available with the online version of this article at electronicdesign.com)*:

V_t: voltage at which the diac triggers
I_t: current at which it turns off
R_{on}: resistance when it is on.
R_{off}: resistance when it is turned off

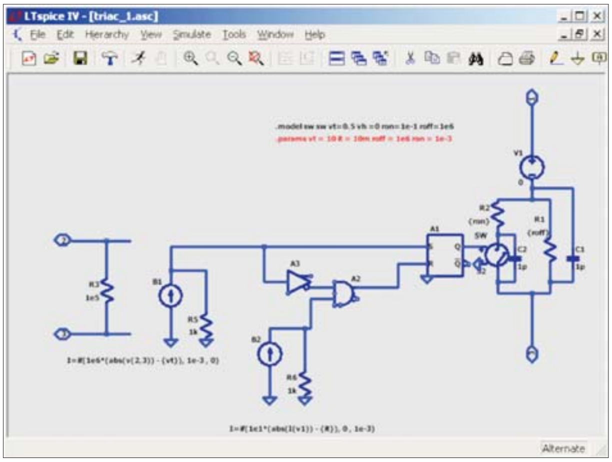
To turn on, the diac needs the voltage to exceed V_t. Once it turns on, it needs the current to go below I_t to turn off. In operation, the device starts as an open circuit. When the voltage across it exceeds V_t, the flip-flop is set, putting the device in its on state with a low resistance of R_{on}.

The device continues in this state until the current through it falls below I_t. At that point the flip flop is reset and the device switches once again to its off state, with a resistance R_{off}. (Note that the device is bi-directional.)

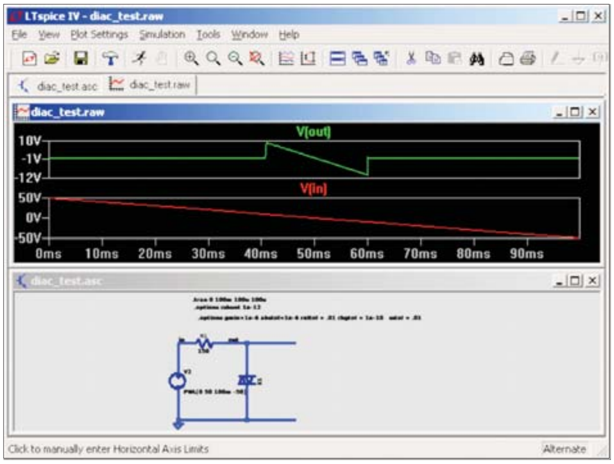
The triac is modeled in a similar manner *(Figure 2 and Listing 2; Listing 2a is for the triac macromodel; Listing 2b is the triac symbol)*. It has the same four parameters as the diac



1. In the diac circuit, the device starts as an open circuit and remains open until the voltage across it exceeds V_t



2. For the triac, the trigger voltage is on an independent port, in contrast to the diac.

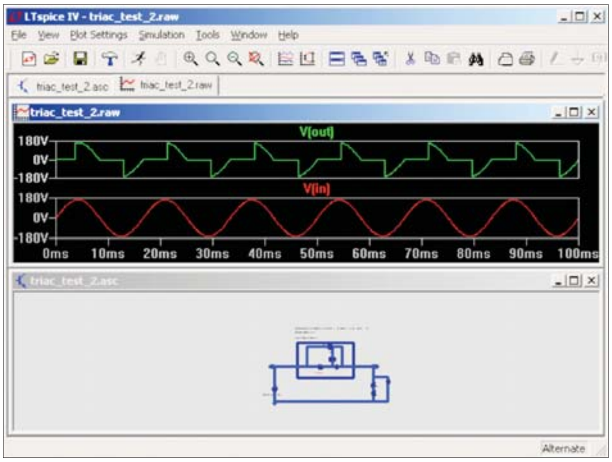


3. The results (top) of the diac test circuit (bottom) show the symmetrical operation of the circuit and allow for user modifications.

component, and it needs the voltage to exceed V_t to turn on. Once it turns on, it needs the current to go below I_t to turn off. The difference between the diac and the triac is that the triac trigger voltage is on an independent port.

It is difficult to design test circuits for these devices because, as a result of their negative resistances, they usually oscillate or provide limit cycles, which in turn makes it difficult for programs such as Spice to converge. The main diac characteristics of interest are breakover voltage, voltage symmetry, breakback voltage, breakover current, and power dissipation.[3]

In the output file for the diac test circuit, V_{In} is initially at its negative extreme, and V_{Out} is low, as the device is in its on state *(Figure 3 (top) and Listing 3a, and corresponding schematic Figure 3 (bottom) and Listing 3b)*. As V_{In} goes lower, the device turns off once the current falls below I_t. It again reaches its on state once the voltage exceeds V_t. The device is bidirectional and inherently symmetric. Also, the model can be modified to include current limits on voltages, as well as asymmetries.



4. The results (top) of the dimmer circuit (bottom) using a diac and triac show the operation possible with a standard resistive load.

For the triac, the popular dimmer circuit is used for test, with output file Figure 4 (top) and Listing 4a along with corresponding schematic Figure 4 (bottom) and Listing 4b. The load is a typical 100-W bulb, and the RC-time constant determines when the triac is triggered.

The diac in series with the gate is chosen to ensure the triac turns off completely. The model can be modified to include current limits, voltage asymmetries, dV/dt effects, and more. By varying the RC-time constant, the duty cycle of the output can be varied from 5° to about 170°, nearly spanning the full 0° to 180° theoretical limit. The device as modeled produces identical results in the positive and negative half cycles.

REFERENCES

1. "A Spice Model for Triacs," A.F. Petrie and Charles Hymowitz, www.readbag.com/intusoft-articles-triac
2. "Model for Diac in Orcad 9.2," www.edaboard.com/thread241914.html
3. "Diac Tutorial," American Microsemiconductor, www.americanmicrosemi.com/information/tutorial/index.php?t_id=2#ixzz2eObwolgW

APPARAJAN GANESAN has an MS from the State University of New York (SUNY) at Stony Brook and has been designing circuits for 40 years. He has worked at companies including General Instrument, Bell Telephone Laboratories (Bell Labs), RCA, and Analog Devices and has been an independent

Downconverting Mixer Delivers Exceptional IIP3 And Gain

THE HEART of all modern software-defined radios (SDRs) is the mixer. The mixer circuit establishes the receiver's basic performance level, which makes it the most critical part of the radio.

Linear Technology's LTC5551 downconverting mixer brings a whole new level of performance to new receiver designs. It targets a wide range of applications including LTE and LTE-Advanced basestations, military and public safety radios, repeaters, backhaul, avionics, radar, phased-array antenna systems, and white space receivers.

The LTC5551 boasts high linearity defined by its input third-order intercept (IIP3) value of +36 dBm and 9.7-dB noise figure (NF). Most passive mixers have a conversion loss of 7 to 9 dB while the LTC5551 delivers 2.4 dB of conversion gain, substantially improving receiver dynamic range. The 1-dB compression point is +18 dBm.

The mixer's 300-MHz to 3.5-GHz operating frequency range makes it useful in a broad array of wireless devices. Its integrated local oscillator (LO) driver only requires 0 dBm (1 mW) of LO power to meet the full IIP3 spec. The elimination of the need for a high-power LO signal greatly reduces the potential for undesirable radiation. As a result, the filtering and RF shielding requirements for the radio are minimal. A fully integrated IF amplifier is also present.

Both the RF and LO inputs have integrated balun transformers, eliminating the need for external components and circuits while simplifying the design and reducing cost and space requirements.

The LTC5551 receives its dc power from a standard 3.3-V supply and draws 204 mA of current while meeting full specifications. A low-power mode drops the current draw to 142 mA but trades off power for an IIP3 of +29.3 dB. Its shutdown mode decreases the current to 100 μA. Its 500-ns turn-on and turn-off time make it suitable for burst mode receivers.

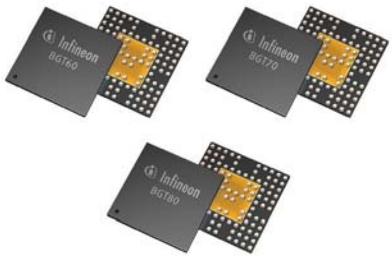
The LTC5551 comes in a 4- by 4-mm, 16-pin quad flat no-lead (QFN) package. It operates from –40°C to 105°C. Pricing is $7.25 in 1000-unit quantities.

LINEAR TECHNOLOGY

www.linear.com/product/LTC5551 **LOU FRENZEL**

Single-Chip Millimeter-Wave Transceivers Target Small-Cell Backhaul

THE HETEROGENEOUS network (HetNet) of small cells promises faster download speeds and greater cellular capacity to handle the growing demands of smart-phone and tablet users. One of the greatest challenges of building out such a network is backhaul, the connection from the small cell back to the carrier switching network. Wireless backhaul appears to be a better solution than fiber for the complex mix of small-cell locations. Infineon's BGT60, BGT70, and BGT80 single-chip millimeter wave RF transceivers make this solution practical, smaller, and more affordable.



The Infineon BGT60, BGT70, and BGT80 millimeter-wave RF front-end chips are designed for small-cell backhaul applications. The packaging is a plastic embedded wafer-level ball-grid array (eWLB) that's 6 by 6 mm.

The transceivers cover the 57- to 64-GHz (V-band), 71- to 76-GHz (E-band), and 81- to 86-GHz (E-band) frequency ranges, respectively. Each chip is a complete silicon-germanium (SiGe) RF front end consisting of a low-noise amplifier (LNA), power amplifier (PA), mixers, programmable gain amplifier (PGA), voltage controlled oscillator (VCO), and related blocks *(see the figure)*. The transceivers are direct conversion/zero IF types, so they connect via balanced I and Q connections to/from a baseband processor for the appropriate protocol. Channel tuning and TX/RX selection is made via an SPI port. The design is based on Infineon's experience with 24-GHz and 77-GHz auto radar chips. With appropriate standards, the chips can deliver the 1-Gbit/s data rates demanded of most small-cell designs.

Production on these chips has started. Samples and evaluation kits are expected in December.

INFINEON TECHNOLOGIES.
www.infineon.com **LOU FRENZEL**

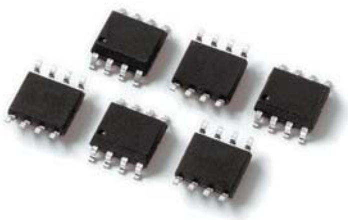
Specified Repetitive Surge Protectors Help Optimize Circuit Design

THE STRVS repetitive voltage surge-protection devices from STMicroelectronics protect against repetitive surges that heat up protection components and reduce their performance in solar-inverter, smart-meter, or mobile charger power supplies. By specifying clamping voltage at high temperature and peak current from 0 to 2 A for these devices, STMicroelectronics looks to save engineers from deliberately over-sizing protection components. The company also provides data regarding printed-circuit board (PCB) metallization on temperature. STRVS clamping voltage is constant for any load, boosting the safety of the protected power components over that of resistor-capacitor (RC) snubber protection. Overall MOSFET protection against multiple surges ranges from 50-Hz to 200-kHz frequencies.

STMICROELECTRONICS
www.st.com/strvs

TVS Diode Arrays Boost Telecom-Interface Protection By 40%

THE SRDA3.3 series of transient-voltage-suppression (TVS) diode arrays from Littelfuse integrates low-capacitance steering diodes and an additional zener diode to protect data lines against electrostatic discharge (ESD) and high-surge events. According to developer Littelfuse, the diode arrays offer 40% greater protection without performance degradation than comparable devices. Also, their 50% lower maximum capacitance versus other solutions helps preserve signal integrity and minimize data loss during transmission. Low clamping voltages for sensitive chipsets protect them from catastrophic failure. Lightning-surge protection, which complies with IEC61000-4-5, is 35 A (8/20 μs) with peak pulse power of 600 W (8/20 μs). Other features include 0.5-Ω dynamic resistance; capacitance of 8 pF (typ)/10 pF (max) from I/O to ground; and ESD protection that complies with IEC61000-4-2 (±30-kV contact, ±30-kV air). Applications include tertiary (IC side) protection of high-speed T1/E1/T2/E3 telecom data lines, xDSL and RS-232/RS-485 interfaces, as well as 10/100 Ethernet interfaces and video lines.



LITTELFUSE INC.
www.littelfuse.com

Synchronous Step-Down Switcher Keeps Quiescent Current Under 2.5 µA

THANKS TO its "Silent Switcher" architecture, Linear Technology's LT8614 4-A, 42-V, input-capable, synchronous step-down switching regulator reduces electromagnetic interference and compatibility (EMI/EMC) emissions by more than 20 dB, which is well below the CISPR 25 Class 5 limit. Synchronous rectification delivers up to 96% efficiency despite switching frequencies in excess of 2 MHz. Burst-mode operation keeps quiescent current under 2.5 µA in no-load standby conditions and output ripple below 10 mV p-p. Linear's switcher offers up to 4 A of continuous output current to voltages as low as 0.97 V. Input voltage ranges from 3.4 to 42 V, suiting automotive and industrial applications. With a minimum dropout voltage of 200 mV at 1 A under all conditions, the LT8614 fits scenarios such as automotive cold-crank. A 30-ns on-time enables 2-MHz constant frequency switching from a 16-V input to a 1.0-V output. It comes in a 20-lead 3- by 4-mm quad flat no-lead (QFN) package.

LINEAR TECHNOLOGY CORP.

www.linear.com/product/LT8614

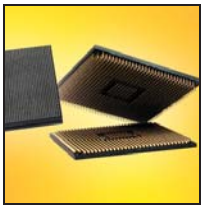
150-W PFC-Input Power Supply Extends MTBF To 170,000 Hours

ABSOPULSE'S PFW 150-24 industrial-grade ac-dc power supply addresses the need for reliable power conversion in applications with problematic or costly unit replacement. Rather than use optical components, the feedback system on the primary side employs a sensing-circuit design. As a result, mean time between failure (MTBF) reaches 170,000 hours at 45°C, minimum. The 150-W supply integrates active power factor correction (PFC) to convert a universal ac-input voltage (95 to 264 V ac) to 24 V dc. Typical line/load regulation exceeds ±2% from 5% to full load. An isolated, floating output can be grounded to either terminal, allowing for use in either positive- or negative-grounded systems, or they may be left floating. The power supply is filtered to meet EN55022 Class B conducted and radiated requirements.

ABSOPULSE ELECTRONICS LTD.

www.absopulse.com

Chip Size BGA 0.8mm Board-to-Board Connector



Ironwood Electronics has RoHS compliant SF-BGA676D-B-62F (socket module) soldered to a mother board using standard RoHS soldering methods. SF-BGA676D-B-61F (pin module) can be soldered to an upgraded daughter board. The board-to-board connector pair requires half the force of conventional connectors at 20 pounds for the 676 pin. The electrical path (the top connection point on the male pin module to the solder ball on the female socket) is 4.5 mm.

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DECEMBER 5 ED ISSUE PREVIEW

In this issue, Electronic Design's Technology editors pick the best OEM products and technologies they have covered during the year on their respective beats.

In addition, readers choose the best ideas for Design published in the magazine during the previous year.

This issue also includes our annual Hall of Fame inductees selected by readers from a list of nominees.

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18 Brenda Roode, Audience Development Director — Date 09/17/2013

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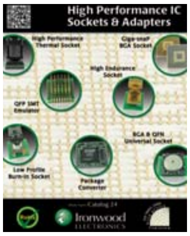
Catalog Literature Review

HIGH PERFORMANCE SOCKETS & ADAPTERS



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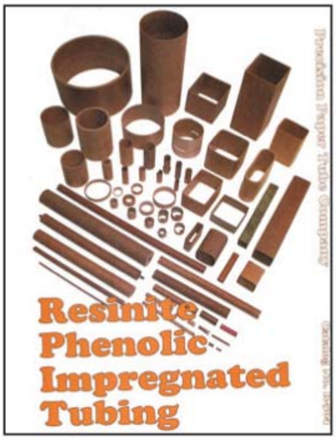

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More than 75 Years - The Original

IR's FastIRFET™ Family Delivers Industry Leading Efficiency for DC-DC Synchronous Buck Applications

International Rectifier announces the introduction of the 25V FastIRFET™ family of innovative power MOSFETs for DC-DC synchronous buck applications including advanced telecom and netcom equipment, servers, graphic cards, desktop, ultrabook and notebook computers.

The FastIRFET™ family features IR's latest generation silicon in an industry standard PQFN package that delivers benchmark power density for discrete DC-DC converters. The family includes the IRFH4201 that offers on-state resistance (RDS(on)) as low as 0.7 milliOhms, and the IRFH4210D and IRFH4213D monolithic FETKY® devices designed to reduce ringing and further improve system efficiency.

Optimized for 5V gate drive applications, IR's FastIRFET™ devices work with any controller or driver to offer design flexibility while delivering higher current, efficiency and frequency capability in a small footprint. The devices are available in industry standard 5x6 and 3.3x3.3mm PQFN packages that feature an environmentally friendly, lead-free and RoHS compliant bill of materials.

More information is available on the **International Rectifier** website at
http://www.irf.com/whats-new/nr130919.html
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How Many Quarks
Does It Take To Make An IoT?

Intel wants to build the Internet of Things (IoT) using the x86 architecture, but that would have been a challenge using the Intel Atom. After starting out small, the Atom has grown to a full-fledged, 64-bit platform with virtualization support and multiple cores. It is still a low-power device compared to the Core or Xeon lines, but multicore Arm platforms have it beat on power utilization.

The 32-bit, Pentium-class X1000 Quark system-on-chip (SoC) is Intel's new solution *(Fig. 1)*. The single-threaded core runs at 400 MHz and is designed for low-power applications well below what an Atom could be used for. The chip has a 16-kbyte L1 cache and a whopping 512 kbytes of SRAM, so the DDR3 memory support may not be required for many applications.

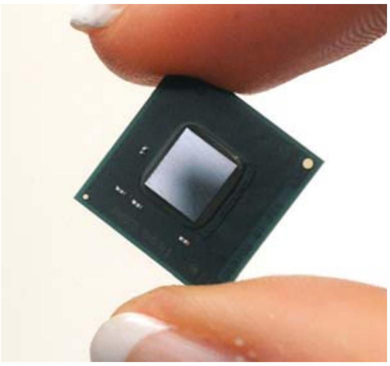
A 32-bit x86 SoC is not a new idea. 486-class SoCs have been popular, but the difference is that Quark is from Intel.

QUARK SPECS

The Quark's peripheral set is typical of this class of high-end microcontrollers. It includes 10/100-Mbit/s RMII Ethernet, x1 PCI Express Gen 2, SD/MMC, USB 2.0, SPI, UART, I^{2}C, and GPIO, as well as a real-time clock.

The Quark is still a compute and communications platform, so any analog support would be off-chip. The PCI Express Gen 2 opens up a number of possibilities such as display or graphics support. Overall, the Quark is a good starting point for a family of SoCs.

The Quark die is one-fifth the size of an Atom, but limitations come with the smaller size. The chip has the x86 virtual memory management support. System virtualization is not part of the package, but that is not as necessary in embedded applications targeted by the chip. This approach seems reasonable since it also requires one-tenth the wattage of an Atom.



1. Intel's Quark X1000 is a 32-bit, Pentium-class, low-power SoC designed for the Internet of Things.

2. The Aruduino Galileo board is a Quark X1000 platform designed for students and developers.

The platform, then, definitely can target mobile and wearable products. Of course, the Quark will have lots of competition from other SoCs including those based on Arm and MIPS cores.

The Quark was announced at this year's Intel Developer Forum (IDF13), but it was presented as a synthesizable SoC platform that Intel customers could add their intellectual property (IP) to even though it would have to be built in Intel fabs *(see "IDF 2013 And Windows 8 Revisited" at electronicdesign.com)*. The X1000 is essentially the base for this design.

AN X86 ARDUINO

The Quark is currently available on the Arduino Galileo board, which is designed for developers and students *(Fig. 2)*. It is compatible with Arduino shields. The Arduino software tools, including Sketch, will be designed to work with the platform, but these are only starting points for students.

The board additionally exposes the USB, Ethernet, and PCI Express, which is via a half-card, mini-PCIe socket. The system boots from 8-Mbyte SPI flash. And, it boasts 256 Mbytes of DDR3 DRAM plus 11 kbytes of EEPROM.

The Galileo will have to compete with many of the 32-bit Arduino-compatible alternatives such as those based on Arm Cortex microcontrollers and Microchip's 32-bit MIPS platform. Many can run Linux or other operating systems. The Galileo runs Linux.

At this point, the Internet of Things comprises multilevel gateways. The Quark is Intel's lowest layer. We will have to see if the bar is low enough. ed

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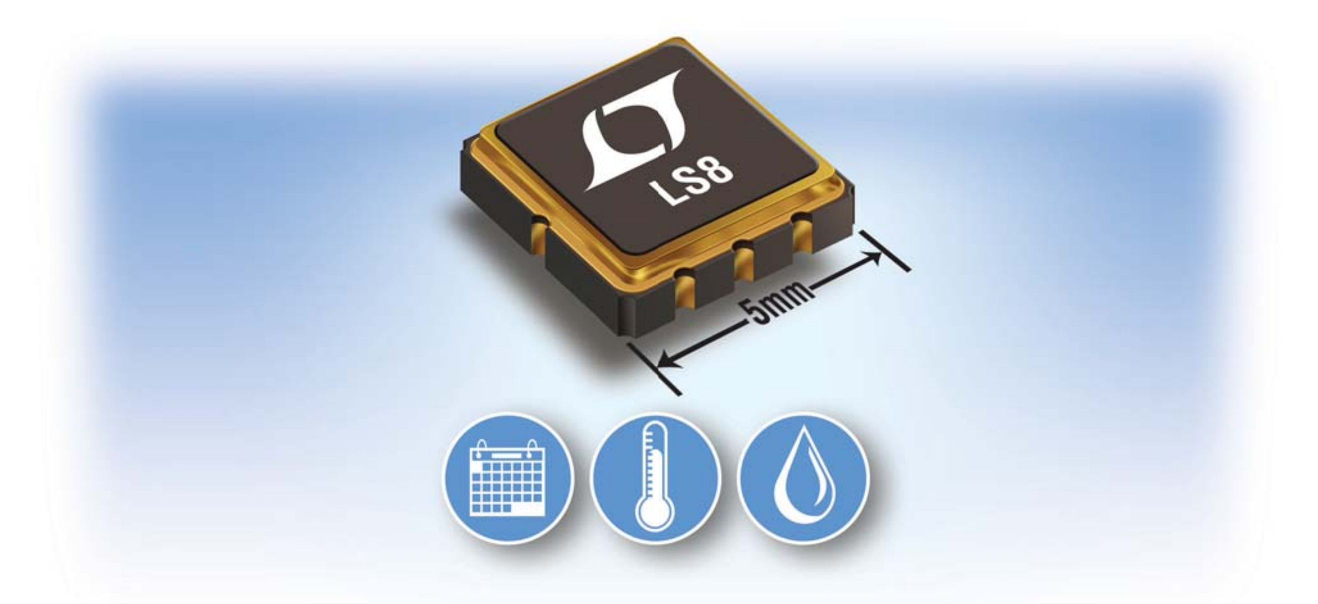

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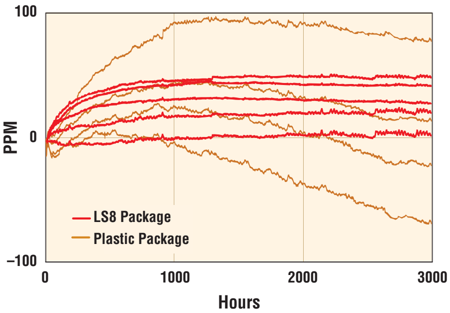

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A Special Section to PENTON'S DESIGN ENGINEERING & SOURCING GROUP OCTOBER/NOVEMBER 2013

1. One-half of the CHAMP-WB-DRFM consists of the CHAMP-WB 6U OpenVPX base board assembly.

SINGLE BOARD CAPTURES, Digitizes DC to 6 GHz

DENIS SMETANA Product Marketing Manager, GARY GONCHER, System Architect

CAPTURING AND digitizing broad swaths of spectrum is now an essential function in many applications. Because of the large amount of digital processing now performed in many systems, platforms ranging from electronic-intelligence (ELINT) and signal-intelligence (SIGINT) to radar and electronic-warfare (EW) systems can all benefit from fast digitizers with broad, instantaneous bandwidths. The CHAMP-WB-DRFM OpenVPX board from Curtiss-Wright (www.cwcdefense.com) in partnership with Tektronix Component Solutions (www.tektronix.com) is the first product to address this challenge at the board level.

This new offering uses an analog-to-digital converter (ADC) from Tektronix that samples at 12 GSamples/s to digitize a bandwidth of 6 GHz. This single-board solution also features a 12-GSamples/s digital-to-analog converter (DAC) at its output, and a Virtex-7 field-programmable gate array (FPGA) from Xilinx (www.xilinx.com) working at 12 GSamples/s.

The CHAMP-WB-DRFM VPX board consists of Curtiss-Wright's CHAMP-WB baseboard assembly (*Fig. 1*) with the FPGA supported by 8 GB of DDR3L SDRAM and the TADF-4300 Enhanced FMC mezzanine card (*Fig. 2*) with the ADC and DAC; together they form the CHAMP-WB-DRFM (see Table). As the 6-GHz bandwidth of the CHAMP-WB-DRFM is nearly three times that of its nearest board-level competitor, it offers possibilities unavailable before. For example, EW, SIGINT, ELINT, and other surveillance systems must scan over a broad range of frequen-

(continued on p. 30)

GTRI STUDIES BLAST EFFECTS ON SOLDIERS

JACK BROWNE /Contributing Editor

AS IMPROVISED explosive devices (IEDs) have become more prominent on the battlefield, it has become correspondingly imperative for the United States Armed Forces to fully understand the destructive effects of these weapons on their troops. GE Intelligent Platforms (www.ge.com) has been working with the Georgia Tech Research Institute (GTRI) to gain more insight into the neurological injuries that can sometimes result from IEDs.

GTRI was made a part of the Integrated Blast Effects Sensor Suite (I-BESS) program by the US Army Rapid Equipping Force (REF). The program was created to record IED blast information that can later be analyzed by doctors; the hope is to eventually help diagnose and determine the best way to treat soldiers with concussions or brain injuries. Sensors are located throughout military vehicles, as well as on soldiers' seats, to capture data during a traumatic event. In addition, soldiers carry smartphone-sized data recorders and a variety of sensors to gather additional data.

(continued on p. 8)

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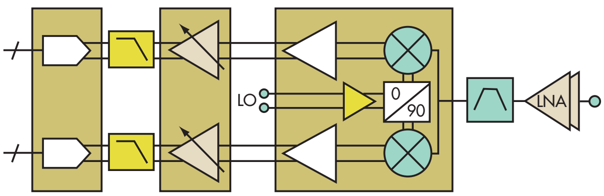

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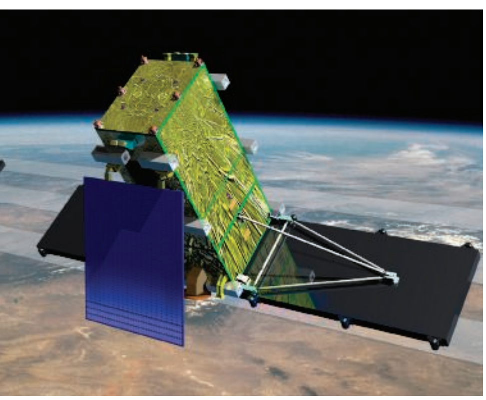

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Radar Systems Now Rely On Data Converters

RADAR SYSTEMS are vital not only to modern warfare strategies, but also increasingly in commercial applications—collision-avoidance systems in automobiles, to give one example. Although the electronic design required for high-performance radar systems still includes some of the most elegant architectures found in RF/microwave applications of any kind, data converters are more and more replacing this functionality. Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are taking on more of the signal generation and analysis in radar systems, with no tradeoffs in reliability.

On the receive side, a high-speed ADC is typically linked to each channel of a receiver's intermediate-frequency (IF) section; this provides conversion of received analog pulsed radar signals to digital signals for processing with digital signal processors (DSPs) and other digital components. With the performance levels possible from high-speed semiconductor processes—among them, the silicon-germanium (SiGe) BiCMOS process from IBM (www.ibm.com)—ADCs and DACs routinely operating across 10-GSamples/s sampling rates and 5-GHz bandwidths are available for the analog/digital interface section of radar receivers and transmitters, respectively. This totally alters the design approach of these radar systems from years past.

As with modern test equipment, such as spectrum analyzers—modern radar systems are as much defined by their digital circuitry as by their analog RF/microwave circuitry. The bandwidth and sampling rates of the ADCs set the limits for the radar's IF stage, while the resolution of the ADCs (in bits) determines the resolution of the radar system receiver. Similarly, the DACs help generate complex modulated pulsed signals for a radar transmitter, relying on frequency upconversion and trusted RF/microwave components (such as amplifiers and filters) for the signal path to the radar system's transmit antennas.

Radar technology is, of course, used in a wide array of military applications, but also in any number of non-defense-related ones. These include the aforementioned automobiles, along with weather radars, aircraft anticollision systems, ocean surveillance, and even NASA's topographical mapping of the solar system. But for radar systems to increase their reach—whether in military applications or even in potentially high-volume commercial applications—the performance/price ratio that ADC and DAC customers have enjoyed in recent years will require a continued boost. de

JACK BROWNE, *Technical Contributor*

(continued from p. 1)

GE Intelligent Platforms has been able to help the cause by providing a pre-configured, pre-validated, pre-tested commercial-off-the-shelf (COTS) Rugged System. This is being used by GTRI as the main system for collecting data from the aforementioned sensors. By providing the system in such a short time, GTRI benefitted from savings in time and cost compared to developing a similar system independently. These packaged, pre-validated computer systems are suitable for use in applications requiring high reliability, such as in unmanned vehicles, ground vehicles, and manned aircraft. The systems will be used as a small, ruggedized data collection box housed within the vehicle compartment.■

Georgia Tech Research Institute (GTRI) has been studying the effects of explosions on soldiers, using a COTS Rugged System for data collection. [Photo courtesy of GE Intelligent Platforms (www.ge.com).]

Navy Sends Missiles Over The Horizon

EARLIER THIS summer, the United States Navy fired two interceptor missiles from an over-the-horizon launch position, successfully engaging a pair of cruise-missile targets. The test involved two Standard Missile-6 (SM-6) interceptors from Raytheon Co. (www.raytheon.com), fired from the US Navy's *USS Chancellorsville* at two BQM-74 drones. The test confirms that the SM-6 missiles are capable of providing extended range protection against fixed- and rotary-wing aircraft, unmanned aerial vehicles, and cruise missiles as part of the Naval Integrated Fire Control-Counter Air (NIFC-CA) mission area.

Raytheon delivered the first SM-6 missile this past February from its production facility at Redstone Arsenal (Huntsville, AL). A Defense Acquisition Board approved full-rate production of the SM-6 in May. The SM-6 employs active and semi-active guidance modes and advanced fusing techniques, with guidance-control capabilities developed in Raytheon's Advanced Medium-Range Air-to-Air Missiles. ■

Advanced Super Hornet Shrinks From Radar

The Advanced Super Hornet incorporates numerous improvements over earlier aircraft versions to increase its range and reduce its radar signature. [Photo courtesy of Boeing Co. (www.boeing.com).]

AMONG THE improvements made on the Advanced Super Hornet by Boeing Co. (www.boeing.com) and partner Northrop Grumman (www.northropgrumman.com) are a harder-to-detect radar signature and a much greater combat range. This latest version of the fighter aircraft includes conformal fuel tanks (CFTs), an enclosed weapons pod (EWP), and radar signature enhancements. The improvements can be included on new jets or retrofitted on existing Block-II Super Hornet aircraft. Recent tests on the new fighter are indicating that the aircraft should be able to outperform threats for many decades.

The Advanced Super Hornets were tested during 21 flights from St. Louis, MO, and Patuxent River, MD. The EWP and improvements to the aircraft's radar signature resulted in a 50% reduction in radar signature compared to the US Navy's stealth requirements for the current Super Hornet. The tests also showed that the CFTs increase the jet's combat radius by up to 130 nautical miles, for a total combat radius of more than 700 nautical miles. The improvements are designed to ensure that the Advanced Super Hornet outpaces enemy aircraft and defenses through 2030 and beyond. ■

MIM Diodes Pave Way For Higher-Speed Circuits

RESEARCHERS IN the College of Engineering at Oregon State University have made advances in metal-insulator-metal (MIM) diodes that could eventually render silicon-based integrated circuits (ICs) obsolete, at least for high-speed, high-frequency applications. The diodes are formed of two conducting metal layers with two insulator layers in between. Rather than moving through insulating material such as silicon, electrons will "jump" from one conductive layer to another, with corresponding increases in speed and frequency.

Essentially a novel approach to electronic circuits, the research findings on these diodes were published in *Applied Physics Letters*, a publication of AIP Publishing LLC (apl.aip.org). According to this report, the step tuning of electrons through the diode could be made possible with the addition of a second insulator layer, forming a metal-insulator-insulator-metal (MIIM) diode. The multiple-insulator-layer approach also allows precise control of diode asymmetry, non-linearity, and rectification at lower voltages.

"This approach enables us to enhance device operation by creating an additional asymmetry in the tunnel barrier," says John F. Conley, Jr., a professor in the OSU School of Electrical Engineering and Computer Science. "It gives us another way to engineer quantum mechanical tunneling."

The MIM diodes were introduced three years ago by researchers at OSU in Corvallis, OR, and they are now seeking practical applications for the devices. Research on the MIM/MIIM diodes was supported by National Science Foundation grants, numbers DMR-0805372 and CHE-1102637, and Army Research Laboratory grant number W911NF-07-2-0083.■

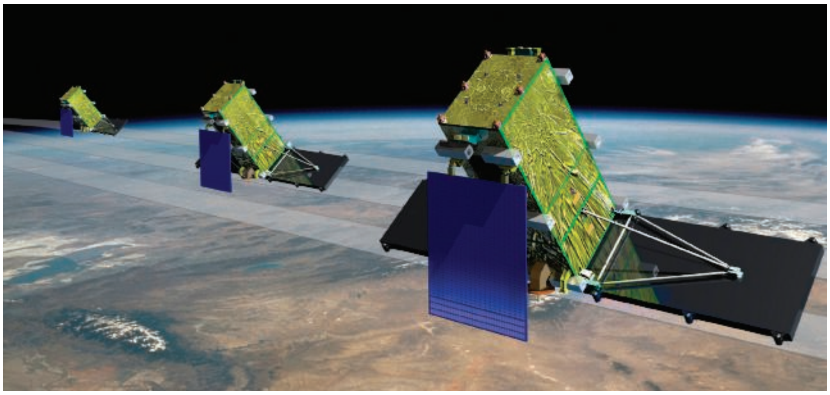
MM-Wave Technology Aids Security Scanner

THE ALLCLEAR® handheld screener is now capable of detecting a wide range of materials on a person's body, including metal, ceramics, plastics, liquids, gels, powders, and paper, by applying patented passive millimeter-wave technology. Developed by Microsemi Corp. (www.microsemi.com), the AllClear handheld screener incorporates a metal detector that can also identify those other materials.

Suitable for security and loss prevention applications, the battery-powered screener operates by detecting extremely small changes in naturally produced millimeter waves caused by objects concealed on the body. It works without emitting high-frequency radiation and without producing an image. This allows operators to detect concealed objects without revealing anatomical details, to maintain the privacy of the scanned individual. The detector reads differences in energy levels between a human body and emissions from objects on a body, for rapid detection of concealed objects, such as weapons.

According to David Hall, Vice-President and General Manager of Microsemi's RF Integrated Solutions group: "Microsemi's patented passive millimeter technology is a safe and effective alternative to radiation-based screeners and protects the privacy of people being screened. It allows the operator to detect a far broader range of objects than conventional metal detectors, including non-metallic contraband such as narcotics, plastic explosives, electronics, and more." The scanner is useful for commercial warehouse scanning, for screening at military and government checkpoints, and for high-security checkpoints, such as nuclear facilities and chemical plants.■

JIB Antennas Will Fly On Canada's RADARSAT



LIGHTWEIGHT JIB antennas from Northrop Grumman Corp.'s (www.northropgrumman.com) Astro Aerospace business unit will be a part of Canada's RADARSAT Constellation Mission (RCM). Planned for launch in 2018, the RCM project seeks to provide Canada with new maritime identification capability.

Astro Aerospace will provide 13 self-deploying, monopole JIB antennas as part of an Automated Identification System (AIS) being added to the three identical radar-imaging satellites. The satellites will provide C-band radar data to RADARSAT-2 users and add new applications available by way of the three-satellite constellation.

The JIB antennas bring a number of improvements to the satellite synthetic-aperture radar (SAR) system, including faster recurring area coverage of Canada and reduced risk of a service interruption. The antennas feature an adaptable configuration that can be tailored to specific applications. They are available with monopole diameters from 0.5 to 1.375 in. and lengths as long as 25 ft. For the RCM AIS application, the antennas are stowed in a compact 4.0 x 4.0 x 2.5-in. canister. ■

GPS Source To Supply Receiver Devices

GPS SOURCE (www.GPSSource.com) has received an indefinite-delivery/indefinite-quantity (IDIQ), firm-fixed-price contract from the Army Contracting Command, Aberdeen Proving Ground in Maryland for its Global-Positioning-System (GPS) receiver-based Defense-Advanced-GPS-Receiver (DAGR) devices. The indefinite-delivery/indefinite-quantity, firm-fixed-price contract is worth as much as $16.6 million. It is for products such as the GLI-FLO DAGR distributed device (DD3) that is designed to replace the position, navigation, and timing (PNT) role currently required of a DAGR or other positioning devices within a fixed vehicle platform. The GLI-FLO is designed as a single, secure access point to multiple devices requiring PNT data on a fixed vehicle platform, to meet the needs for saving space, weight, and power (SWaP). ■

Wyle Wins Award To Analyze Ground Systems and Vehicles

WYLE HAS been awarded a task order worth $39.9 million from the Defense Technical Information Center's Reliability Information Analysis Center to improve US Army ground systems and vehicles. The contract is to provide engineering and logistical analysis to improve the reliability of US Army ground combat systems, tactical wheeled vehicles, associated subsystems, and related test equipment and infrastructure, as well as to also help lower life-cycle costs for the equipment.

Under the award, Wyle (www.wyle.com) will provide support to the Program Executive Office for Combat Support and Combat Service Support and the Program Executive Office for Ground Combat Systems. Both are located at the US Army TACOM Life Cycle Management Command in Warren, MI.

Wyle will examine maintenance practices, as well as logistics structured reliability and maintainability engineering to refine and improve sustainability initiatives. The company will work to support the development, integration, sustainment, and demilitarization of ground combat systems, combat service support systems, tactical wheeled vehicles, and force projection equipment (including various ground vehicles). ■

RUSSELL J. HOPPENSTEIN | Systems and Applications Manager

Digital Correction
Revives Direct-Conversion Receivers

Direct-conversion receivers can benefit from performance improvements and flexibility by applying digital correction with commercially available digital components.

NEARLY 20 years ago, many systems designers began to replace superheterodyne transmitters with direct-conversion architectures. The shift was facilitated by the emergence of high-performance direct-conversion modulators. With the availability of direct-conversion modulators that were stable and reliable—and that met the necessary requirements for linearity and output noise—the transition from superheterodyne transmitters accelerated.

Compared to superheterodyne transmitters, direct-conversion transmitters provided numerous benefits, including reductions in space and cost. The direct-conversion approach also eliminated the need for the transmitter's intermediate-frequency (IF) stage, along with its IF synthesizer, amplifiers, and mixers. In addition, it provided the flexibility to work with a variety of signal bandwidths and output RF signals without having to radically change the component lineup. On the negative side, the direct-conversion modulator yielded some detrimental effects, including unwanted sideband and carrier feedthrough.

Superheterodyne receivers have not made the same transition to the direct-conversion architecture as transmitters, even though they would enjoy many of the same benefits. In a transmitter, designers know in advance the type of signal to be processed, whereas the signals are unknown with a receiver. A receiver's antenna may detect desired signals as well as many unwanted signals.

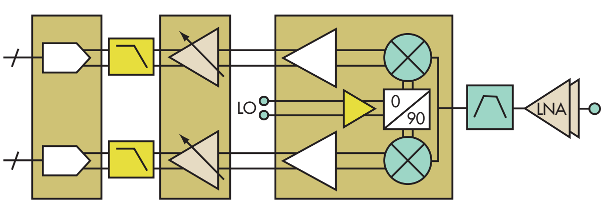
High receiver sensitivity calls for the use of narrowband IF surface-acoustic-wave (SAW) filters to eliminate unwanted signals and interference. Direct-conversion approaches can be challenging for modern systems that must operate with a variety of signal bandwidths and within a variety of frequency bands while also reducing costs. By examining some of the troublesome issues with direct-conversion architectures, it may be possible to minimize or eliminate their effects to encourage the use of the direct-conversion approach.

Fig. 1 shows a block diagram of a direct-conversion receiver. The key component is the demodulator, which handles direct conversion of RF signals to baseband signals. With no narrowband channel filter in this architecture, the performance of the demodulator is critical.

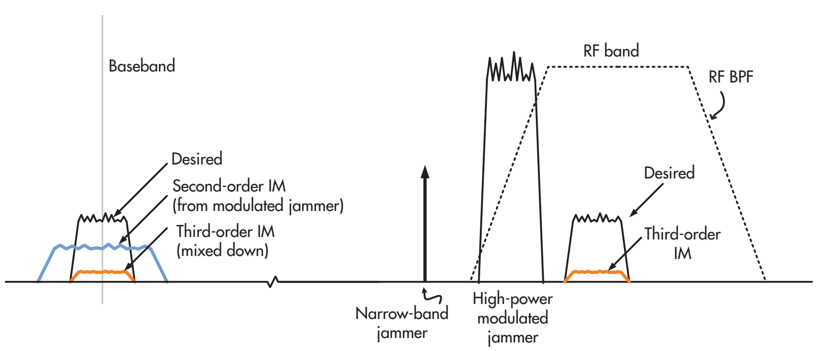
The direct-conversion architecture provides flexibility to a designer. The signal bandwidth and RF can easily be adjusted so that a single design can process single-carrier narrowband signals as well as multicarrier wideband signals, such as those used for fourth-generation (4G) Long-Term-Evolution (LTE) cellular-communications systems. A direct-conversion architecture can work in different RF ranges simply by changing local oscillator (LO) frequencies and the input RF band filter.

In this direct-conversion example, input signals are divided into their quadrature components by the demodulator and fed to a dual analog-to-digital converter (ADC). Though there are two channels, each channel represents one-half of the original signal bandwidth. For a data converter, the smaller bandwidth requires a lower sampling rate to process the signals. For example, given a 100-MHz signal bandwidth for a superheterodyne architecture with IF of 440 MHz, an ADC with better than 200 MSamples/s sampling rate and more than 490-MHz input bandwidth is required.

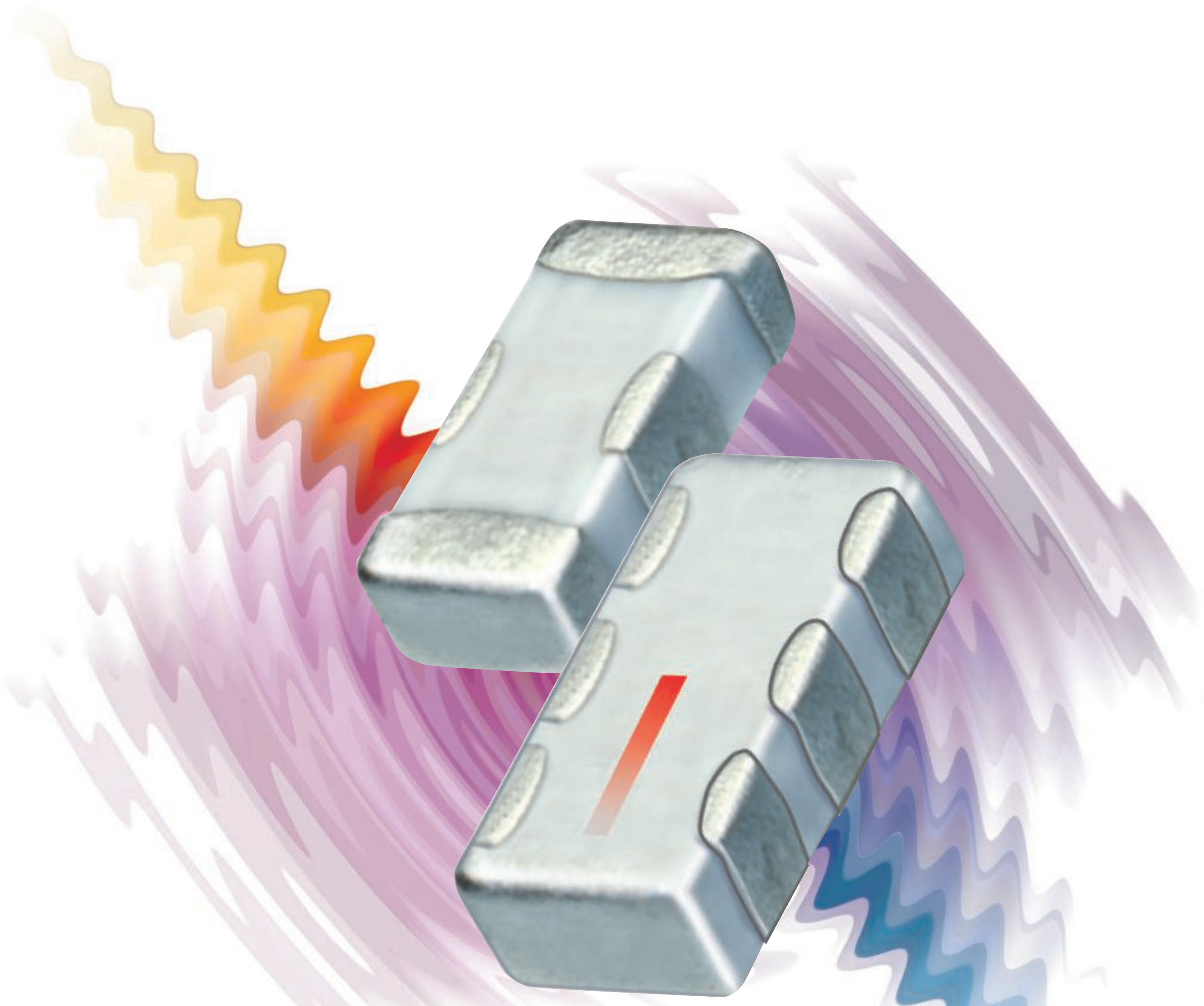
A single 250-MSamples/s ADC with 500-MHz input bandwidth would suffice operating in the fourth Nyquist zone. But in a direct-conversion architecture, RF signals are split into in-phase (I) and quadrature (Q) paths with 50-MHz bandwidth for each. A 125-MSamples/s



1. This block diagram shows the basic components in the direct-conversion receiver.



2. This diagram shows the impact of intermodulation on a direct-conversion receiver.



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www.minicircuits.com P.O. Box 35166, Brooklyn, NY 11235-0003 (718) 934-4500 sales@minicircuits.com dual ADC operating in the first Nyquist zone would suffice in this case, a less-expensive, higher-performance option than the superheterodyne approach.

Dynamic range is an important parameter for a receiver system. Receiver noise figure establishes sensitivity, or the low end of the dynamic range, and input third-order-intercept point (IIP3) helps set a limit on the highest level signals that can be handled. The combination of these parameters establishes the receiver dynamic range. Receivers typical employ some form of gain control to adjust dynamic range for different conditions. When interference signals are present, the gain is reduced to improve linearity and prevent interference signals from saturating the front end of the receiver. When no interference signals are present, the gain can be boosted for the best noise figure and sensitivity.

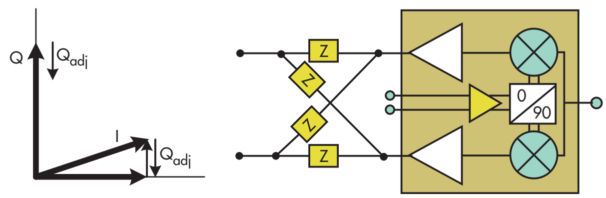
The effects of second-order intermodulation products must be understood when working with a direct-conversion receiver architecture—moreso than with a superheterodyne architecture. Filtering can generally reduce third-order intermodulation concerns, but second-order tones are generated at the sums and differences of interference tones. If a blocker tone is a wideband signal, its own internal difference terms will be located close to DC (i.e., 0 Hz), or the location at which the demodulator mixes the desired signal.

Regardless of the RF signals, these wideband jammers always produce signal products near DC. Hence, it is imperative to have very good IIP2 performance in a direct-conversion I/Q demodulator *(Fig. 2)*. Because a superheterodyne architecture mixes signals to an IF range that is then filtered, second-order terms are not a concern as with the direct-conversion approach.

Impairments related to carrier feedthrough and sideband rejection in a transmitter have counterparts in a direct-conversion receiver. Within a quadrature modulator, DC imbalances in the baseband I/Q input signals can cause a portion of the carrier (i.e., the LO) to feed through to the output. A direct-conversion receiver is susceptible to the same phenomenon, though the result occurs at 0 Hz (i.e., DC). The DC imbalances between the I and Q channels result in a DC offset tone at the output, which can impact ADC dynamic range. Ideally, an ADC processes small, low-level signals while not saturating with high-level blockers. A DC offset level can steal some of that dynamic range.

In a transmitter, sideband suppression refers to the amount of suppression of an

unwanted image signal. In a receiver, a similar parameter is referred to as image rejection. If the amplitude and phase in the I and Q signal paths are perfectly balanced, images are infinitely suppressed. But imperfections in the demodulator and the tolerances of the baseband circuitry lead to some amplitude and phase mismatch that result in unwanted image signals. Although difficult to measure, these image signals can result in signal degradation.



3. This simple diagram shows a circuit concept for analog image correction.

A 16-state quadrature-amplitude-modulation (16QAM) signal plot with a channel that has some amplitude and phase imbalances introduced in the I/Q channel, in theory, should appear as sharp dots for the symbols received, but the quadrature mismatch introduces errors which appear as a "cloud" around the desired point. This cloud leads to bit errors in the digital signals and becomes ever more critical as the constellation size is increased and the symbols are pushed closer together.

The DC output component is created from DC offset imbalances between I and Q output channels. The simplest solution for minimizing the unwanted content is to AC-couple the inputs to the ADC. A series capacitor blocks DC, but also creates a highpass filter effect that blocks some of the low-frequency signal. The capacitor can be chosen for a sufficiently high capacitance value to push the highpass corner frequency to a low value, within the kHz range, which is fine for any applications with no information in the very low-frequency range. Modern OFDM signals such as LTE and WiMAX signals have multiple subcarriers, but no subcarriers within the first few kHz in the center of the spectrum.

Other signal types contain information distributed throughout the entire spectrum and it may not be possible to filter out the first few kHz of information. In addition, the ADC may require a DC common-mode voltage for proper operation. As a result, DC coupling must be maintained and the DC offset balance adjusted so that the ADC's dynamic

range is not compromised. The DC offset can be balanced by injecting a DC signal at baseband that can be independently tuned on the I and Q paths to cancel out the DC component created by the imbalance. This technique makes it possible to reduce DC offsets to the millivolt range, where their impact is negligible. A simple summing amplifier on the output with a variable input DC level can be used to tune the DC offset. Some commercially available quadrature demodulators, such as the model TRF3711 from Texas Instruments (www.ti.com), integrate this capability to facilitate design simplicity.

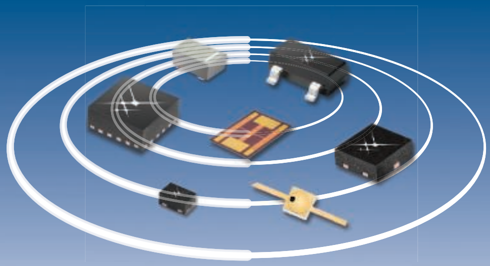
Signal image components occur due to amplitude and phase imbalances between the I and Q channels. The simplest amplitude adjustment can be made by providing a small amount of gain in each element. However, the phase component tends to be the dominant impairment.

Quadrature imbalance can be envisioned as two orthogonal signals skewed from their optimal position (*Fig. 3*). The I channel has some amplitude and phase imbalance compared to the Q channel. The I channel can be broken down into two vectors: One is the true in-phase signal and the other is a small component of the quadrature component. With this image in mind, some of the Q channel can be siphoned to the I channel side to compensate for that quadrature error term and thus, in theory, eliminate it completely.

The feedback of the I and/or Q side to the opposite channel can be adjusted in amplitude level fairly easily and used to compensate for both the amplitude- and phase-imbalance terms. The series compensation elements account for the amplitude imbalance. The crossover compensation elements minimize the unwanted orthogonal vector, which in essence corrects the phase imbalance. Image rejection performance generally can be improved 15 to 20 dB with this technique.

The analog techniques described previously for imaged rejection improvement are effective, but can be difficult to maintain over variations related to process, signal levels, and temperature. The receiver has one advantage compared to its transmitter counterpart for image rejection: The signal is already digitally captured by the ADC. The receiver can employ digital adjustment techniques that adapt in real time to the changing conditions. This approach performs better than analog methods, providing as much as 70-dB image suppression.

Orthogonal signals are defined as signals such that the dot-product sum of the components equal zero. A digital algorithm can be used to capture the quadrature signals and determine the quadrature errors between the signals. This is independent of the signal modulation, level, or bandwidth. From the error signal generated, an error correction term can be calculated to bring the signals back to orthogonal conditions. In a sense, this algorithm employs a digital technique similar to the analog one of siphoning some of the I or Q channel to the opposite path. The digital technique continuously monitors the digital signal and adjusts accordingly to improve the impairment.



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SKY67015-396LF	30–300	0.80	18.5	7.5	12.5	3.3 @ 18
SKY67151-396LF	700–3800	0.25	26.0	8.5	21.5	5 @ 80

Attenuator

Part Number	Freq. (MHz)	Control Accuracy (Bits)	Attenuation (dB)	Insertion Loss (dB)	Input $P_{1\,dB}$ (dBm)	Input IP3 (dBm)
SKY12343-364LF	10–4000	7	31.75	1.8	35	50

Limiter Diode

Part Number	Freq. (MHz)	Breakdown Voltage (V)	Insertion Loss (dB)	Max. Pulsed Input Power (dBm)	Series Resistance (Ω)	Capacitance (pF)	Recover Time (ns)
SMP1330-040LF	DC–600	20	0.3	70	1.5	0.26	1000

Switching PIN Diode

Part Number	Freq. (MHz)	Breakdown Voltage (V)	Insertion Loss (dB)	Series Resistance (Ω)	Capacitance (pF)	Carrier Lifetime (ns)
SMP1345-040LF	DC–6000	50	0.4	1.5	0.18	100

Schottky Diode

Part Number	Freq. (GHz)	Breakdown Voltage (V)	Video Resistance (Ω)	Capacitance (pF)	Forward Voltage (mV)
SMS7630-061	DC–100	1	5000	0.2	180

Varactor Diode

Part Number	Freq. (GHz)	Breakdown Voltage (V)	Q Factor @ 4 V	C_T @ 4 V (pF)	C_T @ 20 V (pF)
SMV2201–SMV2205 Series	DC–10	22	500	0.73 min. / 0.98 max.	0.18 min. / 0.33 max.

Switches

Part Number	Freq. (MHz)	Insertion Loss (dB)	Isolation (dB)	Input $P_{1\,dB}$ (dBm)	Input IP3 (dBm)	Switching Time (ns)
SKY12208-478LF	20–2700	0.3	45	47	70	85
SKY12211-478LF	50–2700	0.3	47	46	73	32
SKY13286-359LF	100–6000	0.35	34	39	–	500

Phase Locked Loop (PLL) Frequency Synthesizer

Part Number	Freq. (MHz)	Synthesizer	Divide-by	Input $P_{1\,dB}$ (dBm)
SKY73134-11	350–6000	Integer-N	1/2/3/4/8	4

Direct Quadrature Demodulator

Part Number	RF and LO Freq. Range (MHz)	IF Freq. Range (MHz)	Input IP3 (dBm)	Input $P_{1\,dB}$ (dBm)	I/Q Amplitude Imbalance (dB)	I/Q Phase Error (Deg.)
SKY73012	400–3900	DC–250	29	12	±0.3	1s

Low Drop-out (LDO) Linear Regulators

Part Number	Dropout Voltage (mV)	Output Voltage (V)	DC Output Voltage Tolerance (%)	Output Current (mA)	Quiescent Current (μA)
AAT3223IGU3.0T1	190	3.0	±2	250	1.1
AAT3223IGU3.3T1	180	3.3	±2	250	1.1

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A signal can be represented by its quadrature components:

$$S_0(t) = S_{0_I}(t) + j\cdot S_{0_Q}(t) \quad (1)$$

The actual signal can be represented by the ideal signal with error terms for the relative amplitude and phase imbalance between the channels:

where:

KI = the normalized amplitude of the I channel (= 1);

KQ = the normalized amplitude of the Q channel relative to the I channel; and

ψ_{err} = the relative quadrature phase error relative to the I channel.

The goal of the digital correction technique is to sample elements of the real signal and estimate the amplitude and phase imbalance from those samples.[1-3] With this information, the signal can be manipulated to correct the signal's quadrature nature and repair the original signal closer to its ideal components.

From samples of the real signal the amplitude and phase error terms can be estimated by Eq. 3. The counting variable L was selected to determine the number of samples that are used to estimate the error.

An example can illustrate the capabilities of this technique by using the simplest of quadrature signals: sine and cosine waveforms:

$$\begin{aligned} S_{0_I}(t) &= \cos(2\cdot\pi\cdot f_c\cdot t) \\ S_{0_Q}(t) &= \sin(2\cdot\pi\cdot f_c\cdot t) \end{aligned} \quad (4)$$

For this example, the carrier frequency was selected at 1 MHz, and the sampling rate at 200 MSamples/s. The error terms are arbitrarily selected to be KQ = 1.2 and ψ_{err} = 2 deg. By applying the estimation calculation shown earlier, and with a counting variable arbitrarily selected at 600 samples, the solutions to the estimation equations are K_{est} = 1.198 (which is equivalent to 0.166% error when compared to actual performance) and θ_{est} = 2.4 deg. In this example, the amplitude error can be estimated very accurately. The phase error is significantly improved, with only 0.4 deg. absolute error from the true error value.

Two variables can impact this approach. One is the length of the counting variable. A higher value provides a larger signal sample and provides better estimation. However, a longer counting sequence requires more processing power and longer convergence time. With the above example and the same formulas, the amplitude percent error and the absolute phase error are calculated as functions of the counting variable length.

The absolute phase error is rather impervious to the length of the samples, primarily due to the consistent periodic nature of the signals used in this example. The amplitude error, however, is impacted. With 100 samples, the amplitude percent error is about 1%, but drops significantly as the length is increased. The impact of the counting variable length is dependent upon the type of signal, sampling rate, and periodicity of the signal.

Another variable that impacts the estimation accuracy is the initial starting error. In the next example, the amplitude imbalance is varied from 0.1 to 1 dB, and the phase imbalance is varied from 0.5 to 5 deg. The estimation formulas are used in conjunction with an arbitrary counting variable length of 500 to illustrate the accuracy

$$\begin{bmatrix} S_I(t) \\ S_Q(t) \end{bmatrix} = \begin{pmatrix} KI & 0 \\ -KQ\cdot\sin(\psi_{err}) & KQ\cdot\cos(\psi_{err}) \end{pmatrix} \cdot \begin{bmatrix} S_{0_I}(t) \\ S_{0_Q}(t) \end{bmatrix} \quad (2)$$

$$Kest = \sqrt{\frac{\sum_{k=0}^{L} \left[S_Q(k)\right]^2}{\sum_{k=0}^{L} \left[S_I(k)\right]^2}} \qquad \Theta est = \frac{\sum_{k=0}^{L} \left[S_I(k)\cdot S_Q(k)\right]}{\sum_{k=0}^{L} \left[S_I(k)\right]^2} \quad (3)$$

as a function of inherent residual error. The amplitude correction is consistently accurate, regardless of inherent error. But phase correction is dependent upon the inherent phase and amplitude imbalances.

For the case where the inherent phase error is 5 deg. and the amplitude imbalance is 1 dB, the estimation formulas do a poor job and the resultant phase error is barely improved. Amplitude improvement is still consistent. Compare the response with a case where the inherent phase imbalance is 1 deg. and the amplitude imbalance is 0.2 dB. Under this condition, the phase error after correction is only 0.2 deg.

This example illustrates the performance improvement possibilities of digital correction and a digital algorithm. However, this technique generally works well only for static imbalances, not imbalances that change with respect to offset frequency. In an actual receiver, there are frequency-dependent terms that result primarily from filter elements or parasitics. If the frequency-dependent terms are small, static compensation can be very effective.

As an example, the reference design for the model TSW6011 from Texas Instruments includes a receiver with a direct-conversion demodulator and ADC, along with digital processing that uses a proprietary blind correction algorithm. System performance provides 60-to-70-dB image rejection with wideband signals.

If further improvement is required, the digital algorithm needs frequency-dependent terms within its filter taps. This requires a more complex approach with some level of calibration (or "training") to give the algorithm the input conditions and bounds required for implementing the correction. With this level of complexity, image rejection of 80 dB or more can be achieved.[4]

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4. For additional information, refer to the TSW6011 reference design and TRF3711 datasheet, available from www.ti.com.

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JOHN HANSEN | Senior Applications Engineer

Spectrum Simulation
Helps Verify System Performance

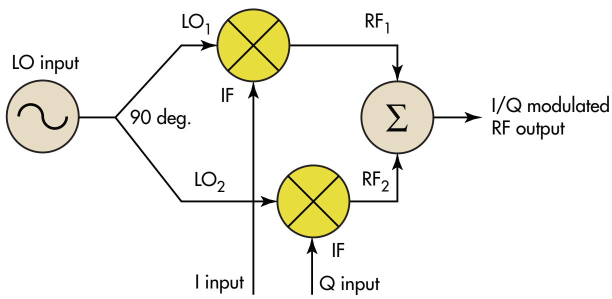
The use of high-performance AWGs and RF/microwave frequency-upconversion circuitry can create realistic signal environments for evaluating electronic equipment.

SPECTRUM IS an invaluable resource, and it is growing more crowded each day. An RF/microwave spectrum overcrowded with too many signals can make it difficult for some sensors and systems to perform optimally. One solution is to locate a source of interference and either eliminate it or develop a filter to remove it from a system's signal path. But many times, the cause of degraded performance may be more than one interference signal.

Taking into account the constant, legal signal activity from such sources as mobile telephones, frequency-modulated (FM) radios, and automotive radar systems—and how these signals can mix and interact—there is no recourse but to design systems that minimize their susceptibility to such interference. Also, in wideband, multiple-channel systems, it may be signal distortion from the system itself that is the cause of that very system's reduced performance. Spectrum simulation can provide an effective means of analyzing problems caused by too many signals and finding solutions.

Some systems, such as signal-intelligence (SIGINT), geolocation, and counter-improvised-explosive-device (counter-IED) systems, must operate in spectrally cluttered environments—yet still be capable of detecting, identifying, and (in some cases) suppressing signals near a broadband noise floor. Understanding the interaction of different signals within the operating spectrum can be a critical part of achieving optimum performance from these types of systems.

Of course, it is not always possible to perform spectrum measurements in some types of operating environments, and the availability of a wideband multiple-emitter signal environment that is controlled and repeatable could be a tremendous tool for system developers. Fortunately, methods exist for accurate and realistic spectrum simulation in the laboratory for signal environments from DC through and beyond Ka-band frequencies. One of the key tools for simulating these realistic signal environments is the arbitrary waveform generator (AWG).

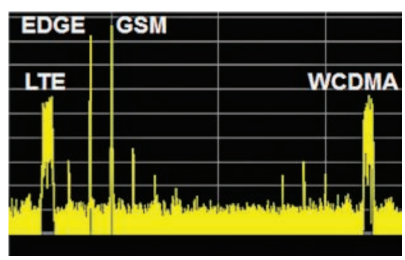


1. This diagram shows the main function blocks of an I/Q modulator.

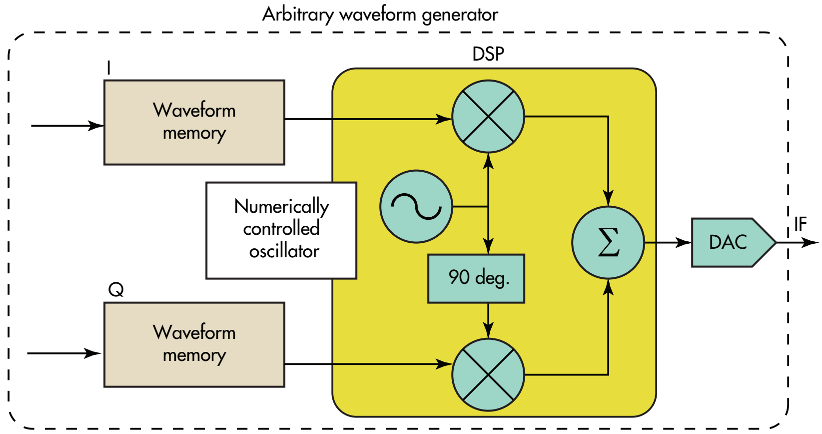
Vector modulators are important instruments for creating a signal environment. They provide the means of imposing both amplitude and phase changes on a signal's in-phase (I) and quadrature (Q) components, thus creating the I/Q-modulated signals widely used in modern communications systems. An I/Q modulator includes a 90-deg. phase shifter, two mixers, and an RF summing junction to generate the required arbitrary phase and amplitude of the modulated RF signal (*Fig. 1*). This makes it possible to modulate carriers to a bandwidth equal to that of the I and Q signals combined.

Numerous alternatives are available for creating I/Q baseband waveform files. These include MATLAB from MathWorks (www.mathworks.com), Visual Basic from Microsoft (www.microsoft.com), and other general-purpose software offerings, although many more specialized software packages are also available. For example, many test-equipment manufacturers offer software products that provide the capability to create very detailed waveforms for specific communications, radar, and electronic-warfare (EW) applications. One example of these more specialized tools is Signal Studio vector signal creation software from Agilent Technologies (www.agilent.com). It is available for the creation and analysis of a wide range of signal formats.

Digital-to-analog-conversion (DAC) technology has evolved to the point where wide instantaneous bandwidths and high resolution are available with the latest commercial-off-the-shelf (COTS) AWGs. An AWG provides the capability to generate virtually any waveform loaded into its memory and within the performance limits of its DAC circuitry. The right AWG makes it easy to create radar and communications emitters scattered throughout a synthetic test range that simulates thousands of cubic miles of airspace and across several GHz of spectrum.



2. Multiple commercial communications signals can be derived from a single AWG channel.

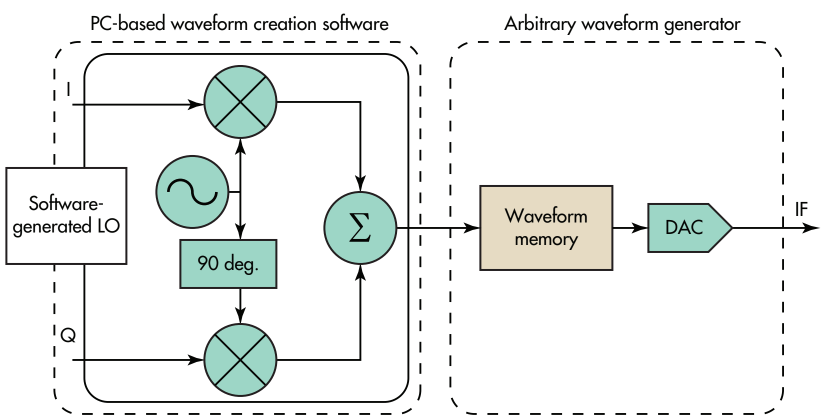


3. Real-time I/Q modulation can be orchestrated by means of AWG DSP firmware.

By programming multiple modulated signals into a single waveform file and loading that file into an AWG, it is possible to generate a composite signal and build a full electromagnetic (EM) signal environment across a given frequency band of interest (*Fig. 2*). Creating a waveform such as this can be done with an AWG and a general-purpose programming tool such as MATLAB, although other available methods can make the process much more straightforward.

Recent advances in integrating design simulation with precision wideband AWG hardware have made possible a new approach to creating and analyzing multiple-emitter test signals. Design simulation arbitrary resampling techniques can combine multiple signals into a single waveform, which is then downloaded into a high-precision AWG to generate a multiple-emitter test signal. Multiple signal inputs with different center frequencies, bandwidths, and sample rates can be combined and resampled to produce an output signal at a sample rate defined by the user, and that is compatible with the AWG. Using this capability, waveforms created mathematically can be combined with signals recorded from the field or from another signal simulation generator. The SystemVue software is a system-level modeling software program that enables such combinations.

Of course, this capability to combine signals in a single I/Q file for playback by an AWG does have its limitations. For each new modulated signal added to the file, the dynamic range of the composite signal decreases. Also, the noise floor rises and the realism of the signal diminishes. Additionally, combining sig-



4. I/Q modulation can be controlled via software when waveforms are created.

nals for the purpose of wideband spectral simulation quickly consumes AWG waveform memory since it is difficult to effectively employ memory conservation techniques such as waveform segmenting and sequencing. Ultimately, the solution to memory limitations will be to stream very large waveform files to the AWG over a high-speed bus from a deep memory source such as a redundant-array-of-independent-disks (RAID) configuration.

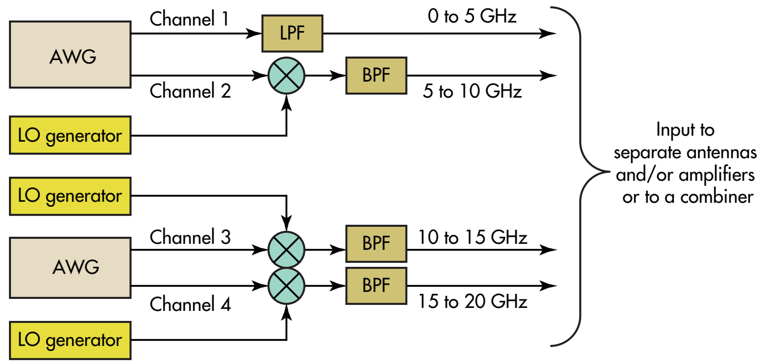
For analog I/Q modulation performed in hardware (*Fig. 1*), an AWG generates I and Q signals on separate channels that are fed to an I/Q modulator, which is often part of a vector signal generator (VSG). An advantage of the analog approach is the fact that since we are using two channels to create one baseband signal the bandwidth achieved for RF modulation is twice the maximum bandwidth of the individual AWG channels. For example, with a 500-MHz AWG, it is possible to generate a signal with 1-GHz modulation bandwidth. On the negative side, an analog I/Q modulator also generates a number of undesired distortion products, such as image signals and carrier feedthrough, which can only be reduced to a certain extent.

The I/Q modulation process can also be performed in software. Waveforms can be defined such that the waveform samples represent a vector signal that has already been modulated. This modulated IF signal is loaded into an AWG's memory and played out on a single channel of the AWG. Some advanced AWGs, such as the model M8190A 12-GSamples/s AWG from Agilent Technologies, incorporate the capability to perform software I/Q modulation in real time from files stored as I and Q samples.

When digital techniques are used, I/Q modulation is produced as the result of a mathematical operation, either in real time with the aid of a digital signal processor (DSP, *Fig. 3*) or in advance by means of software used to create AWG files stored in an AWG's electronic memory (*Fig. 4*). In the case where a digital technique is used, the I/Q modulation is carried out as a mathematical operation, either in real-time by a digital signal processor (*Fig. 3*) or ahead of time in the software used to create the AWG waveform file stored in AWG memory (*Fig. 4*). The result of this calculation is fed into a digital-to-analog converter (DAC) and upconverted by means of an RF/microwave frequency mixer or frequency multiplier together with an RF or microwave signal generator. With this approach, the images and LO feedthrough can be filtered out more easily as long as the IF is high enough. However, this method requires a higher AWG bandwidth.

One issue with both analog and digital modulation methods is compensating for the less-than-ideal frequency responses of the hardware components, including the DAC, the I/Q modulator, the signal generator, and the frequency mixer or multiplier stages. By measuring the amplitude and phase deviations of the frequency response across the bandwidth of interest, it is possible to include predistortion in the waveform file and loading it into the AWG's memory.

Some currently available AWGs offer good high-frequency performance with large bandwidths, but may lack the total range needed for EW, radar, communications, and other applications. Some form of frequency upconversion will be needed with the AWG. Unfortunately, the high conversion loss of an external mixer may result in a lower-level signal than when using analog wideband I/Q modulation within a signal generator to upconvert the signal. Use of an external mixer for upconversion may require an external amplifier to overcome the mixer's loss. In comparison, within the model E8267D microwave VSG from Agilent Technologies, modulated signals are multiplied to a desired carrier frequency; the output level is amplified, controlled, and calibrated, all within the instrument.



5. This diagram shows banded frequency upconversion from DC to 20 GHz.

For EM environment simulation, perhaps the best configuration for wideband upconversion is a banded upconversion arrangement as shown in *Fig. 5*. Multiple AWG channels are independently upconverted to the required band.

Modern AWGs provide a great deal of flexibility in creating realistic signal scenarios, whether with or without signal upconversion. By producing accurate signal environments in a laboratory, it is possible to evaluate other electronic products (such as communications devices and radar detectors) under real-world signal conditions. de

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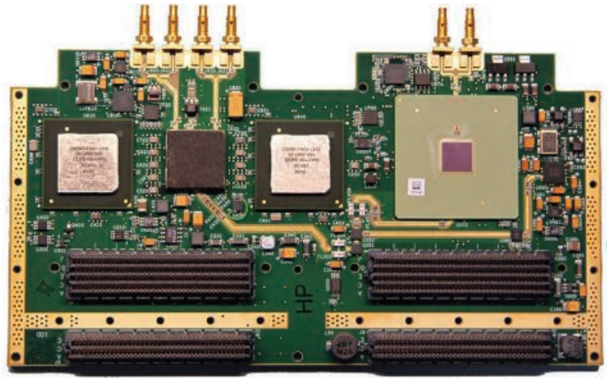


2. The other part of the VPX solution is the Enhanced FMC mezzanine card. The two parts combine to digitize an analog bandwidth of 6 GHz with 8-b resolution, provide signal processing using a Virtex-7 FPGA, and reconvert the signal to analog form using a 10-b DAC.

cies, so this capability to bridge the gap between the analog signal from the antenna and the point at which it enters the digital domain, without requiring a frequency downconverter for input frequencies to 6 GHz, helps reduce the size, weight, power consumption, and overall complexity of the receive path.

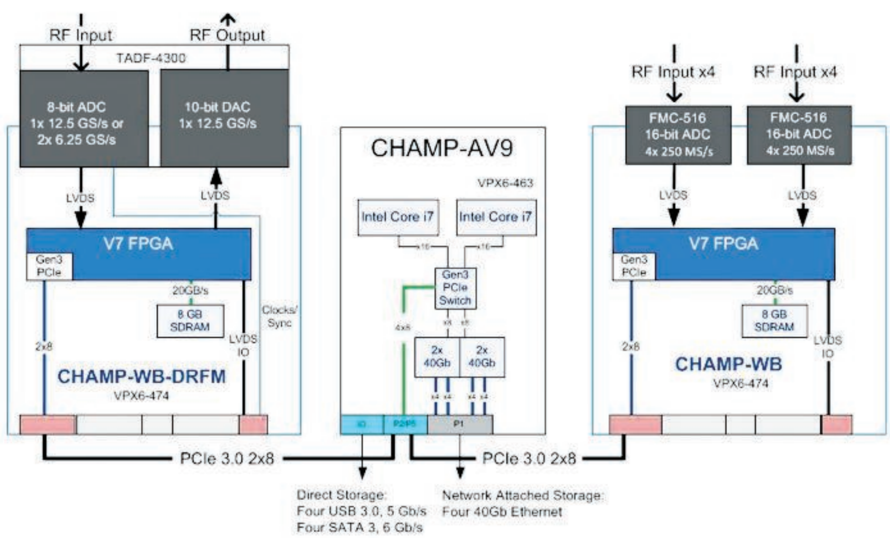
Such capability can also be useful in measurement applications such as radar test ranges where it can capture and externally store information using the 200 Gb/s of available backplane bandwidth. These tests are performed to judge the performance of an aircraft's radar, radar warning receiver (RWR), or EW system during multiple passes through the test range while being subjected to threats transmitted from the ground. Spectrum management and long-term surveillance are other applications.

Using the CHAMP-WB-DRFM as the core conversion and processing portion of a digital RF memory (DRFM) in a fighter aircraft as an example, the analog signal from an antenna or downconverter is directly digitized by the ADC on the TADF-4300 and sent via LVDS to the FPGA. Customer-supplied algorithms resident in the FPGA scour the captured signal stream to find the comparatively narrowband signals from an enemy radar.

If such signals are found, the FPGA performs the signal processing tasks required to confuse the radar, drawing on a threat library or other data stored in the synchronous dynamic random-access memory (SDRAM) on the CHAMP-WB-DRFM board. The output of the FPGA, which is a modified version of

THE CHAMP-WB, TADF-4300, AND FMC-516 SPECIFICATIONS AT A GLANCE.

CHAMP-WB	
FPGA digital signal processing	3600 25 x18 MACs (1 TFLOP)
FPGA general purpose processing	980,000 logic cells, 1.2 million FFs
FPGA internal memory	54 Mb
On-board memory	8 Gbytes
Memory bandwidth	19.2 Gbytes/s
Mezzanine bandwidth (per site)	154 Gb/s
Backplane data bandwidth	200 Gb/s
TADF-4300	
Maximum sampling frequency	12 GSamples/s
Bandwidth	6000 MHz
Number of channels	1 or 2
Resolution	8 b
Effective number of bits (30 kHz to 6 GHz)	More than 6.1
Spurious-free dynamic range (30 kHz to 6GHz)	More than 40 dBc
FMC-516	
Maximum sampling frequency	250 MHz
Bandwidth	500 MHz
Number of channels	4
Resolution	16 b
Effective number of bits (typ.)	11.3
Spurious-free dynamic range (typ.)	84 dB FS



3. Two CHAMP-WB-DRFM boards combined with a CHAMP-AV9 computing and signal processing board can perform low-and high-resolution signal detection, pre-and post-processing, and application processing.

the original input stream, is sent to the TADF-4300 and reconverted to analog form and then sent off-board to an upconverter, transmitter, and antenna.

A SIGINT scenario that requires higher-resolution samples of the signals detected and processed by the CHAMP-WB board and TADF-4300 is shown in *Fig. 3*. In this case, the high-bandwidth CHAMP-WB-DRFM board is complemented by a second CHAMP-WB board with two four-channel FMC-516 mezzanine cards that can capture as many as eight signals with 16-b resolution.

The CHAMP-WB-DRFM (shown on the left-hand side of *Fig. 3*) performs conversion and initial processing functions. The second CHAMP-WB shown (on the right-hand side of *Fig. 3*) has the two FMC-516 mezzanine cards, which have a narrower bandwidth but higher (16-b) resolution. With their eight independent channels (four on each card), they can receive the signals of interest identified by the first CHAMP-WB-DRFM at their original frequencies but analyze them in greater detail.

A system control board is required to coordinate the multiple receivers. The Curtiss-Wright CHAMP-AV9 computing and signal processing board performs this function, employing two fourth-generation Intel i7 quad-core processors with 16 GB of DDR3 SDRAM, a Gen3 PCIe switch, and interfaces to network-attached storage via its four 40-Gb/s Gigabit Ethernet interfaces. It also provides four USB 3.0 and four SATA 3 interfaces for local storage, displays, or other USB or SATA-enabled devices. With the combined eight cores of the i7 processors operating in parallel, the CHAMP-AV9 has more than 1.3 TFLOPS processing power, allowing a variety of analysis and data to and from each CHAMP-WB-DRFM board. All boards communicate via PCIe 3.0.

This three-board subsystem adds considerable functionality. Its 40-Gb/s Gigabit Ethernet and Gen3 PCIe interfaces allow the broadband data stream from the left CHAMP-WB-DRFM or the fine-tuned, higher-resolution "signals of interest" data stream on the right (or both) to be sent to and received from external RAID hard drives or solid-state storage modules.

The addition of a workstation or laptop computer and signal analysis software forms a complete system that performs broadband "direct-to-digital" signal capture; coarse and fine signal identification; pre-and post-processing; high-speed data transfer between all elements of the system; detailed waveform analysis and other RF measurements; and high-capacity data storage.

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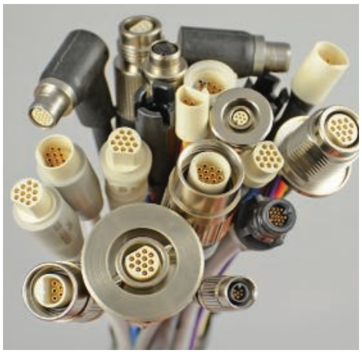

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