Electronic Design®

INNOVATORS
IN ELECTRONICS

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ALTECH CORP.

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Flemington, NJ 08822

ABOUT ALTECH

Altech Corporation is an established United States supplier of components and devices used in industrial control, instrumentation, medical and automation applications. Altech provides a very broad line of products that meet UL and international standards and are RoHS and REACH compliant. Altech's commitment to continuous quality management has been recognized since 1999 when they were awarded ISO 9001 certification.

Altech provides a multitude of services for customers. This starts with its employees, where product managers provide technical support and partner with customers in design assistance, ensuring the best solution for the application. Next, an efficient customer service department ensures that customers are informed with complete order information. Depending on the product, the versatile assembly department provides manufacturing, value-added, or customization services to expedite delivery. Altech's marketing department has been highly recognized for its catalogs, advertising, and website designs, while the sales department motivates the sales organizations throughout North America, ensuring product information is current and complete.

LARGEST Selection of DIN Enclosures

SERVING AUTOMATION AND CONTROL INDUSTRIES SINCE 1984

Altech's products meet UL and international standards, and all are RoHS- and REACH-compliant. Altech's commitment to quality and continuous quality management had been recognized since May 27, 1999 when it was awarded the prestigious honor of ISO 9001 certification. Since then, Altech has successfully gone through the recertification process and complies with ISO 9001:2015.

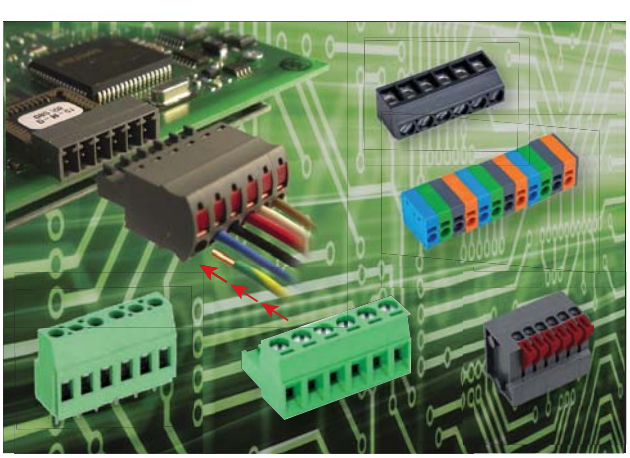
WIDE VARIETY OF AUTOMATION & CONTROL SOLUTIONS

The Altech product line includes miniature circuit breakers, busbars, DC-UPS devices, digital panel meters, DIN rail terminal blocks, printed circuit board terminal blocks, contactors, industrial relays, motor disconnect switches, pin and sleeve devices, receptacles, foot switches, relay modules, safety relays, slimline relays, solid state relays, push buttons, and pilot lights.

Also available are metal detection systems, ferrules, marking and engraving systems, fuses, power distribution blocks, corrugated tubes, liquid tight strain reliefs, programmable relays, digital multi-timer, test and measurement devices, LED panel lights, mechanical thermostats, panel filters, tower lights, and wire ducts.

OUR POLICY

Altech Corp.'s Company Policy remains to provide adequately stocked quality products at competitive prices. Superior customer service and delivery are maintained through a quality management system and continuous process improvement and by performing these services with honesty and integrity. All Altech employees are regularly trained in quality management systems, and as a team are committed to achieving these goals.



Altech®

Your Source for Automation & Control Components

Altech®

Top Components for Designing Electronics

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- SCREW TERMINAL BLOCKS
  - Wire Guard Type
  - Lift Type
  - Excenter Type
- SPRING TERMINAL BLOCKS
  - Push-In Type
  - Tension Spring Type
  - Lift Type

PLUGGABLE MULTI-CONNECTOR

- SCREW TERMINAL BLOCKS
  - Wire Guard Type
  - Lift Type
  - Excenter Type
- SPRING TERMINAL BLOCKS
  - Push-In Type
  - Tension Spring Type
- PIN STRIPS

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- Clamp-Type Test Probes
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- Measuring Sets

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- Integral PC Board Guides
- Many terminal to PCB connection options

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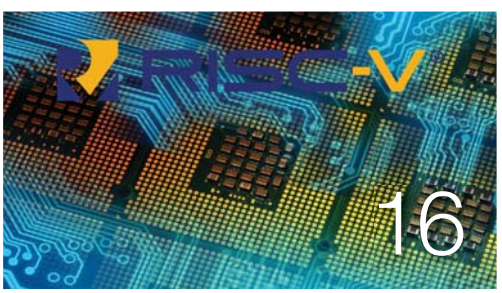

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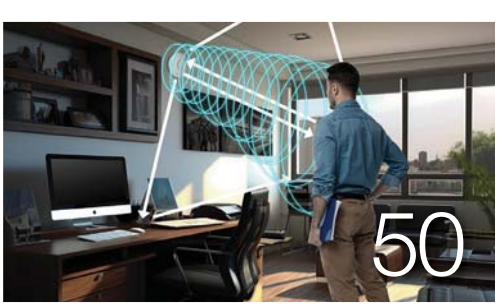

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Innovators, Disruptors, and AI

The never-ending upheaval of technology and electronics will continue unabated in 2024.

IN SOME WAYS, 2024 will be a repeat of 2023 but only worse when it comes to disruptive technologies and a changing landscape. This is in part due to the rapid maturing of technologies from artificial intelligence/machine learning (AI/ML) to GaN- and SiC-enabled power supplies. In the past, any disruption was due to planning for future possibilities.

These days, some of the guessing becomes foregone conclusions as these new technologies are available. Unfortunately, they're not standing still. Large-language-model (LLM) generative AI is becoming better at what it does, but it's also being utilized in different application areas.

Technologies like PCI Express Gen 5 enable related technologies like CXL, which are changing the ways that data centers are designed. Chiplets and glass substrates may make chiplet-based solutions more economical. We could talk about everything from microLEDs to augmented-reality/virtual-reality (AR/VR) technology, but this list keeps going on and on. It's what we report on a daily basis at *Electronic Design*.

Many of these technologies are covered in this special Innovators issue, which also addresses disruptive technologies like those mentioned above. On top of that, the issue includes a few profiles of innovators in the industry. It's a short list due to space limitations, so it touches on a very small fraction of innovators worth recognizing—especially given that much of the technological disruption is driven by technical innovators among a large array of companies.

The effects of COVID have not worn off and work-from-home along with a distributed workforce has had its good and bad effects. Disruptions due to global turmoil are worsening. This isn't just a supply-chain issue—it's an intellectual one as well. Developers, designers, testers, and support personnel may be located in countries affected by this turmoil. Like a critical chip in a design, these people can be just as critical to a product's success.

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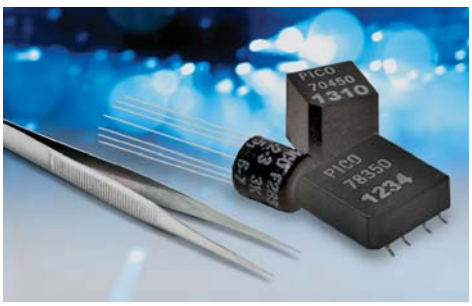

At Pico Electronics, we develop miniature and ultra-miniature units that meet the high quality, high reliability specifications of military, commercial and other critical applications.

When Pico Electronics was founded in 1967, transformers and converters were quite large, and not terribly efficient. Our mission was to change that. It wasn't long before we became ***the*** ultra-miniature inductor and transformer resource.

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MICHELLE KOPIER | Group Content Director

Innovators in Electronic Design

Now in its second year, the 2024 Innovators in Electronic Design issue features new faces of those who have been instrumental in the advancement, development, growth, and progress of the electronics industry. The following individuals have been recognized as key innovators in the market.

UP & COMER

Hellen Parpinel, Bluespec Inc.

Hellen has developed an integrated design environment that includes open-source RISC-V tools as well as Bluespec's and other commercials vendor's tools. *Bluespec Inc.*

WHEN HELLEN JOINED Bluespec Inc., she immediately made an impact by playing a lead role in multiple company initiatives that drive adoption and enable innovation with RISC-V.

After graduating with a BS in Computer Science with honors at the University of Washington in 2021, Hellen Parpinel joined Bluespec Inc. She made an immediate impact upon her arrival by playing a lead role in multiple company initiatives that drive adoption and enable innovation with RISC-V.

Hellen developed an integrated design environment that includes open-source RISC-V tools, as well as Bluespec's and other commercial vendor's tools.

Most recently, Hellen has been leading the company effort to standardize and automate the delivery of Bluespec's processor IP and RISC-V tools, making RISC-V more accessible and easy to use for the development community.

TRAILBLAZER

Martin Schneider, CTO, STARTEAM Global

WITH A FOCUS on the next 2-4 years, Martin is committed to substantially increasing production capabilities while also expanding STARTEAM GLOBAL's expertise to include high-layer PCBs, high-frequency PCBs, and HDI PCBs.

Martin Schneider, a precision mechanic, began his professional career in 1983 at Siemens in Karlsruhe, Germany.

Martin started his career in printed-circuit-board (PCB) manufacturing at Siemens in Karlsruhe, Germany in 1983. Due to the increasing demand for electronics within the Siemens Group, production was expanded and modernized.

Martin went through all production processes, got to know every area of production, and at the end of the 1980s began to significantly increase the production of internal layers and to produce high-layer PCBs.

In addition to his work as a production manager, Martin continued his education as a technical business economist. In the 1990s, Siemens introduced SIMOV technology to PCB production in Karlsruhe and invested heavily in state-of-the-art production facilities for HDI production.

Martin took over the entire area of inner-layer production and significantly contributed to the successful implementation of these technologies.

In the 1990s, the electronics industry began massively shifting the production of PCBs to Asia. As a result, it became increasingly difficult for production in Karlsruhe to remain competitive.

Siemens spun off PCB manufacturing in the late 1990s and sold it proportionately to Sanmina, resulting in a complete sale in the early 2000s.

Martin was appointed production manager of the Karlsruhe site and set himself the goal of driving productivity increases, cost reduction, and producing special technologies.

Martin Schneider, a precision mechanic, began his professional career in 1983 at Siemens in Karlsruhe, Germany. *STARTEAM GLOBAL*

In 2007, after over two decades at Siemens and Sanmina, Martin moved to CML, where he took over the Technology and Quality division.

In the early years, he spent most of his time in China, expanding the supplier portfolio, establishing effective supplier management, and building engineering and quality departments.

Martin focused on the introduction of automotive standards methods to improve quality and increase productivity. In 2016, Martin was offered the position of Sales Director, and in the following years he led the sales team. Together with his colleagues, he expanded the customer portfolio in Europe.

In 2018, STARTEAM GLOBAL, formerly CML, took over its first production plant in China and then gradually expanded its production capacity.

At that moment, STARTEAM GLOBAL needed Martin's production experience to align the newly acquired plant in Sichuan, China. Subsequently, he took over the global Technology division, and in the following years, he was able to contribute and implement his valuable experience in the production of PCBs.

Over the years, the company has successively expanded its production capacity and prepared for the introduction of further applications such as metal substrates, PCBs, and high-voltage applications.

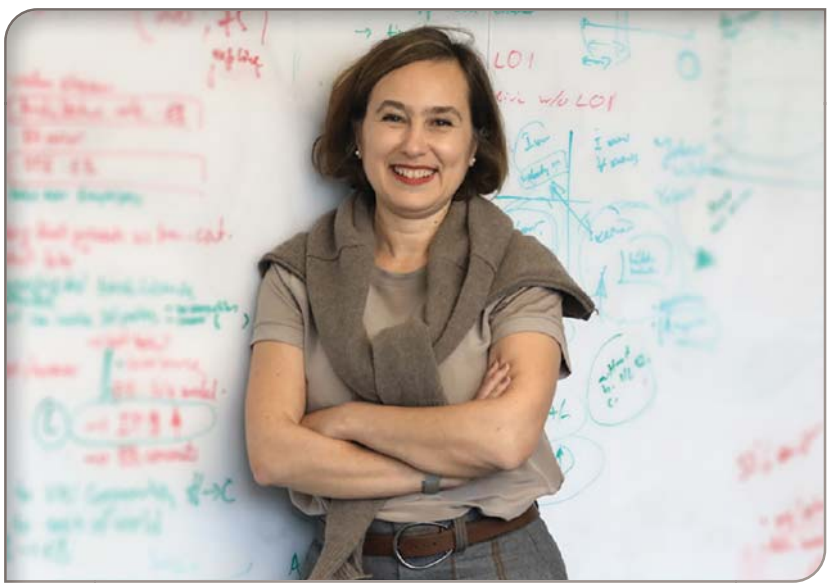
The engineers and technicians of his department intensified the cooperation with the development departments, thus helping STARTEAM GLOBAL's customers develop their new products much faster and more cost-effectively.

STARTEAM GLOBAL recently unveiled a new PCB manufacturing plant in the thriving industrial zone of Pranchinburi, Thailand on September 27, 2023. This additional facility complements the company's existing factory in China as part of its China+1 strategy.

With a focus on the next 2-4 years, Martin is committed to substantially increasing production capabilities in both factories while also expanding their expertise to include high-layer PCBs, high-frequency PCBs, and HDI PCBs, enriching the company's diverse array of offerings.

WOMEN IN SCIENCE & ENGINEERING

Maria Anhalt, CEO, Elektrobit



Maria Anhalt is CEO at Elektrobit, an award-winning and visionary global vendor of embedded and connected software products and services for the automotive industry. *Elektrobit*

UNDER THE LEADERSHIP OF MARIA ANHALT, Elektrobit has been collaborating closely with carmakers and technology partners to bring their visions for the cars of the future to life.

Maria Anhalt is CEO at Elektrobit, an award-winning and visionary global vendor of embedded and connected software products and services for the automotive industry. Maria leads an international team focused on providing carmakers with software that transforms mobility, drives sustainability, and enables a more interactive and intuitive driving experience. Maria Anhalt is one of the thought leaders behind the software-driven transformation of the automotive industry.

The future of vehicles is software-defined, and visionary carmakers are investing in partnerships and technologies that enable them to build the complex software systems necessary for their next-generation vehicles. To this end, Elektrobit has found a unique niche. Under the leadership of Maria Anhalt—who became CEO in 2021—Elektrobit has been collaborating closely with carmakers, both established and startups, as well as technology partners and suppliers to bring their visions for the cars of the future to life.

Following decades of leading software efforts at companies like HP, Maria brought software expertise that helped transform corporate data centers to the automotive industry just as it was entering an era of dramatic change. She started with a simple mantra that was foreign to automotive: "Software First."

Until recently, developing vehicles revolved around hardware components—think braking systems and powertrains—typically sourced by carmakers from suppliers as components. If software was needed, it was usually added after the fact. Today, the reverse is true. Software is redefining mobility…and doing so much quicker than the industry envisioned. To bring EVs and autonomous and connected vehicles to life, carmakers are on a challenging quest to build a common software platform for their lines of vehicles, and Maria and Elektrobit are leading the charge to support these efforts.

With this goal in mind, Maria pivoted the company to focus on collaborations to help carmakers fast-track their next-generation vehicles. One example is Elektrobit's partnership with Jaguar Land Rover (JLR). Elektrobit software and services is being used for the next-generation EVA Continuum electrical architecture that will be in JLR's full line of vehicles in 2024. Maria and Elektrobit believe that partnerships, collaboration, and open source are crucial to the foundation of the software-defined vehicle. To this end, she has been leading efforts in collaborative development including involvement in organizations like Eclipse SDV and COVESA.

Another example is Elektrobit's multi-year collaboration with Sony, providing software and integration services that enable the unique in-vehicle experience of the Sony Honda Mobility (SHM) AFEELA.

Under Maria's leadership, since 2021, Elektrobit has grown by approximately 25%, and a quarter of new hires have been women. Maria's accolades include the Automotive News 2022 All-Star Award for Software Innovation and Technology Innovators' Top 20 CEOs 2022 in Automotive Technology. She belongs to the Top 50 Women in the Automotive Industry.

For International Women's Day 2023, Maria was highlighted as a Top Female Leader in Tech by Amazon AWS.

In addition, Maria is one of the visionaries of "Women in Mobility"

2023 has been the "year of the software-defined vehicle," and Maria Anhalt is its most passionate evangelist.

TRAILBLAZER

Chuck Lewin, CEO, Performance Motion Devices

OVER THE YEARS, CHUCK LEWIN has worked closely with his team to deliver motion-control ICs and boards that tackle the unique requirements of today's machine designers.

Chuck Lewin is a pioneer in delivering high-performance motion control on an IC and installing that IC in a range of products so that they would speak one common motion language. Today, PMD delivers on that original vision with world-class motion-control ICs, drives, and boards, allowing machine designers to build systems faster, more reliably, and at a lower cost using this common motion-control IC approach.

Some might say that it began with a passion for software. Early in his career, while working as a software engineer for a manufacturer of semiconductor robotics, he repeatedly butted his head against National Semiconductor's LM628's limits. He concluded that there was an opportunity to develop a higher-end product, so in 1992 he started Performance Motion Devices (PMD). In less than a year, the first commercial multi-axis motion processor was released. This breakthrough product paired the advantages of IC packaging with sophisticated functions previously available only in board-level motion-control products.

The drive to innovate and develop breakthrough motion products led him to introduce the Magellan family of motion-control ICs in 2003. Magellan multi-axis ICs and boards provide position and velocity for brushless DC (BLDC), DC brush, and step motors. These flexible and powerful ICs provide profile generation, servo-loop closure, commutation, current control, and pulse and direction output along with direct quadrature encoder input.

Seeing the need for standalone modules, in 2006 he expanded the company's product offerings to include the ION Digital Drive. Driven by the Magellan IC, these compact, fully enclosed modules provide high-performance motion control, network connectivity, and power amplification. They became popular for medical, scientific, semiconductor, robotic, industrial, and other automation applications.

Over the years, Lewin has worked closely with his team to deliver motion-control ICs and boards that tackle the unique requirements of today's machine designers. Some of these new products include the Magellan MC58113 IC, which provides high-performance control with an integrated digital current loop, Atlas compact, solderable single-access modules for torque control, and the Juno family of ICs that provide advanced velocity and torque control.

The trailblazing continues… In 2021, PMD released one of the industry's smallest, most intelligent motion-control drives, the ION/CME N-Series Drive. N-Series IONs feature a patented, ultra-rugged, PCB-mountable package and provide high-performance motion control, network connectivity, and power amplification for BLDC, DC brush, and step motors.

What's more, like all PMD products, it's powered by a single-axis IC that speaks one common motion language.

With one simple idea, motion control on an IC, Chuck Lewin revolutionized how today's leading manufacturers of laboratory equipment, medical automation, and robotics deliver solutions that demand speed, precision, and power. *Performance Motion Devices*

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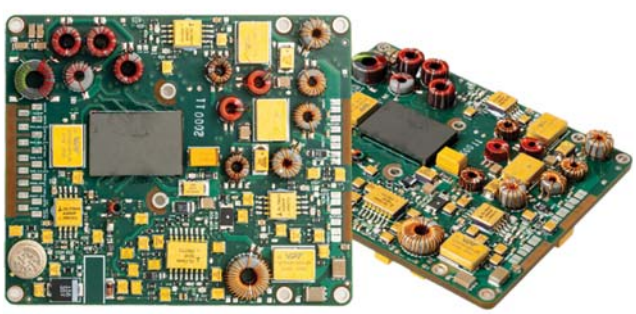

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DC-DC converters from 1 – 250 Watts, point-of-load converters from 3 – 20 Amps, EMI filters, transient suppressors, inrush current limiters, bus converters, and thermal pads. VPT's VXR Series for rugged military and commercial avionics applications is epoxy-encapsulated with dual-sided thermal conduction and features a wide input voltage range (9 to 60 Vdc). The patented V-SHELD® epoxy-encapsulated packaging is highly resistant to chemical, solvent, and salt environments. It is fully compatible with high-volume manufacturing processes, including wave solder, cleaning solvents, high-pressure sprays, and aqueous wash.

VPT also offers a range of DC-DC converters and accessories designed, tested, and proven for the challenging environments of space. Input voltages are available in 28V, 50V, 100V, and 120V, all with the latest revisions of MIL-PRF-38534 Class K. The SVR Series products feature maximum levels of radiation hardening with a Total Ionizing Dose (TID) of 100 krad(Si) and SEE of 85 MeV/mg/cm2. VPT's SVL Series products feature a TID of 60 krad(Si) and SEE 85 MeV/mg/cm2, with 28 and 50 input voltage options.

VPT's space line also includes the VSC Series of commercial-off-the-shelf (COTS) converters and EMI filters designed for "NewSpace" applications, smaller satellites in low Earth orbits (LEO), and NASA Class D missions. VPT is releasing the next product in this series, the VSC100-2800S, in the first quarter of 2024. Additionally, the GaN-based SGRB Series is radiation tolerant, achieves a high efficiency of up to 96%, and includes a fixed-frequency reduced voltage switching topology resulting in low input and output noise.

VPT recently introduced its first configurable quad-output power supply designed for RF space applications, the SLNP17-100CQ. Thanks to a multi-stage approach, the SLNP17 achieves an exceptional rejection of noise for both conducted emissions and conducted susceptibility. With 11 configurable options, this DC-DC converter was designed and built with customization top of mind. As a space-qualified product, the SLNP17 guarantees TID performance to 100 krad(Si) and SEE performance to 85 MeV/mg/cm2, which is ideal for GEO orbit missions.

Global customers of VPT include NASA, Lockheed Martin, Boeing, Raytheon, ESA, and Thales. VPT is part of the HEICO Electronic Technologies Group (NYSE: HELA) (NYSE: HEI).

More information can be found at ***www.vptpower.com***

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WILLIAM G. WONG | Senior Content Director

Dealing with **AI Disruption**

AI is already disrupting the product planning and development process—and it's only getting worse.

1. This is an AI-generated image based on a simple request: cute dark furry cat playing with a colorful Rubik's Cube on the ocean. *268115686 © Rufous | Dreamstime.com (AI generated)*

DO YOU LIKE the cute dark furry cat playing with a colorful Rubik's Cube on the ocean *(Fig. 1)*? I found it while searching for "AI Playing Cards" at Dreamstime.com, where we get a lot of our stock images. The search engine obviously missed the point of my query, but it was a cute AI-generated image.

Instead of chasing down more card-playing AI images, I tried the description above at Craiyon.com. One of the results was the image shown in *Figure 2*. Though not necessarily as playful, it's at least accurate to the description. Both are not too useful in general, unless you happen to be writing an article about generative artificial intelligence (AI) like I'm doing here.

I also tried out OpenAI's Dall-E 3 *(Fig. 3)*. Dozens of websites and tools like Dall-E and Craiyon out there use generative AI and lots of training material to create images on demand.

I think one thing that's captured everyone's interest in generative AI is the ability to utilize it directly with online tools like ChatGPT or github's Copilot rather than indirectly. Almost everyone who's on the internet is likely to have used generative AI in some form as it creeps into our search engines, website sales tools, etc.

One interesting aspect about these generated images is that they're free to use, although most require an annotation of where they were sourced. The other aspect is that right now those images can't be copyrighted; hence, anyone can copy them.

2. This AI-generated image was also based on a simple request: cute dark furry cat playing with a colorful Rubik's Cube on the ocean. *Craiyon.com (AI generated)*

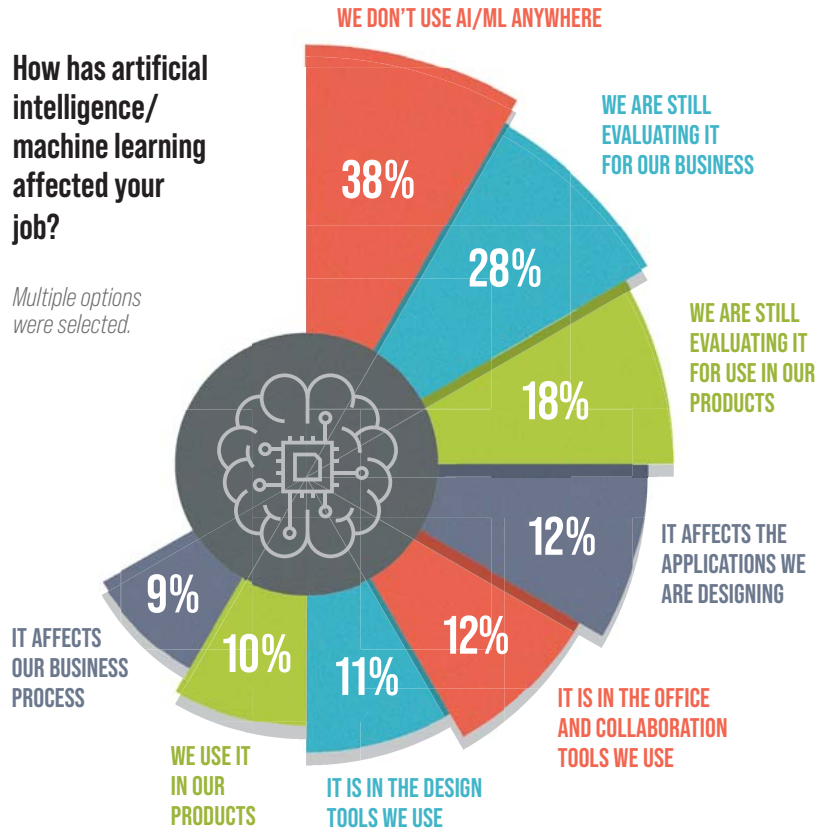
3. Here's another AI-generated image based on the same simple request: cute dark furry cat playing with a colorful Rubik's Cube on the ocean. *OpenAI Dall-E 3 (AI generated)*

Choosing a Disruptive AI Model

Generative AI covers a lot of ground, not just image creation. These tools tend to be based on large language models (LLMs) that use a tremendous amount of training material. While much of the input for using these models is text-based, it's not a requirement. The inputs and outputs and training data can take almost any form, from sensor data to audio and video streams. One almost needs AI tools to discover the AI tools to incorporate in a product or service that utilizes AI or optimizes the product or service using AI models and techniques.

According to our recent Salary Survey results *(Fig. 4)*, AI and machine-learning (ML) tools are only being employed by a small fraction—but it's growing. While using tools like Dall-E and Midjourney might be easy for anyone, their incorporation into products such as self-driving cars or smartwatches is much more challenging and prone to issues that a self-described AI artist doesn't have to contend with, e.g., reliability and liability.

Developers must keep one factor in mind: Unlike digital logic, which has a 0 or 1 output, the output from almost any AI model—not just generative AI tools—is full of potentially unknown variations, and results aren't necessarily optimum or even valid all the time.



4. One of our Salary Survey questions addressed AI/ML use. It looks like the jury is still out for many companies. *Electronic Design*

In some sense, there's the garbage-in-garbage-out issue. However, it now applies not only to the data coming in and out, but also to the model that's chosen as well as the training material involved. Though the model and training data may be static, these days the trend is also toward dynamic updates based on new input. This can be a challenge when dealing with stability and reliability issues.

Where is AI Headed?

LLMs are relative. Most are hosted in the cloud or large servers to handle lots of requests, and simply because of the compute requirements. Using the same techniques on the edge is possible—a trend that's growing. This isn't being done on conventional processors, but rather on those platforms equipped with hardware AI acceleration.

These days, the challenge is that acceleration hardware is often tuned to particular AI models such as convolutional neural network (CNN) inferencing. This means not all platforms will support all models. Then again, not all applications need to utilize LLMs. Still, AI in some form tends to be more in the mix these days.

Online AI assistants might be the rage and direction of cloud-based services, but it would still be challenging as a standalone edge application. Nonetheless, improved user interface support, including voice activation, is doable today and getting better over time. Touch interfaces have improved, too, and are ubiquitous in embedded applications. Voice and video interfaces are likely to follow a similar path as AI support ramps up and matching hardware support makes low-power operation feasible.

In many ways, AI is like hardware security support. Dedicated hardware security support was almost nonexistent many, many years ago, but advances like TPM and secure elements cropped up. Currently, not one new, single application processor that I know isn't equipped with its own dedicated security processor, secure boot, and hardware encryption acceleration.

AI is Everywhere...Almost

AI acceleration isn't as ubiquitous yet, but it's close. Every major processing chip has AI acceleration of some sort and every flagship microcontroller does as well. By the way, they all feature security enhancements.

The challenge with AI is that unlike security systems incorporating standards with known algorithms and implementations, the AI support can be either too general or too specific with tradeoffs in performance, functionality, and power. AI support for CNNs and LLMs is similar but not necessarily the same, and the large amounts of hardware required means that using it optimally will be key in terms of performance and power utilization.

Chip and tool vendors were finally getting conventional neural-network support into their hardware and tools, and then along came generative AI. Expect to see more support targeting LLMs in the embedded space. It's also likely that we'll see significant optimizations along the way, often in software, that will benefit existing hardware platforms. This has been true for existing AI models and platforms, where improvements have sometimes been an order of magnitude over time.

It's always important to remember that AI isn't a solution alone, and not all platforms or services will need or benefit from AI support. Developers should not overlook basics like state machines or rule-based systems just because AI hardware is available or because of the overall "cachet" of AI. An FFT is still better at what it does, but don't overlook new alternatives.

I've seen AI models that have replaced 3D object detection and range determination with a single video camera. Often finding a model, training it, and incorporating it into an application is the easy part. The hard part is determining whether AI is a viable option, what approach to take, and what models may be applicable to the problem. ed

JIM HANDY | Objective Analysis

7 Technologies That Will Change Everything

Jim Handy's crystal ball reveals trends about many topics, ranging from memory chips to generative AI.

MANY YEARS AGO, when I moved to Silicon Valley, technology was undergoing massive change and was poised to make massive inroads, changing our lives as we know it. Although nobody expected this startling progress to last forever, the excitement continues, with newer technologies still expected to make massive inroads, changing our lives as we know it.

Let's look at some of the current technologies that are likely to create significant change over the near term:

Generative AI

Probably the darling of the industry, this new approach to the use of artificial intelligence (AI) doesn't limit itself to recognition and learning. It goes the additional step of reviewing phenomenal volumes of data to create reports, designs, and manipulated images faster than any human being.

What will be its impact on chip demand? Well, it takes such a huge amount of data that few organizations can afford the hardware or even the electricity to run it, so it's fallen into the domain of the internet data center, where numerous users can access it over a 24-hour day.

Generative AI is likely to be embodied by a pretty small number of colossal computing machines that, put together, will account for a very small share of chip consumption. Even so, its use should change our lives.

Electric Mobility

It seems like everyone here in Silicon Valley (and probably in most other urban areas) is moving around electrically on eBikes, electric scooters, electric and hybrid cars, electric skateboards, unicycles, and Segways.

All of them require power conditioning and batteries. Some require fancy balancing controllers, and the autos include driver assistance. This is fertile ground for designers and electronics suppliers as a growing share of the world's transportation budget will be devoted to electronics over time while this exciting field blooms and matures.

MRAM, ReRAM, Other?

Whether it's because of tightening process geometries or concerns about power, existing memory technologies are already seeing emerging memories nibble away at their markets. MRAM and ReRAM have seen rapid adoption for embedded program and data memories in wearables and IoT endpoints. Their use will grow over time to create a $44 billion market by 2032, according to a report recently published by Objective Analysis and Coughlin Associates *(Fig. 1)*.

As their application broadens, unit volumes will rise, allowing the economies of scale to drive down their prices. Today, these and other emerging memories compete against NOR flash and SRAM. But as their price continues to decline, they will encroach upon DRAM and NAND flash, eventually replacing them altogether. Expect big changes in both the kind of memories used and in the applications that they enable, as their technical advantages led to the development of new usage models.

CXL

DDR DRAM has nearly run its course, migrating over the past two decades from DDR1 through DDR5. A new approach will arrive to support the voracious data

needs of high-end processors, and CXL is poised to take on that role *(Fig. 2)*.

Although CXL today appears to require no more than a sophisticated controller and standard DRAM, expect the sophistication of the controller to increase even as its price shrinks. This will have a major impact on systems design, first in hyperscale data centers, but eventually migrating down to all levels of computing, including PCs and cell phones.

Chiplets & UCIe

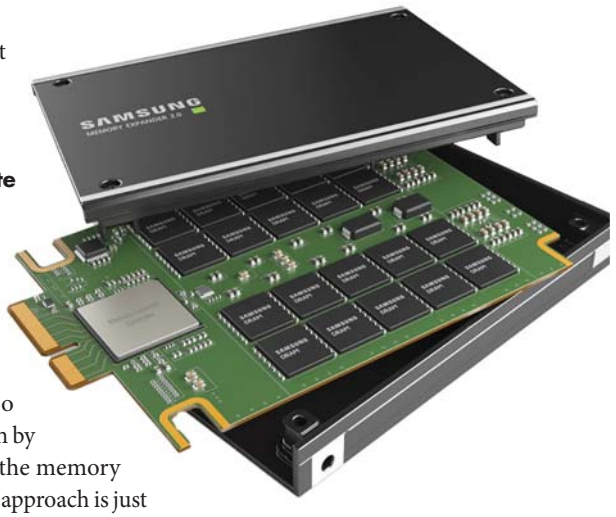
The limitations of modern photolithography equipment have stopped die sizes from growing, which was one of the three components Gordon Moore identified in 1975 that drove Moore's Law forward. Chip designers are just now moving to chiplets to keep Moore's Law on track.

So far, the communication between these chiplets has been proprietary, but UCIe (the Universal Chiplet Interface) is destined to change that. This will drive important costs out of the chiplet approach to broaden its use. Today, chiplets are found in high-end processors, but eventually, UCIe will be used to cost-reduce chiplets so that they will find homes even in modest SoCs.

In-Memory Compute

For decades, computer designers have hungrily looked at the kilobit-wide data paths within memory chips and dreamed of ways to harness that bandwidth by adding processors to the memory chips themselves. This approach is just now beginning to gain a reputable following through experiments like Samsung's Aquabolt XL. Many others are working on similar efforts, but expect it to take some time for this technique to catch on.

Two factors are poised to stall it: One is that it requires software changes, and those conversions are always implemented extremely slowly, even if they aren't that hard to develop. Nobody wants to take the chance of introducing new bugs into time-proven code. The other factor is that it drives up the cost of a memory chip, and system developers greatly dislike costly memory. Still, exciting change is in the air!



2. Samsung's 512-GB CXL DRAM provides low-latency storage for CXL-based systems. *Samsung*

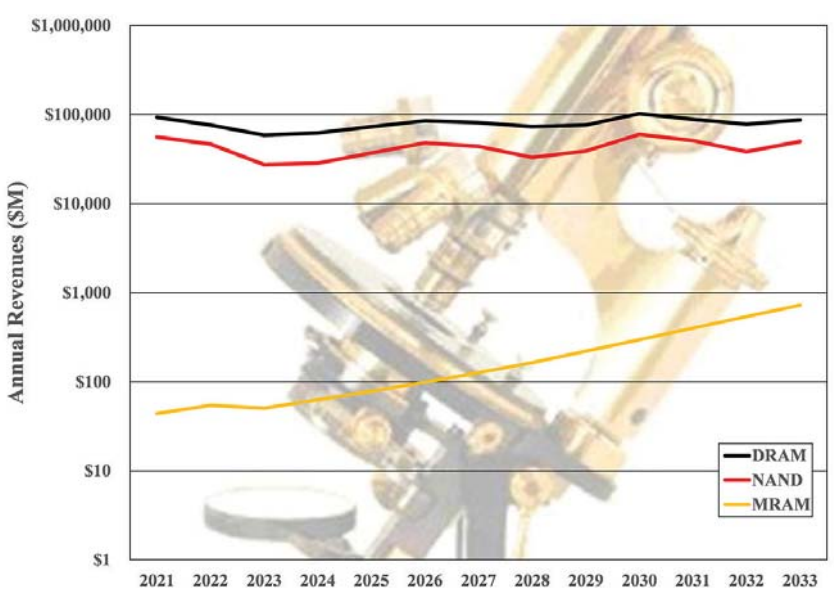
Computational Storage

Computational storage is very similar to in-memory compute, since it adds smarts within the storage device (SSD) or storage array. This approach isn't driven by the huge bandwidth advantage that drives in-memory compute, but it's instead aimed at reducing I/O traffic between the server and storage device.

While today's advocates see computational storage as a programmable device that can offload varying tasks from a server, my guess is that we will see SSD-based smarts used mainly in fixed-function devices like those now provided by IBM, which compress data and perform primitives to help detect ransomware before it's used in an attack.

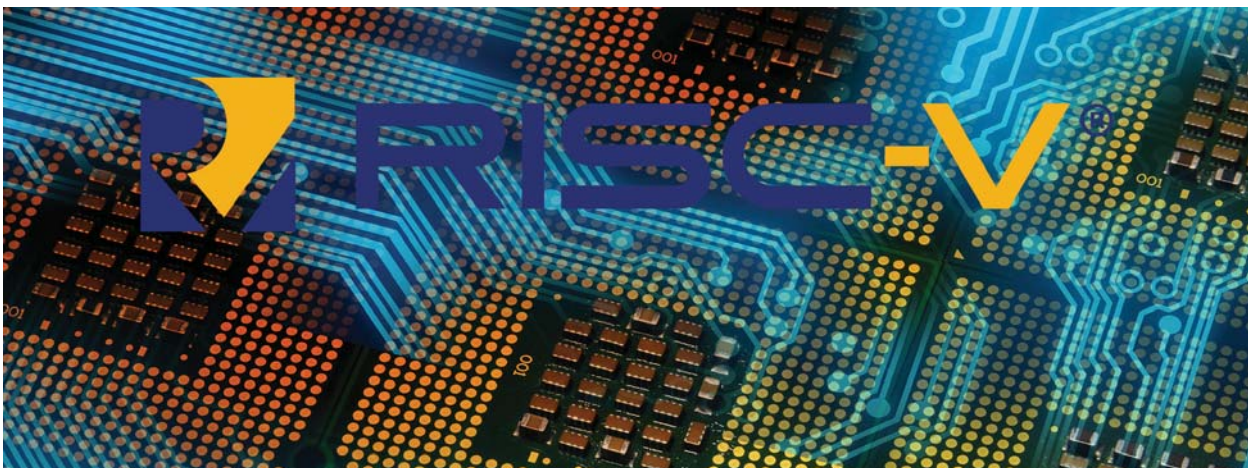
Exciting Times

I'm sure that readers will note several other new technologies I've overlooked, and that's a good thing, since it means the excitement in this field will continue for a long time to come. ED



1. Emerging memory revenue is forecast to grow significantly faster than DRAM or NAND flash. *Objective Analysis*

JACK KANG | Senior Vice President of Customer Experience, SiFive



The Rise of RISC-V: From University Lab to Global Force in Silicon Design

How did RISC-V transform from a student project into an architecture that's being used by organizations, universities, and governments around the world? Let's dive into the history of RISC-V to find out.

RISC-V ORIGINATED IN academia as a summer project and later turned into a global phenomenon driving a new era of innovation in the semiconductor industry. Today, RISC-V is in more than 10 billion cores on the market, and it's being used in a wide variety of applications from aerospace to automotive, data centers, the IoT, and beyond. So how did RISC-V transform from a student project into an architecture that's being used by organizations, universities, and governments on a global scale?

RISC-V's Roots

RISC-V was dreamed up in May 2010 at UC Berkeley's Parallel Computing Laboratory (Par Lab). Professor Krste Asanović and graduate students Yunsup Lee and Andrew Waterman were looking for a processor core they could use for a summer research project. They considered using either x86 or the Arm instruction set architecture (ISA). However, the team quickly realized that even if they could negotiate a commercial agreement, they would not be able to customize the core—and, more importantly, they would be unable to share the results with other researchers.

Since there wasn't a viable ISA on the market that met their needs, they decided to develop their own. By August 2010, the team came up with a new ISA that they called RISC-V, representing the fifth generation of reduced instruction set computer (RISC) designs.

The team continued to work on the architecture over the next year. They were joined by Dave Patterson, director of the Par Lab and one of the pioneers of early RISC designs. Patterson is also credited for having coined the term RISC, and he co-authored the book "RISC in Computer Architecture: A Quantitative Approach," which is known as the standard text for processor design.

In May 2011, the team published the initial version of the RISC-V Instruction Set Manual and taped out the first hardware implementation of RISC-V on a 28-nm fully depleted silicon-on-insulator (FD-SOI).

The Forming of SiFive and RISC-V International

Over the next few years, the word about RISC-V spread and the creators realized that it held significant commercial potential. In fact, they later founded the RISC-V company SiFive. The creators held the first RISC-V Workshop in January 2015 to gather together developers interested in RISC-V.

Later that year, they launched the nonprofit RISC-V Foundation (now called RISC-V International) to manage, guide, and promote RISC-V around the world. RISC-V International now acts as a standards body that continues to oversee the RISC-V standard with its collaborative group of technical, industry, domain, and special interest groups.

Why Opt for RISC-V?

Several aspects of RISC-V make the ISA stand out and have contributed to its impressive growth. As an open standard, anyone can use RISC-V for commercial, research, or individual use cases without proprietary restrictions or limitations. However, companies can still invest, develop, deploy, or license proprietary implementations for commercial purposes.

Since RISC-V was created with a clean slate design, it offers more flexibility, extensibility, and scalability than the closed architectures in the market that have decades of baggage. This has led to superior power, performance, and area implementations.

Companies also have the option of adding application-specific extensions designed for specific workloads, which is especially important for cutting-edge applications like AI and ML *(Fig. 1)*. As a result, RISC-V is making custom silicon available to companies of all sizes.

RISC-V's design freedom has spurred the rise of a new generation of startups, including SiFive, which was founded in 2015. Asanović, Lee, and Waterman saw a growing need for high-quality, world-class RISC-V solutions in the commercial market, so they started SiFive to meet that demand.

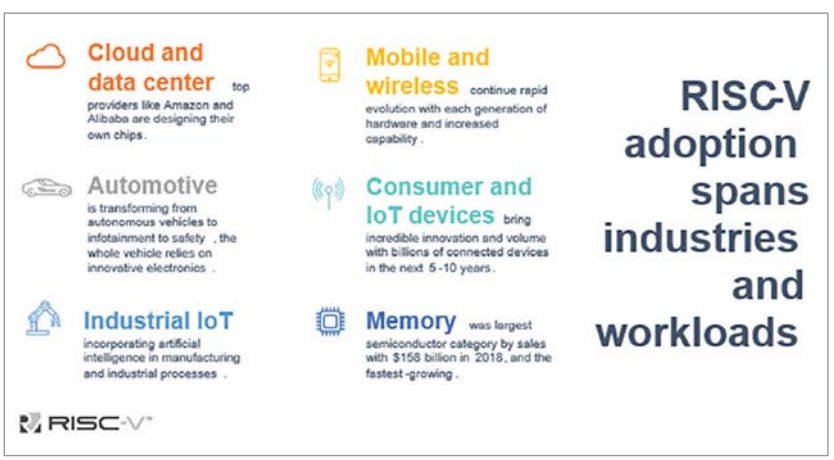
Today, SiFive is valued at more than $2.5 billion and the company has secured more than 300 design wins from over 100 customers with its high-performance RISC-V IP. In 2010, it would have been hard for the founders of RISC-V to imagine that one day the technology they developed would be adopted by NASA for future space missions on Mars.

An Open Ecosystem

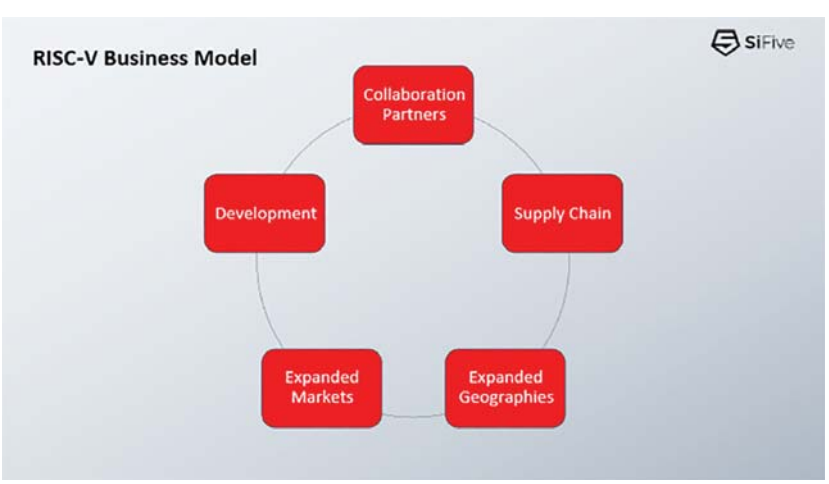
RISC-V International now has more than 3,800 members across 70 countries. The organization is made up of corporations (including some of the biggest tech companies), universities and research institutions, non-profit organizations, and individuals. The spirit of collaboration is what continues to drive the RISC-V ecosystem forward. Instead of everyone having to reinvent the wheel, they can build on the efforts of other developers and focus on innovation and differentiation *(Fig. 2)*.

As an open standard, RISC-V is also unconstrained by borders. Anyone from anywhere can learn, create, and design with RISC-V. That's why countries like India and China, along with the European Union, are all embracing RISC-V. At the recent RISC-V Summit Europe, Luis-Carlos Busquets-Perez, Administrator at the EU Commission, explained that RISC-V has "a very important economic impact in the European economy."

While RISC-V had humble beginnings, it's seen significant adoption and is reshaping the silicon industry as we know it. Industry giants and startups alike are using RISC-V to innovate, which has increased competition in the industry for the benefit of everyone. It's become clear that the future of RISC-V has no limits.



1. This infographic shows use cases, industries, and workloads that impact RISC-V adoption. *RISC-V International*



2. A visual representation of the RISC-V business model and key focuses. *SiFive*

GIJS WILLEMSE | Senior Director of Product Management, Rambus Security

Securing Data in the Quantum Era

The quantum-computing market size is expected to grow 11X by 2030. So, how do we safeguard our equipment and data now from these post-quantum era threats?

QUANTUM COMPUTERS ARE moving closer to tackling challenges where traditional computers fall short. In 2021, the quantum computing market size was valued at around U.S.$457.9 million and is expected to reach around $5.3 billion by 2030, according to Zion Market Research.

With the potential to perform faster calculations, work on multiple computations simultaneously, and utilize interconnected quantum bits (entangled qubits), the rise of accessible quantum computing will be advantageous across industries—from finance and banking to healthcare to transportation. From an artificial intelligence/machine learning (AI/ML) perspective, quantum computers will have the ability to solve optimization problems, analyze large datasets, simulate quantum systems for AI use cases, and so much more.

However, with new technological milestones come new threats that the industry must learn to combat. Quantum computers are no different. As companies race to reach the quantum finish line, serious security implications come into focus. It's time to start considering what the future of security may look like with quantum computers in the picture and determine how to advance cryptography standards accordingly.

A Leap Forward for Computing, a Step Back for Security

Governments, researchers, and tech leaders around the globe have warned that quantum computers will eventually be able to break the asymmetric encryption used today, putting critical communication and data protected with existing hardware and software at risk.

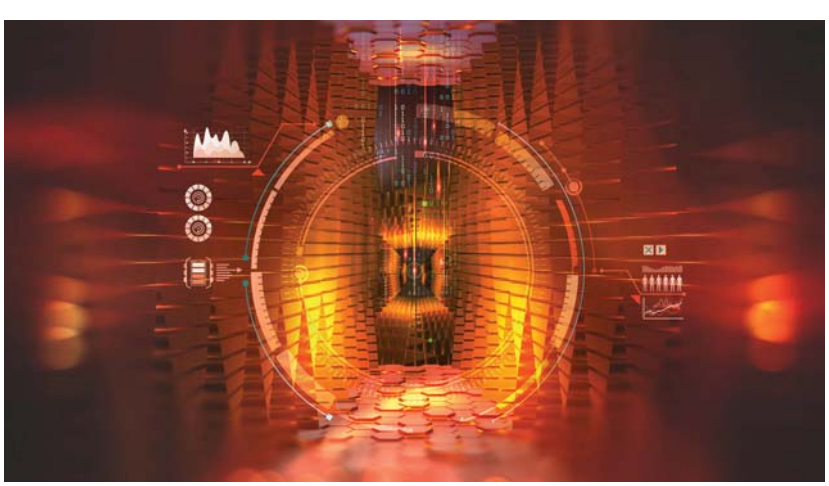
While quantum computers are still in the development stages, the U.S. National Institute of Standards and Technology (NIST) noted in January this year that by 2029, there's a one in five chance some fundamental public key cryptography will be broken.

Some of the most widely adopted security algorithms, such as elliptic-curve cryptography (ECC) and Rivest-Shamir-Adleman (RSA), used to safeguard sensitive electronic data like bank account information and medical records can be compromised in the quantum era. All modern security protocols, including TLS, IPsec, MACsec, and DTLS, rely on ECC and RSA for their key exchanges and are therefore at risk.

Classic asymmetric cryptographic methods for key exchange and digital signatures will quickly become vulnerable once powerful-enough quantum computers exist. This is because quantum computers leveraging appropriate algorithms, like Shor's, could accelerate the extraction of the corresponding private key from a publicly accessible key. Thus, any data encrypted using the public key can be decrypted without authorization.

AI/ML often deals with sensitive data, including personal information, confidential business assets, financial transactions, and more. If an adversary were able to break the key encryption used in an AI/ML system, not only would they gain unauthorized access to sensitive data, but they could manipulate ML models or impersonate authorized users.

Quantum computers leverage Shor's algorithm, reducing the security of integer discrete logarithms, including ECC and RSA. This makes it so no reasonable key size would effectively secure data. General symmetric cryptography, as well as Advanced Encryption Standard



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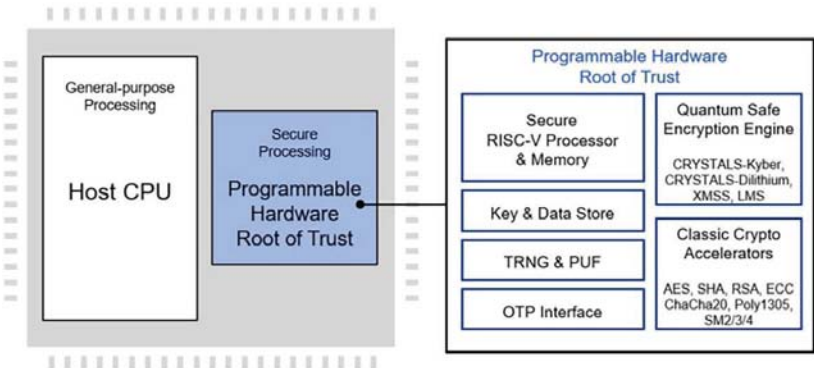

Shown is a representation of programmable hardware root of trust. *Rambus*

(AES), Secure Hash Algorithm 2 (SHA-2), and SHA-3, will likely experience a relatively smaller security decrease due to quantum computers.

To reap the full benefits of quantum computers and avoid consequences when they do hit the market, security solutions must be developed and implemented simultaneously.

The Quantum Secure Transition

Numerous efforts have been initiated to create and implement novel cryptography algorithms able to replace RSA and ECC while evading both classical and quantum attacks. This is known as "post-quantum cryptography" (PQC).

NIST has been central to developing and standardizing PQC algorithms in the U.S. In July of 2022, they announced the first group of algorithms designed to defend against a quantum attack. CRYSTALS-Kyber was chosen as a Key Encapsulation Mechanism (KEM) and CRYSTALS-Dilithium, FALCON, and SPHINCS+ as digital signature algorithms. The NIST post-quantum cryptographic standard is expected to be finalized over the next few years, integrating the four encryption standards selected.

Soon after the algorithm selection, the U.S. National Security Agency (NSA) released "CNSA 2.0," an update to its Commercial National Security Algorithm Suite (CNSA) mandating the utilization of CRYSTALS-Kyber and CRYSTALS-Dilithium as quantum-resistant algorithms. For firmware protection, NIST and NSA recommend stateful hash-based algorithms such as eXtended Merkle Signature Scheme (XMSS) or Leighton-Micali Signatures (LMS).

These updates provide a recommended timeline for the U.S. government and related suppliers to adopt these new PQC algorithms before data is vulnerable to quantum attacks.

Given the speed at which modern encryption standards may become obsolete, the NSA requires all National Security Systems (NSS) to transition to PQC software and firmware signing now, prefer its use by 2025, and complete this transition by 2030. Networking equipment should support and prefer CNSA 2.0 by 2026, and exclusively use CNSA 2.0 by 2030. A full transition to PQC algorithms by legacy equipment should be completed by 2033.

What to Expect Next

Transitioning from classical to quantum computers is a global endeavor, with organizations around the world laying out their own PQC recommendations as well. Europe's guidelines, for example, are closely aligned with NIST's, but Frodo KEM and Classic McEliece KEM algorithms are also accepted.

While a timeline for the standardization of more algorithms has yet to be solidified, it's plausible that soon, international organizations like the Internet Research Task Force's (IRTF) Crypto Forum Research Group, the Internet Engineering Task Force (IETF), and the International Organization for Standardization/International Electrotechnical Commission (ISO/IEC) will begin to approve additional algorithms. And they will integrate these into the RFCs and specifications for the secure communication protocols, such as TLS, IPsec, MACsec, etc.

Chip manufacturers have already started preparing for the "Quantum Secure Transition," expanding security IP offerings with Quantum Safe cryptographic solutions for future-proof data center and communications security. One way these organizations are taking strides toward quantum security is with next-gen hardware solutions that use NIST and CNSA quantum-resistant algorithms to secure hardware and data. These can include standalone acceleration hardware, or more advanced root-of-trust technology *(see figure)*.

With these offerings, applications requiring the highest level of security, such as data centers, AI, and ML, will be able to transition away from traditional cryptography for encryption and begin preparing to fight quantum attacks of the future.

Conclusion

Quantum computing has long been a concept of science fiction, often depicted in pop culture and entertainment as a futuristic development changing the world as we know it. But as it gains momentum across industry, government, and academia, it won't be long before we transition from the testing stages to deployment.

While the industry works to safeguard data from quantum threats with PQC, it's up to enterprises to inventory systems for applications that use public-key cryptography and create a game plan for transitioning to new cryptography standards before future quantum threats become vital. ed

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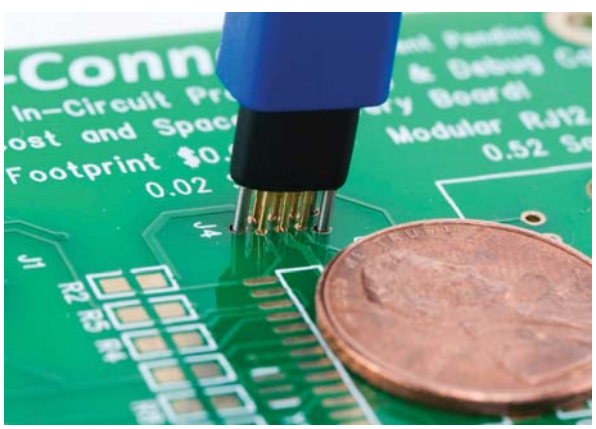

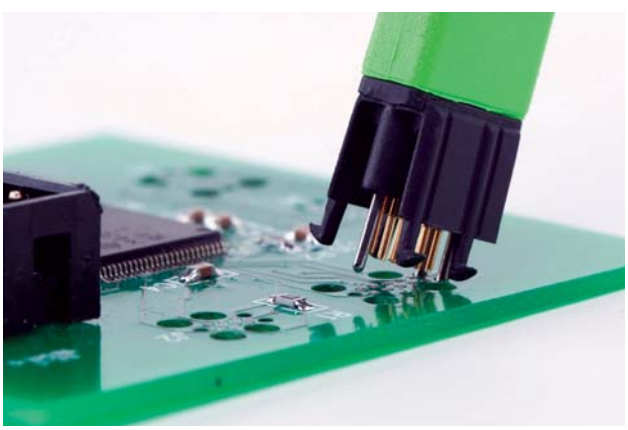

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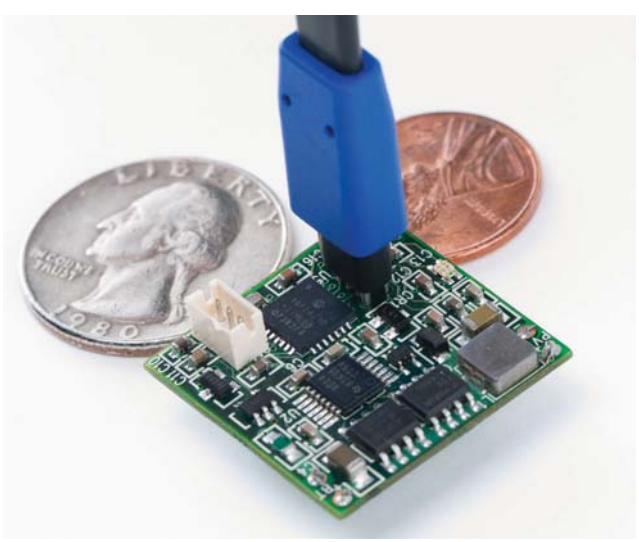

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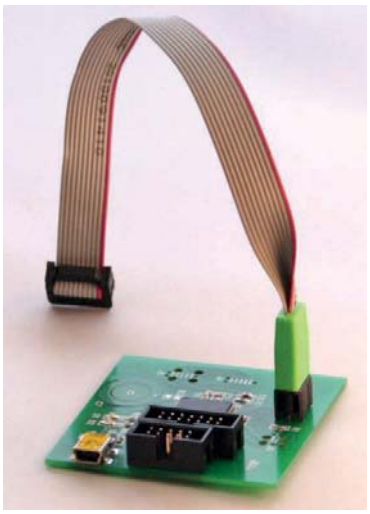

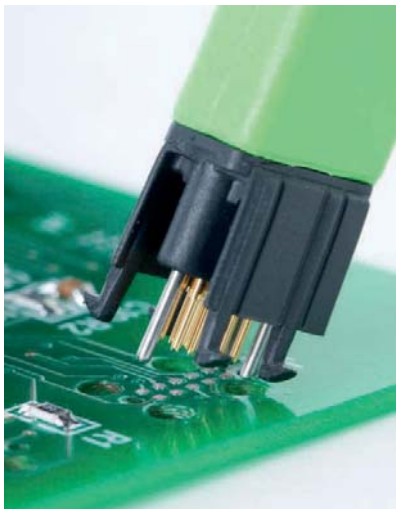

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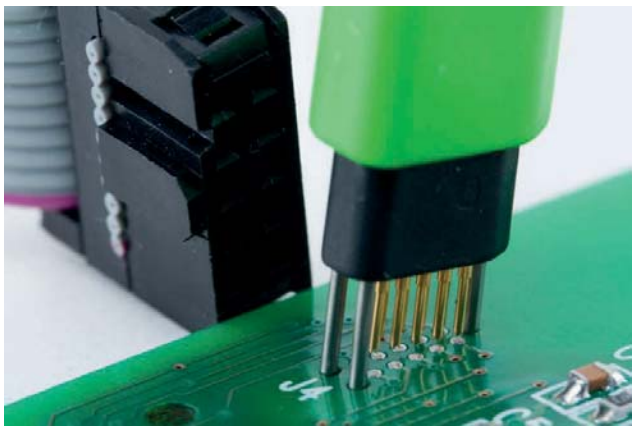

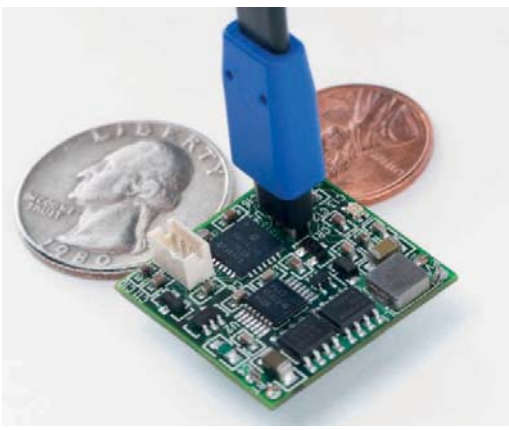

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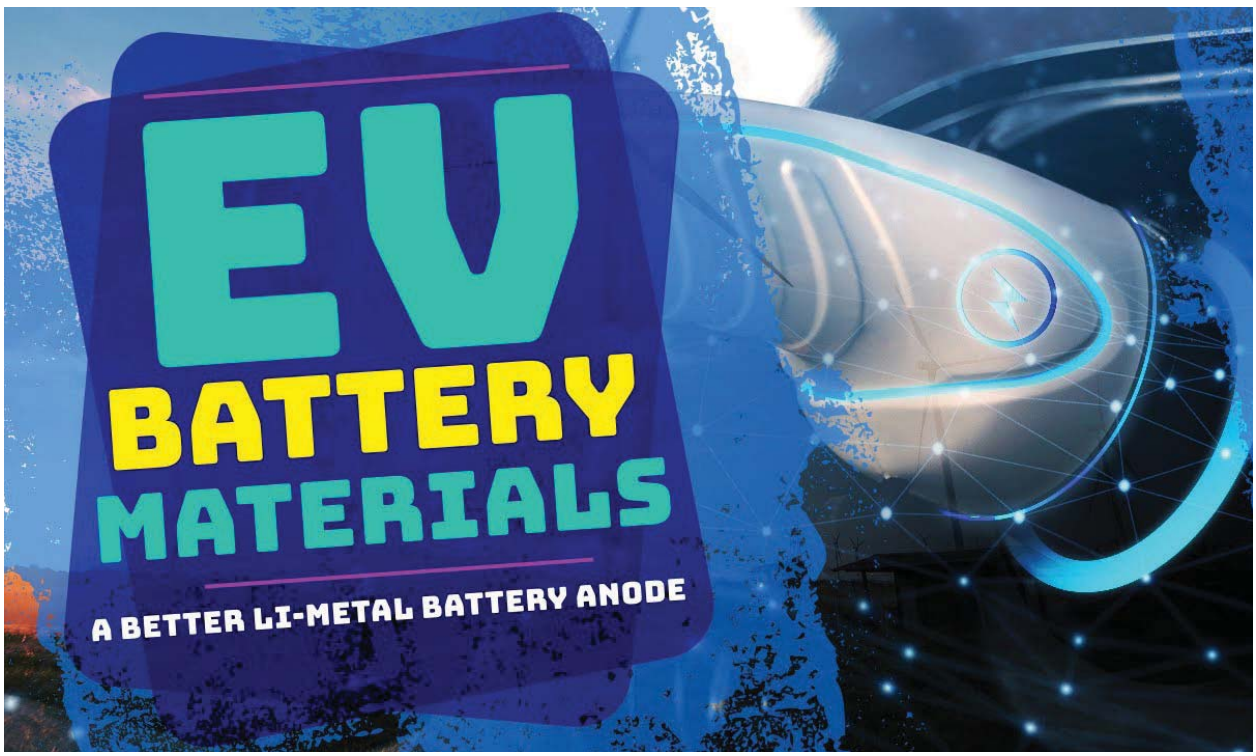


What's Next for EV Battery Evolution?

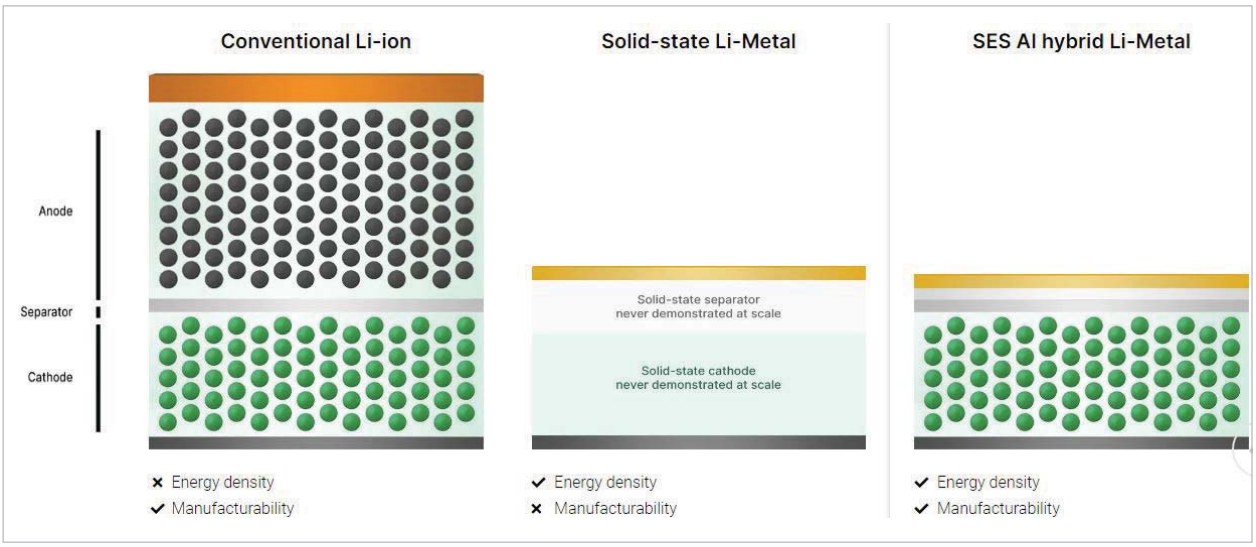
What's kept Li-metal batteries from fulfilling their potential to be a viable intermediate technology between today's Li-ion cells and the solid-state batteries expected to eventually power most EVs? The CFO of a leading battery technology company reveals some interesting answers.

RAPID ADVANCES IN battery technology have become the most significant factor in determining the future of electric vehicles (EVs). The lower costs, higher power densities, and reduced reliance on strategically sensitive materials are helping automakers make significant improvements in the price, performance, and practicality of each succeeding generation of EVs.

Electronic Design had the opportunity to gain some deeper insights into the technology and economics of the ongoing battery revolution during a recent interview with Jing Nealis, CFO of SES AI, a global developer and manufacturer of high-performance Li-metal batteries.

During our conversation, Nealis shared a bit about SES's technologies and how they serve the company's mission to help manufacturers produce better-performing, more affordable EVs, electric aircraft, and other forms of electric transportation. To accomplish this, SES uses a hybrid Li-metal architecture *(Fig. 1)* that incorporates several key technologies:

- A proprietary high-concentration solvent-in-salt electrolyte that fundamentally changes the way lithium dendrites grow, which reduces their rate of propagation.
- A protective coating that further stabilizes the interface between the electrolyte and Li-metal anode.
- A composite Li-metal anode that has a fundamentally different lithium dendrite formation mechanism, which almost eliminates the ability to degrade battery cells



1. SES AI claims that its hybrid Li-metal battery architecture overcomes most of the challenges earlier Li-metal approaches suffered from, enabling it to enter commercial production in the (relatively) near future. *SES AI*

Designed primarily for use in pouch-type cells, the new battery architecture enables existing manufacturing plants to be quickly upgraded to produce cells with 20% to 30% higher energy density at little or no added cost per unit. Slated to enter production in 2024, the company's large-format 100-Ah cells are expected to deliver >400 Wh/kg and 1,000 Wh/L while charging more rapidly and delivering a large number of charge/discharge cycles.

Some of the initial markets for the cells are anticipated to be eVTOLs and other electric aircraft, but joint development agreements with three of the world's largest automotive companies (General Motors, Honda, and Hyundai) clearly point to their widespread adoption in EVs. The higher power densities afforded by the new cells could change both the economics and the shape of the EV market.

Until now, the relatively lower densities of earlier batteries have forced manufacturers to either produce compact cars with relatively limited range or SUV-sized vehicles with beefy structures capable of accommodating a much larger battery pack.

Smaller, lighter, more powerful batteries, such as those made possible by SES, will enable manufacturers to produce a wider variety of vehicle types at more affordable costs. For example, the sleek concept cars recently announced by Mercedes and BMW *(Fig. 2)* are said to be fairly accurate previews of the production vehicles expected to offer ranges in excess of 450 miles. Such range is made possible by next-generation, high-capacity batteries that could enter the market as early as 2025. ed

2. Mercedes-Benz and several other leading automakers are using the higher power densities and lighter weights anticipated for next-generation batteries to develop sleeker, more affordable EVs that deliver much greater range. *Mercedes-Benz*

JAMES MORRA | Senior Editor

Can Silicon Supply Enough Power for the **Future of AI Silicon?**

Are traditional power electronics able to satisfy the rising power demands of AI chips in data centers?

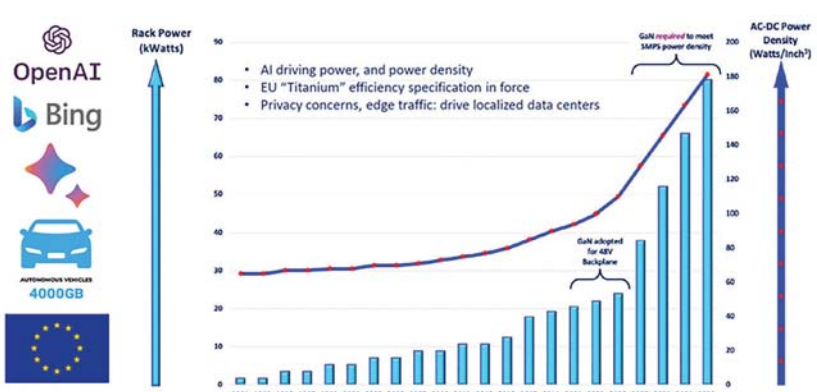
AS AI CHIPS grow larger to handle the rapid development and deployment of large language models (LLMs) such as OpenAI's ChatGPT, the amount of power that they require is rapidly ramping up, too.

New power-hungry AI accelerators such as NVIDIA's H100 GPUs have a thermal design power (TDP) of 700 W, while the most advanced CPUs and purpose-built AI chips are close behind. This is driving power-per-rack specifications up to 90 kW, which conflicts with what most data centers can manage at 15 to 30 kW per rack. As rack power demands for data centers rise by up to 3X, delivering more power in a smaller space is vital.

What must change to deliver power safely and reliably to these densely packed server racks? What about limiting and removing the heat generated in the process? For Stephen Oliver, VP of marketing and sales at Navitas Semiconductor, the solution starts in the power electronics. He contends that the silicon MOSFETs widely used today to convert and regulate the power entering each rack are reaching the end of their rope.

For its part, Navitas rolled out a new generation of gallium-nitride (GaN)-based power ICs, called GaNSafe, that "break through the glass ceiling" into high power levels reaching 22 kW in data centers, solar, and other renewable-energy storage, and even electric-vehicle (EV) subsystems. It's placing everything possible into a single GaN power IC, including control, gate-drive, sensing, and protection features that lend themselves to the harsh realities of these applications.

While silicon still dominates, many of the movers and shakers in the world of power semiconductors, such as Infineon and TI, are also pushing for power switching devices based on GaN as an alternative. GaN is the gold standard for consumer fast chargers and power adapters, but the challenge is proving that it can handle even higher power levels (thousands of watts at a time) as safely and robustly as silicon MOSFETs, said Oliver.



As industry leaders devote more of their data centers to AI workloads, power demands are rising fast. *Images courtesy Navitas Semiconductor*

He added, "GaN is relatively new technology, so expanding into these high-reliability areas has taken time."

Power Supplies: Translating Electricity from the Grid

Once electricity enters a data center from the power grid, it travels through several different checkpoints, where it's converted, regulated, and conditioned as it gets closer to the processors in servers. These chips require stable, clean DC power at very precise voltages. If the voltage is insufficient, the chip will fail to switch correctly. Overloading the chip with too much voltage can cause permanent damage to its delicate circuitry.

As power traverses a series of transformers when entering the data center, one of the core building blocks it encounters before hitting the processor is a switch-mode power supply (SMPS). Housed in a "silver box," its job is to step down the high-voltage electricity entering the rack—typically 220 V AC—to a lesser DC voltage that can be successfully used by the circuit board housing AI silicon. For a long time, 12 V was the standard DC voltage output by a power supply, but technology giants are currently raising their standards to 48 V.

The key to minimizing power loss is to deliver power at higher voltages and lesser currents and then step down the voltage as close as possible to server processors. Since Ohm's Law states that power is equal to the current times the voltage ($P = I \times V$), upgrading the power delivery to 48 V up from 12 V means 4X less current is required. Thus, power losses will be 16X less in the end. Elevating the voltage also makes it possible to use thinner, lighter copper wiring to ferry power through the system, saving on cost.

Even so, server power supplies are becoming more of a challenge to run

effectively as the demands for data-center rack power continue to rise, said Oliver. While the silicon MOSFETs that have long dominated power electronics are constantly improving, they fall short when it concerns AI chip power delivery. He noted, "You are throwing money at the problem by using more—and larger—silicon transistors than you need."

Given the challenges of supplying power to AI accelerators, Oliver said it finally makes sense to swap silicon out for GaN FETs. Using the unique material properties of GaN, these chips reduce gate charge (Q_g), output capacitance (C_{OSS}), and reverse-recovery loss (Q_{RR}) and limit power losses at faster switching frequencies. So, while they are more expensive per unit, they end up bringing better power density to the table, said Navitas.

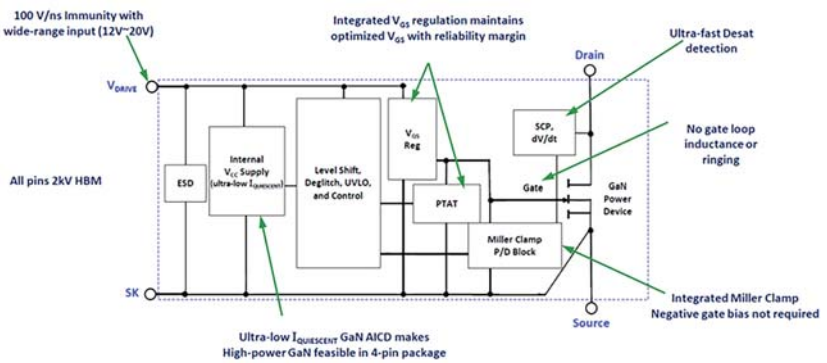
Oliver pointed out that "if you want three times more power, it's a lot easier to slide in GaN power electronics. Upgrading from silicon, which is at the end of its life, to GaN is a game changer for the data center."

GaN Geared for AI Power Delivery

Navitas is upgrading its GaN power ICs to check more of the boxes for AI power delivery in the data center.

GaNSafe is based on the same basic blueprint as its existing GaNFast family, integrating a dc-dc bias supply and gate driver with control and sensing in a single chip to deliver higher power density. But they also add "application-specific" protection features into a 10- × 10-mm, 4-pin TOLL package, which is physically more robust to survive mechanical fatigue as well as harsh temperatures and other grueling operating conditions.

According to Navitas, the GaN power ICs are significantly larger and 2.5X thicker than the last generation to improve their power-handling capabilities. The power FET inside operates at voltages of up to 650 V—typically, the upper limit for GaN—with the ability to tolerate large transient voltages of up to 800 V to aid with survival in extraordinary conditions.



Navitas is upgrading its GaN power ICs with integrated control, drive, sensing, and protection to handle the harsh realities of high-power systems.

Navitas said the family covers a range of $R_{DS(ON)}$ from 35 to 98 mΩ.

Targeted at 1- to 22-kW systems, the GaNSafe chips also have protected and regulated gate-drive control, with minimal gate-source loop inductance to curtail ringing and reduce the risk of damaging voltage spikes. Reducing the inductance also opens the door to reliable high-frequency switching of up to 2 MHz. Faster switching rates allow for the use of smaller transformers, chokes, capacitors, and other passives in the system, adding to power density. GaN also increases slew rate during turn-on and turn-off, limiting switching losses.

Rapid responses prevent unusual conditions in the power electronics from affecting the rest of the system. "Safety in this context means the power supply won't fail," said Oliver. "Data centers are all about uptime."

To effectively reject EMI, GaNSafe is equipped with programmable resistors and diodes at the input and output pins, enabling precise and dynamic control of turn-on and turn-off speeds (dV/dt).

Don't Overlook Data-Center Power Supplies

The TOLL package is a cut above in terms of mechanical durability and heat dissipation. Navitas said the new packaging gives its GaN power ICs more robust performance compared to multichip modules (MCMs), which require three times as many connections and have trouble staying cool. The TOLL package is also equipped with a larger, thicker copper pad to optimize heat removal.

While the TOLL package is easy to cool compared to a standard QFN, the high efficiency of GaN also rejects heat. "For every watt of power burned on the way from the power supply to the processor, that is another watt that you have to air condition away from it," said Oliver. The rule of thumb in data centers, he pointed out, is that for every dollar you spend on electricity for a processor, you spend another cooling the system.

While the power supply itself is easy to overlook, even small efficiency gains when converting power add up for hyperscalers when the process happens as often as it does in data centers. As their fast-switching speeds reduce the area, weight, and cost of the passives in a power supply, Navitas estimates its new GaN power ICs save 5% of the LLC-stage cost, plus more than $60 of savings per power supply in electricity over three years.

Despite its advantages over silicon, upgrading to GaN power supplies is not a cure-all for the challenges of powering AI chips, which will require many other changes up and down the power-delivery network (PDN). ed

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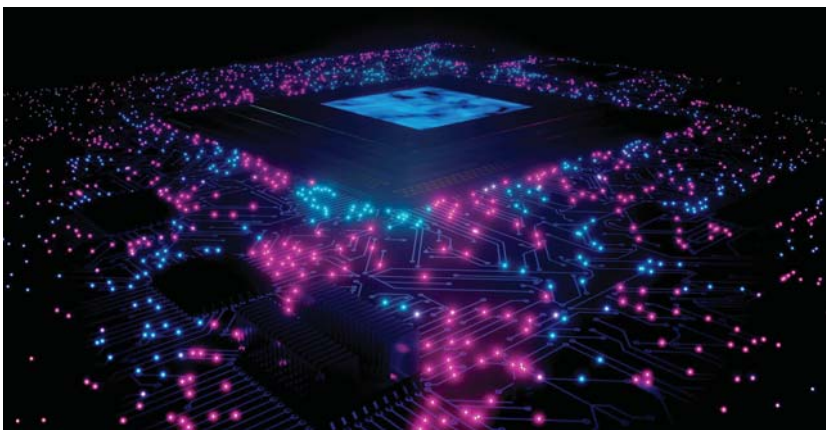


Edge AI: Rewards are Matched by Challenges

Intelligence and the edge—what could possibly go wrong? Plenty, it turns out, whether it's power limitations or security concerns, among other issues.

AI AND THE EDGE are made for each other. But that doesn't mean it's easy to make edge AI work. In fact, numerous potential "gotchas" can derail an edge AI initiative.

The edge, a huge physical and logical space at the periphery of the enterprise, including the mobile and vehicular world, is a frontier being explored and exploited more than ever. And, of course, AI has been the biggest buzzword of the last few years. Combining the two can certainly make lots of sense since AI has the potential to make the edge more independent of central control and more useful, too.

Edge AI usually involves applying algorithms that can make decisions and predictions in near-real-time. The general challenge has been to get compute-intensive AI to succeed within edge resource constraints. So, it isn't something to undertake casually.

One of the rationales for the edge is that local processing reduces latency as well as bandwidth needs and compute loads at a data center. So, the promise of AI at the edge is that it can make edge computing even more effective by pushing decisions closer to the data.

But edge AI can quickly bump up against realities that make it harder than might be expected.

Set Your Expectations, Have a Plan

Before diving into edge AI too deeply, spend some time thinking about what you want to accomplish. Is the right kind of data available to support that goal and what kind of processing will be needed and, therefore, what kind of hardware or cloud resources would likely be required?

With some of those ideas organized, you can begin to make some rough calculations about the cost, feasibility, and potential payback of implementing edge AI.

Powering the Edge

Power is a more important consideration at the edge than it would be in the cloud or in a data center. It may be that an AC power source is "dirty," e.g., subjected to variations or noise due to nearby industrial activities like welding. Or it may be limited by existing wiring or lack thereof.

In the case of the many edge activities, such as simple temperature and vibration sensors that can function well for long periods on battery power, adding local AI hardware and software can be thwarted by the much greater power needs they bring.

So, efficiency is a necessity and options that can keep power consumption low are important. Extensive deployment of edge AI will likely require a review of the system-wide power architecture.

Options for implementing power conservation include low-power chips, hardware accelerators to make processing more efficient, and power-management systems that can optimize power use for specific goals.

Compute and Memory Needs for the Edge

Recognizing how AI functions in a computing environment is far more important with the resource constraints of edge. For instance, many mainstream microprocessor CPUs consume a great deal of power in accomplishing iterative-rich inference processes. This architecture also tends to run slower than might be desired. Hardware accelerators or even GPUs can help improve performance while reducing power consumption. Systems that can "sleep" when not processing also save energy.

Faced with limitations of existing AI hardware, NIST researchers are exploring alternatives that use new technologies such as Spintronics for Neuromorphic Computing.

The reality of edge—limited power, etc.—usually means that hardware options

for running AI processing are limited, too. But vendors such as TI offer embedded processors that can run AI algorithms. When "low-code" software is added to the mix, the compute and power challenges can become more manageable. And these types of processors also offer good performance. For example, TI's AM62Ax, aimed at battery-powered systems, operates at 2 teraoperations per second (TOPS).

Single-chip microcontrollers designed for IoT systems often combine a general-purpose CPU, SRAM, non-volatile memory (NVM), and I/O functions. However, performance limitations generally confine these devices to basic inference AI software.

Systems-on-chips (SoCs) that include accelerators can potentially deliver more performance. NVM doesn't always go along for the ride due to chip geometry limitations and costs.

If costs aren't critical, AI performance can be achieved with a two-chip approach including some form of NVM.

Software Side of the Edge

The limits of edge hardware and the need for efficiency has encouraged the creation and adoption of lightweight algorithms and coding. Training, an important element in many AI/ML deployments, is a time-intensive process that can be especially frustrating in an edge environment.

Developing the AI model that will be deployed on the edge device involves training the model using a dataset that's representative of the use case, and then deploying the model to the edge device. If realistic training can be accomplished in another environment, it can save time and allow for more convenient and thorough testing.

Finally, commercially available tools can help create a "low-code" or even "no code" environment for developing and testing AI models. Some provide guidance to those new to AI programming.

Into the Cloud

Latency is always a concern with edge AI, which often makes cloud options less compelling. Nonetheless, all major cloud players offer edge AI options, including AWS, IBM, and Microsoft Azure.

AI's Role in Security Efforts?

In general, the edge has often been where security concerns arise. Physical access to the edge (depending on how it's defined) can be hard to control, potentially allowing bad actors to access or potentially even tamper with edge AI. Data can be lost through physical access as well as network and device communication means.

On the other hand, AI can provide more intelligence and insight at the edge. It could assist security efforts and, more importantly, reduce the amount of data needing to be handled and protected elsewhere in the enterprise.

Still, there are plenty of risks to think about.

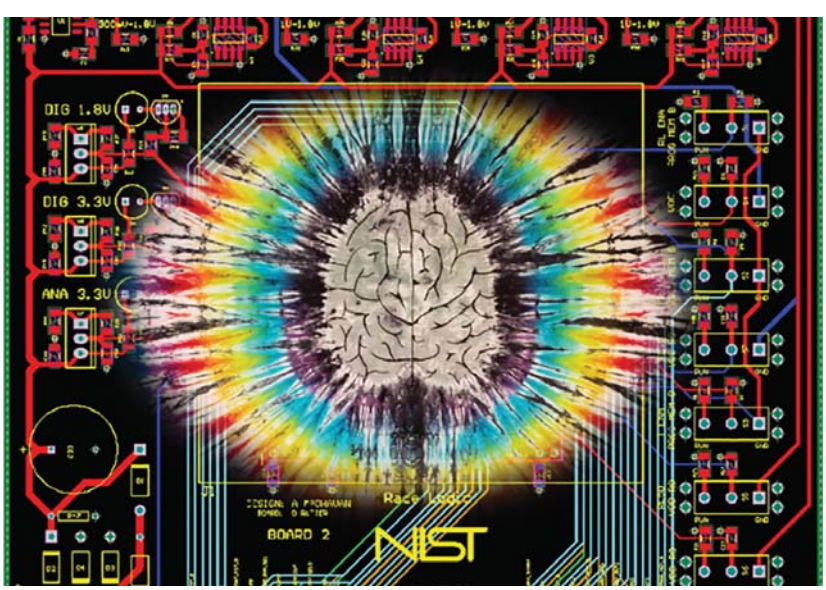
Loss of personal data can be a significant concern in some edge AI use cases. For example, customer data can be captured and used at the edge, including by AI. Ensuring that AI handles this data in accordance with company practice and regulations, such as GDPR and California Consumer Privacy Act (CCPA), is essential, particularly given the value attached to this data by hackers who might target edge sites.

External attackers can brew up other kinds of trouble for edge AI, too. One of the most serious involves an attacker injecting incorrect or extraneous data or interrupting a desired source of data. The motivation is mostly malicious, resulting in things like manufacturing errors or, with vehicle controls, potentially leading to injury. This technique can also be used by an attacker to learn about how a system operates to enable further, more sophisticated attacks. These "inference attacks" may reveal sufficient data to reverse-engineer systems or products.

Finally, of course, edge systems could be hit by the same kind of DDOS attacks and viruses that affect other systems. On top of that, insiders unfortunately can continue to be a source of problems.

REFERENCE

"Artificial Intelligence-Assisted Edge Computing for Wide Area Monitoring," NIST.



Faced with limitations of existing AI hardware, NIST researchers are exploring alternatives that use new technologies, such as Spintronics for Neuromorphic Computing. *NIST*

FAQ

Incorporating High Power Relays into Solar Power Applications

With the proliferation of the use of solar power systems throughout the country, designers need components that are right for each segment of the system. Understanding what is required and what is available is key to designing a quality system.

Q1: How are relays used in solar power applications?

Solar power is considered a photovoltaic generator and is comprised of one or more solar panels along with an AC grid inverter that is interconnected with the public power grid. These systems may also include batteries for storing solar energy and a battery charger that is integrated with the AC inverter. These systems can vary in size from rooftop systems to utility-scale generation plants.

Q2: How is the DC voltage created from a solar power system converted to AC voltage?

Direct current voltage generated by solar panels is converted into alternation current through the AC converter. This voltage is either fed into the power grid or collected by receivers that are connected directly to the system. The inverter provides voltage to the connected AC receivers from the solar power system batteries or the power grid and allows it to be redirected directly from the AC grid input to the inverter output. If the absorbed energy by the receivers is greater than the energy supplied by the solar power system batteries, the DC/AC converter works in bypass mode, switching to power from the public grid.

Q3: Where are high-power relays incorporated into a solar power system?

High-power electromagnetic relays used in solar power systems have two main purposes. Relays are used on the DC side to switch DC voltage generated by the photovoltaic cells off and on. On the AC side of the system, high-power relays are used to connect or disconnect the entire system from the power grid (see Figure 1).

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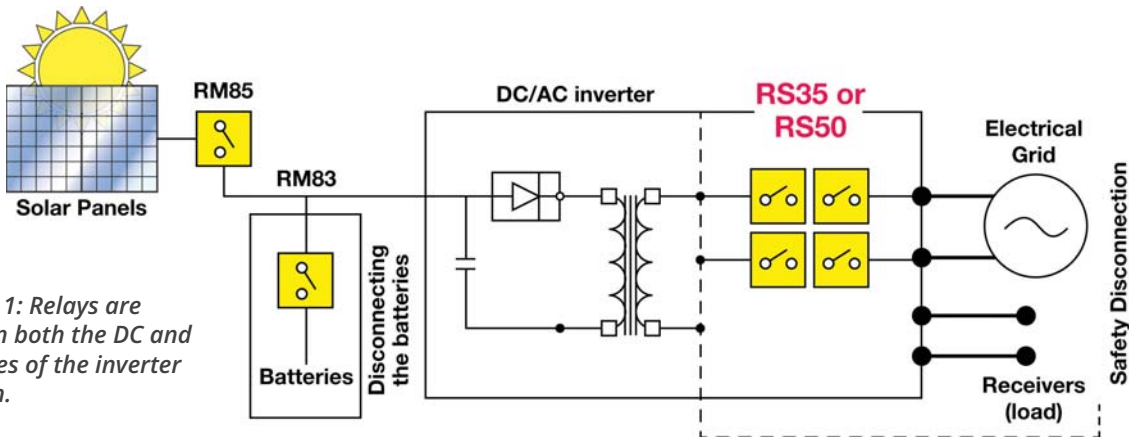


Figure 1: Relays are used in both the DC and AC sides of the inverter system.

Q4: Are there special requirements for relays used in solar power systems?

Any time there is a supply of energy to the public grid, it is susceptible to special requirements relating to the relays being incorporated. Some important requirements include a minimum contact gap of 1.5mm, a minimum open contact dielectric strength of 2500 V rms, low holding power for the coil and a wide temperature rating.

Q5: What is meant by an "automatic system"?

An automatic system refers to safety regulations. A solar power system must be equipped with an automatic system that disconnects the generator from the AC power grid for safety reasons. This protection circuitry is often built into the DC/AC inverter. Two-pole relays are used so that each contact disconnects a separate line during emergencies—the single-phase line and the neutral line in a single-phase application and two phases in a two phase application. Two contacts connected in series are required for each line. The separation of the circuit is therefore carried out by two two-contact high-power relays.

Q6: What relays are recommended for this type of application?

Altech has partnered with Relpol to provide high-power relays for these applications. Their RS35, RS50, and RS80 relays are specifically designed in accordance with the requirements of many safety standards, including the DIN VDE 0126-1-1, to fulfill the needs of users. The RS35 relay, with a switching power rating of 8750 VA, is intended for smaller solar power systems such as those installed in single-family homes. The RS50 relay, with a switching power rating of 12,500 VA and the RS80 with a switching power of 20,000 VA are designed for larger industrial systems (see Figure 2).

Figure 2: The RS35 and RS50 high-power relays for solar power systems are designed in accordance with the requirements of DIN VDE 0126-1-1.

Q7: Is relay power consumption an important factor in solar power applications?

Yes, that is one of the most important elements To ensure the highest efficiency of the inverter, the power relay components must have the lowest possible power consumption possible. That is why the RS35/RS50 high power relays are equipped with coils that are rated for only 0.4 Watts of power consumption. Heat emission is also significantly reduced by decreasing the supply voltage of the relay coils after activation. For example, for a relay with a 12V coil, the minimum supply voltage used during continuous operation can be as low as 5V. This means that power consumption is only 85

mW, which translates into high efficiency for the entire device.

Q8: Are their relays available for printed circuit board use?

Yes, the RS35, RS50, and RS80 relays are designed for PCB mounting. In addition to the RS type relays, Altech supplies many other varieties of relays. For example, the company offers the RUC relay line specifically for printed circuit board designs—with a contact gap of 3mm. These relays are available in both 2NO and 3NO configurations, which allows them to be used in three- phase designs in addition to single- and two-phase systems.

Q9: What high-power relays are available for DC voltage disconnection?

An array of products are available for all areas of solar power systems, including disconnecting the voltage generated by assemblies of the photovoltaic cells such as on the DC side of the inverter. Disconnecting the system on the DC side is often required for safety reasons—in the event of a failure—as well as during service inspections or for test and measurement purposes. Altech also offers relays for this purpose. Their RM83 and RM85 offer an increased contact gap ideal for these applications (see Figure 3). The relays can also be used to disconnect the battery system or be used in the equipment that calibrates the angle of inclination of the solar panels.

Figure 3: A wide variety of power relays for the solar power industry are available, including Altech's RM83 and RM85 used for DC voltage disconnect.

Q10: What other applications might require high-power relays?

Power relays are a versatile component used in a wide variety of industries, including industrial automation and home automation, telecommunications systems, lighting and safety monitoring, automotive electronics, computer systems, battery testing equipment, elevators, and numerous industrial control applications. High-power relays have become key components in many circuits for a variety of safety reasons, including protecting humans as well as protecting other electrical or electronic equipment.

CABE ATWELL |
Technology Editor

AI's Impact in the **Engineering Workplace**

AI is already playing an increasing role in the engineering workplace, but is integration of AI an inevitability? Electronic Design's Salary Survey brings this issue to light.

WE KNOW THIS: Artificial intelligence (AI) is a useful tool, time-saver, and a crutch in some cases. When some technological breakthrough rolls out, we instinctively gravitate to it and, in turn, it becomes a part of our daily lives. Take the iPhone and subsequent touch-based phones that came afterward. They are, without a doubt, essential to our lives, fitting like a glove in how we access the world. And AI is following the same path.

Countless large data projects use AI to, for example, model molecules, detect cancerous cells, and/or enhance CRISPR tools or the production of biomolecules and materials. These are constantly running, constantly producing results that aren't possible with humans. The world of electronics has embraced AI, like machine-learning applications, circuit design, simulation, etc. Take Synopsys DSO.ai, launched in 2020. It has already produced over 100 production tapeouts through increased workflow optimizations and reduced design times.

Such increased productivity and accuracies through AI come at a cost. CNN reported that 212,294 jobs were lost in the tech industry in 2023 due to AI. Goldman Sachs predicts that 300 million jobs will be impacted in the next five years (via Forbes).

This is what humans do, we use technology and displace the old ways. Over 200,000 elevator operator jobs were lost with the use of automatic elevators. It took years to replace all of those workers. AI, on the other hand, is hitting us all fast—11 months and over 200k jobs already gone.

That said, AI will steadily grow in the workplace, which is indicative of the numbers detailed in a 2022 report from Global Market Insights. According to the report, the AIU engineering market is expected to grow by 35% by 2032 with a market value of $180 billion, up from $8 billion in 2022. That number alone is striking, considering it's a base driver for business expansion and long-term research projects in the AI engineering market.

Since ChatGPT launched, more engineers and companies have taken notice of AI's potential, making it a top conversation across multiple industries and workplaces. From the instances of what ChatGPT has been used for in that time makes it easy to see why AI has been gaining momentum across the engineering fields.

How is AI Leveraged in the Workforce?

AI in the engineering workplace is broken down into hardware and software components. As machines become more sophisticated, they will support not only smart production lines and complex manufacturing tasks, but will also be able to design and improve tasks over time via machine learning (ML).

This is evident in many industries such as automotive and aerospace. However, it's also becoming more beneficial in the design phase of other industries, including using ML to glean insights

from other departments to make the design process more efficient with increased precision.

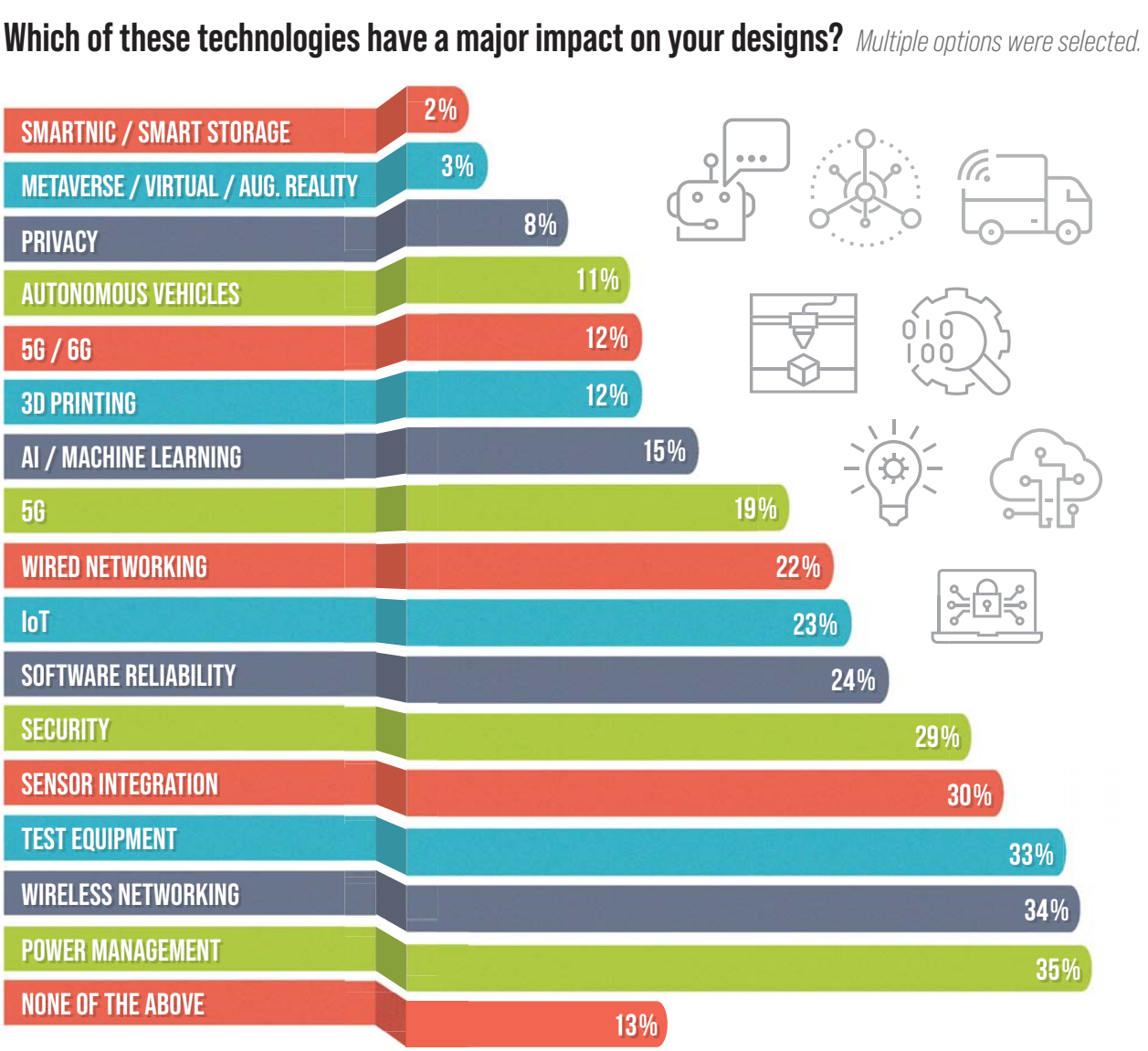
AI is also being leveraged in the electrical engineering field, with the most prominent being the automation of routine tasks, including those for circuit design, component selection, and system analysis. It's also being used to provide new tools and techniques to aid in solving complex problems.

For example, engineers can use AI to create models that learn from data to make predictions based on a number of external factors, such as operating environments, temperatures, and power usage via simulations. Software engineers have taken advantage of AI to streamline repetitive coding tasks, including code conversion, converting data maps, and generating working unit tasks.

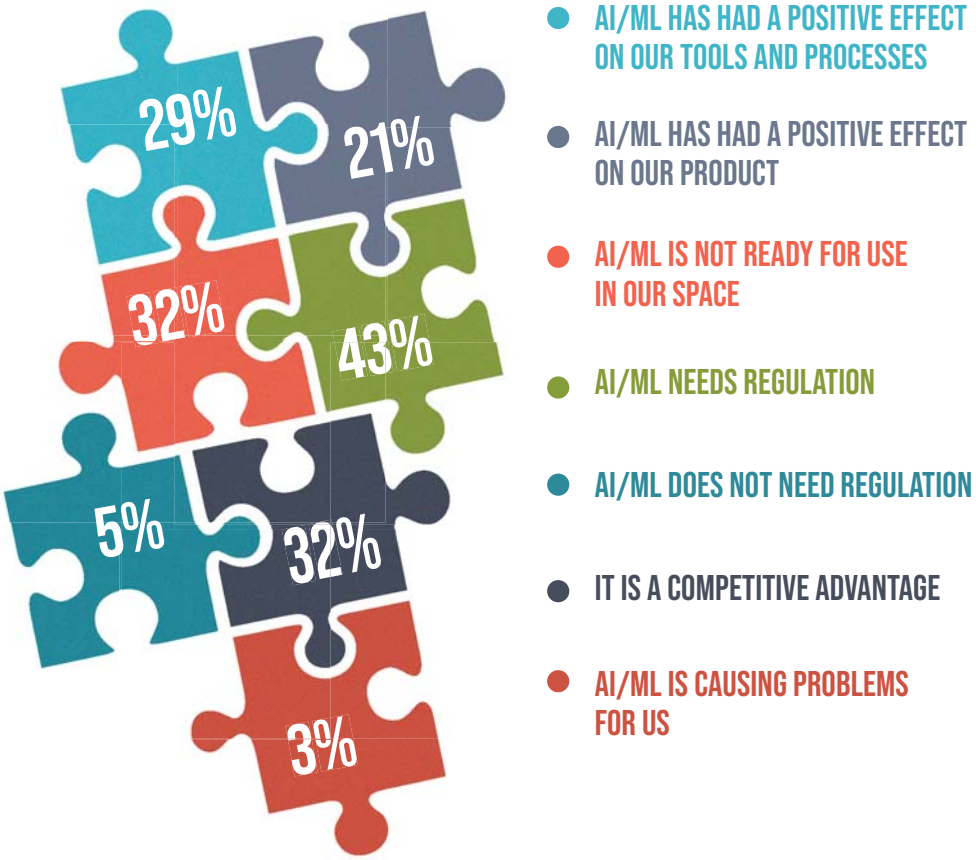
What Does the Survey Say?

According to a recent survey conducted by *Electronic Design* and others in the Endeavor Business Media group *(Fig. 1)*, which polled engineers from diverse fields and garnered 1,977 responses, 21.25% stated AI and ML technologies have had a major impact on their designs. That's a significant amount, especially for a diverse group, with most employed in the design and development fields.

Another good portion of those engineers polled currently design industrial control systems and equipment, areas where AI tools help streamline everything from component placement to predictive maintenance.



1. A significant number of engineers utilize AI and ML in their current projects across a number of fields. *Electronic Design*



2. Not all companies and engineers utilize AI in the workplace, as some are in the evaluation process, while others feel it needs regulation before being implemented. *Electronic Design*

Of course, not all engineers see AI and ML as beneficial in the work environment. Among those polled, 7.46% have considered leaving the profession due to its impingement or the fear of eventually being replaced. These numbers aren't a reflection of engineers on a national scale, but they do represent the notion that some do consider AI to be a detriment to the profession.

For example, the same survey shows that some businesses and companies are still evaluating the use of AI in their practices *(Fig. 2)*, while a good portion don't use it at all. Most feel that AI needs to be regulated before being implemented, while others say it provides a competitive advantage. Still, 3.59% feel AI is causing problems in the workplace or job functions.

Revolutionary—with Caveats

The integration of AI in the engineering workplace represents a transformative approach in much the same fashion as the industrial revolution, with its advantages and challenges. AI has provided engineers with powerful tools to automate tasks, optimize designs, and solve complex problems, which have led to increased efficiency and innovation. It has the potential to revolutionize the engineering fields, allowing workers to create complex projects at immense scales.

It also has its drawbacks, as AI raises concerns about privacy, security, and biases within the algorithms themselves. Ethics is a serious concern, too, certainly when it pertains to intellectual and proprietary technologies and those who create them. These issues must be addressed—the concerns are valid and legal issues are already being scrutinized.

Ultimately, successful integration of AI in the engineering workplace will hinge on a thoughtful, ethical, and forward-thinking approach to maximize its benefits while mitigating its drawbacks. AI everywhere is an inevitability, but how we see it and use it will decide our fates.

JUSTIN MOLL | Vice President of Sales & Marketing, Pixus Technologies

What's Trending in **SOSA-Aligned OpenVPX Chassis?**

Heat dissipation takes center stage in SOSA-aligned OpenVPX chassis. New methods of chassis cooling and the latest in backplanes are discussed.

PRODUCTS EMANATING FROM the Sensor Open Systems Architecture (SOSA) consortium continue to gain traction in the Mil/Aero embedded-computing market. A primary goal of SOSA is to limit the wide variation of MOSA (Modular Open Standard Architecture) designs to a more manageable level. The benefits to the military (at least theoretically) are ease of integration, less training time, a more plug-and-play ecosystem, less confusion, less vendor lock, lower costs, and more. It also gives them the ability to have a more manageable innovation process.

By proving the military's design goals at the front end, this helps the engineering groups in the open standard committees to come up with appropriate solutions. This hand-in-hand approach keeps the design community focused and solutions-oriented.

SOSA is primarily focused on 3U and 6U OpenVPX-based open standard systems, but other specialty architectures are also emerging. SOSA is leading the "demand" for certain routing profiles for the backplane that accept certain slot profiles for the OpenVPX boards. From a chassis platform perspective, SOSA's efforts are driving the backplane speed requirements, hotter plug-in cards that require more advanced cooling solutions, the RF and fiber interfaces that lead to new I/O solutions, and chassis management.

1. One way to manage faster and hotter plug-in OpenVPX boards is via a SOSA-aligned enclosure, which provides airflow over the fins of specially made conduction-cooled card mats. It can cool over 1500 W in the system. *Images courtesy Pixus Technologies*

Backplanes for SOSA-Aligned Systems

Backplanes requiring 100 GbE (4 lanes of 25 Gb/s) and often PCIe Gen4 (16 Gbaud/s) are common for SOSA-aligned systems. However, 40 GbE is often acceptable. The backplanes will typically have fiber and/or RF interfaces.

We're seeing clear delineations of which versions (NanoRF, SMPN, MT options, etc) that are commonplace. The NanoRF is particularly notable as it offers up to 20 RF interfaces along with MT fiber and comes in various mixes/configurations. The MT ferrule options are expanding from the supplier base with 3 MT and even 4 MT options (which typically have 12- and 24-fiber options) that fit into the standard VITA 67.3c or VITA 66.1 envelop size, respectively.

Chassis Cooling

The high-wattage systems are driving more advances in cooling. A 19-in. Mil rugged rackmount chassis *(Fig. 1)* can be designed to hold up to 16 slots of VITA 48.2-compliant conduction-cooled boards. With special card mats, the heat is dissipated to the fins where airflow can be applied with Mil-grade fans to cool the fins. The approach as a rule of thumb can cool approximately 100 W/slot.

In a fully loaded 16-slot system, a mezzanine-based chassis manager can affix to the rear of the backplane, so that it doesn't consume any slots. The "Tier3+" SOSA-aligned chassis manager can monitor/control intelligent fans and SOSA VITA 62 power-supply units (PSUs), provide graceful shutdown and sequenced initialization of plug-in boards, and much more. The specification requires the use of a SOSA-aligned chassis manager in the enclosure platform.

Similarly, this approach can be utilized in an ATR format enclosure. The ATR *(Fig. 2)* can also be designed with special I/O interface boards both on the front and rear of the enclosure to provide more

I/O space. It should be noted that not all applications would allow for this type of configuration.

For even hotter system requirements, there are newer airflow approaches *(Fig. 3)* such as VITA 48.7 (Air Flow By) with airflow over the fins of the plug-in cards, VITA 48.8 (Air Flow Through), and new concepts meant to optimize slot spacing with similar approaches. Liquid cooling is often the last resort with its own complications, high costs, smaller ecosystem, and infrastructure requirements. However, some of the high-end SOSA designs (and future aspirations) seem to make the use of liquid cooling inevitable.

I/O Considerations

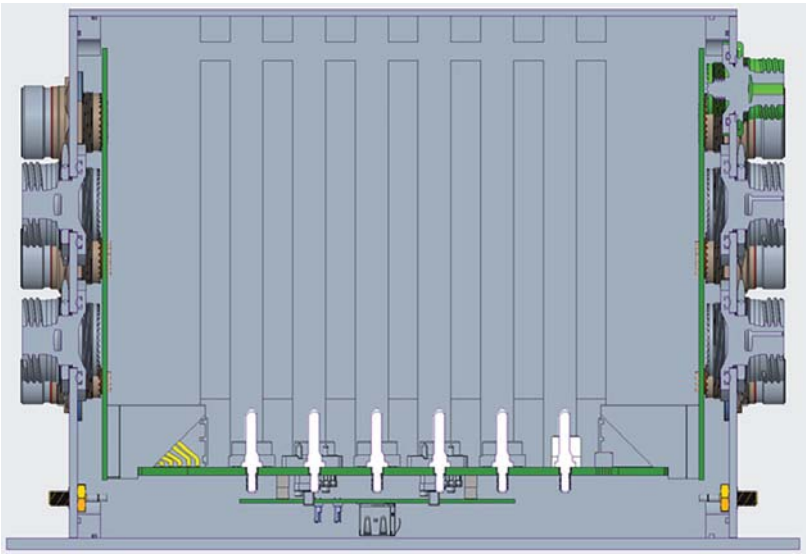
As discussed, in the unit shown in *Figure 1*, these applications sometimes require a wealth of I/O interfaces. While SOSA may limit some of them (or shift more to fiber, etc.), many designs have almost more I/O than space is available by typical means.

One potential solution is the use of a special serial multiplexer board that provides for the condensing of multiple serial ports into one compact interface. This type of design can save significant I/O panel space in a chassis platform.

In this example, a single USB 2.0 Micro interface on the multiplexer mezzanine board allows for 28 UART connections, two USB interfaces, and a chassis manager interface on a board that measures approximately 50 × 112 mm. The board can be mounted to the rear of a backplane like a mezzanine in the same type of approach as the SOSA-aligned chassis manager described earlier.

An Exciting Future

While SOSA applications look to have a bright future, a wealth of other designs still don't need to meet those requirements. As mentioned, SOSA has many benefits, but it can be overkill, or conversely, too restrictive for many design needs. It will be exciting to see the continued evolution of SOSA and other MOSA technologies for Mil/Aero applications.



2. Placing a mezzanine-based, SOSA-aligned OpenVPX chassis manager below the backplane saves a slot from being consumed.

3. The VITA 48.8 specification provides for airflow to go through the modules themselves, enabling more heat to be dissipated in the system.

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SHEKHAR KAPOOR | Sr. Director of Product Management, Synopsys

Multi-Die Systems Reshape Semiconductor Innovation

Explore the main driving forces behind today's multi-die systems, how they're becoming the choice system architecture, and how they're catalyzing the next wave of semiconductor innovation.

DEMANDS HAVE NEVER been higher for—and on—semiconductors. From smart speakers to self-driving cars and robotic manufacturing equipment, chips are elevating our smart everything world to new heights. In 2021, the semiconductor industry marked a record by shipping 1.15 trillion chips. Increasingly, as applications become more intelligent, these chips are being asked to deliver much more processing prowess, better power efficiency, and, for space-constrained designs, smaller footprints.

It's a promising and exciting time for the electronics industry, with transformer models, generative artificial intelligence (AI), and immersive experiences creating unprecedented demand for compute and data rates at ever lower power levels. As a result, new players are entering the chipmaking landscape and bringing to life innovations that are transforming the way we learn, work, play, and, when you think about it, live.

However, all of these chipmakers are facing deep limitations as Moore's Law slows, particularly for designs targeting compute-intensive workloads.

The reality is, migrating traditional, monolithic semiconductor designs to smaller process nodes is no longer generating the benefits that such scaling once did. And attempting to do so will even hit manufacturing walls.

To meet the challenges of scale as well as systemic complexity, more chipmakers are turning to multi-die systems. An interdependent architecture that provides integration of heterogeneous dies, or chiplets, in a single package, multi-die systems enable accelerated scaling of system functionality *(see figure)*.

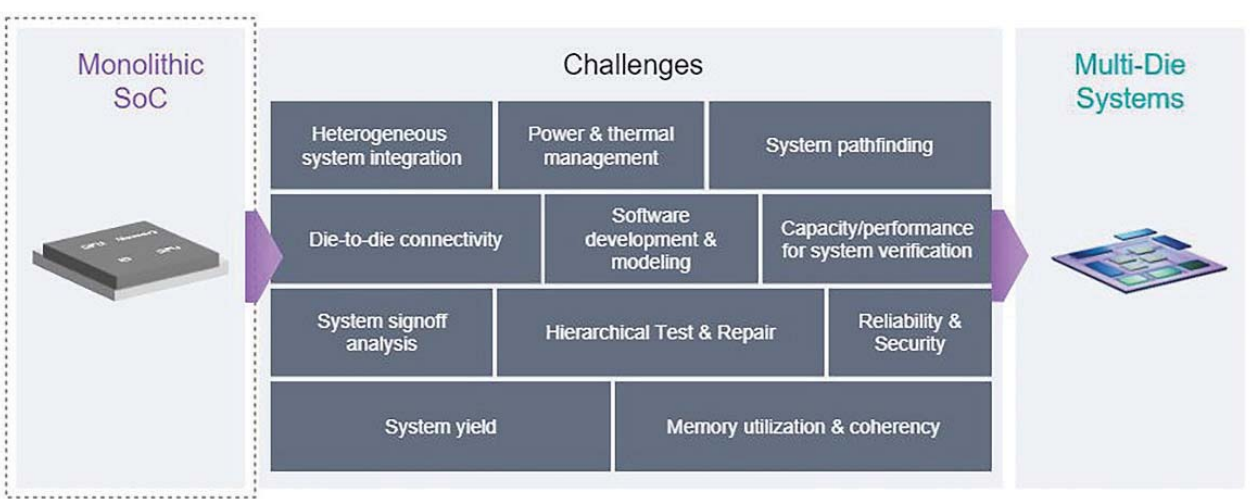
Designers can also reduce risk and time-to-market, lower system power, and more quickly create new product variants. Multi-die systems are becoming the system architecture of choice for applications like high-performance computing (HPC), autonomous vehicles, mobile, and hyperscale data centers.

This article examines the main drivers of multi-die systems, how they can generate bottom-line benefits, and how they're moving innovation forward.

What Makes Up a Multi-Die System?

Rather than a single SoC consisting of a processor, memory, and I/Os, a multi-design system is all of this and much more. Inside a single advanced package, you'll find multiple dies—potentially on different process technologies and for different functions.

There are different approaches to creating such a system. Disaggregation is one approach, whereby a large die is partitioned into smaller dies to enhance system yield versus monolithic dies. An example of a disaggregated, heterogeneous design is an automotive system in which different dies in the package are designated



Monolithic SoCs face many challenges that can be addressed by moving to multi-die systems. *Synopsys*

for disparate functions, such as sensing, object detection, and general compute. The disaggregated approach can also be applied to a homogeneous design, such as one that's disintegrated into multiple instances on the same compute chiplet.

Furthermore, multi-die systems can be developed by assembling dies from different process technologies to achieve optimal system functionality and performance. An example is a system with dies for digital compute, analog, memory, and optical compute, each at a process technology that's optimal for its function.

Dies in multi-die systems can be placed side-by-side or stacked vertically in a 2.5D or 3D package. Advanced packaging technology, along with interconnect standards like Universal Chiplet Interconnect Express (UCIe), are helping to usher in this new era of chip design.

What's Driving Demand for Multi-Die Systems?

The late Gordon Moore's 1960s observation that chip density would double every 18 to 24 months has continued to drive innovation in the semiconductor industry. However, increasing systemic and scale complexities are pushing the limits of Moore's Law.

Compute-intensive applications like hyperscale data centers and AI/machine learning (ML) are flourishing, while the data itself has become more complex given the emergence of bandwidth-hungry machine-to-machine communication. Massive SoCs with trillions of transistors can support some of these applications.

But as die sizes hit the reticle limit of the manufacturing equipment, adding more transistors to support application demands requires adding more chips, which leads to impossible-to-achieve die sizes. There's also a steep learning curve to ramp up production for desired yields.

Multi-die system architectures provide a way to address the learning curve, along with yield and silicon cost concerns. Not every function needs to be on the most advanced process node. By mixing and matching dies from older technologies with those on more advanced nodes based on their targeted functions, design teams can reap the benefits of a better performance/cost ratio as well as better yields.

There are also manufacturing advantages, because multi-die systems don't involve the very large dies that come with greater yield risks. What's more, by reusing silicon-proven dies, designers can speed up time-to-market for their systems.

The convergence of four key drivers is moving the needle toward multi-die systems:

- ***Growing functionality:*** In the face of reticle limit challenges, applications are demanding higher bandwidth, lower latency, and substantially greater compute performance.
- ***Power predicaments:*** Splitting up a large design can more effectively address the power requirements that vary based on target functions.
- ***Opportunities to serve multiple end markets:*** Optimized, modular architectures provide a faster way to develop product variations and, thus, capitalize on multiple business opportunities.
- ***Cost:*** Achieving the level of yields for the types of chips that can address today's complexities has become prohibitively expensive.

Companies that haven't traditionally designed their own chips are now doing so, in the interest of achieving differentiation for their unique market requirements.

From the digital behemoths creating immersive online platforms to hyperscalers building out massive data centers and AI innovators developing the next intelligent product, these companies are in many ways driving the evolution of multi-die system architectures. AI companies may seek a specialized architecture to boost performance of ML algorithms, while a hyperscaler might want to find the ideal power/performance balance to support compute-intensive workloads and operate as energy efficiently as possible, for instance.

What are the Key Challenges to Designing Multi-Die Systems?

The shift from monolithic SoCs to multi-die systems can be likened to the move from hand-drawn schematics to RTL and synthesis so many decades ago. The latter was made possible by electronic design automation (EDA) technology, which brought software and hardware solutions to automate the flow to design and verify chips. Today, advances in chip packaging technologies and the emergence of industry standards such as HBM3 and UCIe are enabling heterogeneous integration of dies.

On the packaging front, there are a variety of types to choose from, based on advantages in performance, area, and connectivity, including silicon interposers, redistribution layer (RDL) interposers, fan-out wafer-level packaging, and hybrid bonding.

As for the standards, they help to ensure quality, consistency, and interoperability. HBM3 provides high-capacity memory, preventing memory bottlenecks in 2.5D multi-die designs. UCIe is fast becoming the de facto standard for die-to-die interconnects, providing the bandwidth, low power, and low latency for package-level integration of chiplets.

The challenges involved in developing multi-die systems balloon due to the interdependencies in these complex systems.

With so many interconnected components, multi-die systems are best considered from a system-wide perspective. A co-optimization approach that simultaneously addresses the system, the dies, and the package can help optimize performance, power, and cost.

But, as with any complex system, many questions arise: How should the dies be split? What's the best type of packaging to use? How do you ensure that your system will perform as intended? How do you develop such a system under aggressive time-to-market targets? And so on.

To read the article in its entirety, go to: https://www.electronicdesign.com/21274821.

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Through the Substrate Looking Glass

Intel is looking to use glass, which has strong thermal and mechanical characteristics, as a substrate for chiplets.

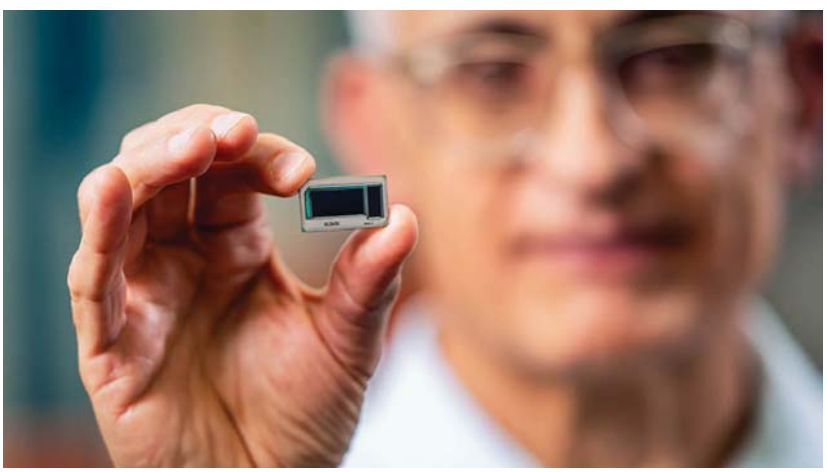
CHIPLETS AND ADVANCED packaging have been on the cutting edge of electronic technology for a while, but Intel is changing where it might be headed. Today's organic substrates, like Ajinomoto build-up film (ABF), are getting some competition from a common material—glass.

Glass has great thermal characteristics. It can be extremely flat, which is useful in chiplet applications, and it has very good mechanical characteristics. Intel is now showing off its glass substrate solution, one that could wind up in shipping devices in a couple years.

I talked with Jim Handy, an analyst at Objective Analysis, about Intel's latest announcement.

The use of chiplets in system-on-package (SOP) devices is becoming more common, especially when employing the latest transistor node. Mixing technologies in a device using chiplets based on different nodes or technologies allows for more effective designs as well as making construction less expensive. Standard chiplets like high bandwidth memory (HBM) and interconnect standards such as the Universal Chiplet Interconnect Express (UCIe) facilitate heterogeneous integration.

Intel has been producing, but not selling, glass-based devices to test out the technology and production requirements *(Fig. 1)*. So far, the results have been excellent. The glass substrate has half the pattern distortion compared to the competition, and the ultra-low flatness improves depth of focus for the lithography support. It also helps enhance dimensional stability required for extremely tight layer-to-layer interconnect overlays. This, in turn, allows for higher-density connections.

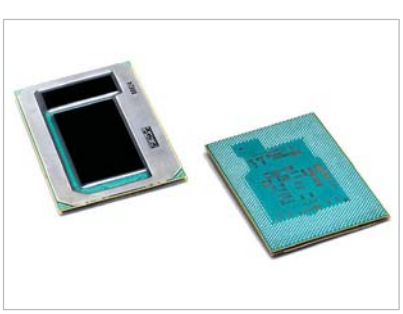


1. Intel is in the process of producing chips based on glass substrates. *Images courtesy Intel*

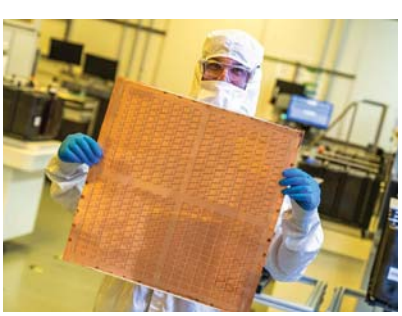
The company has created devices using its latest technology *(Fig. 2)*. The yield with glass is also better, as glass substrates can handle higher temperatures. This affects everything from signal routing to power delivery. Integration with components like resistors, capacitors, and inductors is possible, too, due to the higher temperature support.

Intel projects that glass substrates will first target applications that utilize chiplets and large form-factor packages. This includes data-center applications where high-density system-on-chip (SoC) solutions are used for CPU core counts in the hundreds and, in the future, thousands of cores. It's also where large amounts of memory with high-bandwidth connections will benefit applications. Another area where glass substrates may have an advantage is optical connections.

The company has been working on glass-substrate technology for more than a decade. The latest announcement shows off its production capabilities *(Fig. 3)* as well as where its headed. ed



2. System-on-package devices were created using chiplet technology.



3. Glass substrates can be manufactured to any format, unlike silicon that comes in the form of circular wafers.

ULRICH HOFMANN | Co-founder and Co-CEO, CTO, OQmented

Solve Augmented-Reality Display Challenges with **Laser Beam Scanning**

MEMS-based laser beam scanning (LBS) engines offer an alternative solution to current AR technology challenges, leading the way to stylish, lightweight, affordable, and powerful consumer AR glasses.

BILLIONS OF U.S. DOLLARS HAVE been invested in display technology for augmented-reality (AR) glasses *(Fig. 1)*. However, from startups to tech giants, companies have failed in delivering truly wearable consumer AR glasses. Some have confined themselves to enterprise or military solutions.

The available headsets suffer from major limitations, particularly their price point, bulkiness, and restriction to indoor use. These all come down to mainly one factor—display technology.

An adequate display solution has yet to be developed, so, some consumer wearable companies are creating workaround AR for their headsets. Cameras record the user's surroundings and digitally reproduce the scenery on the display of a closed system, which can then be augmented with digital content. One solution goes to the lengths of displaying the user's eyes, or some digital form of them, on another display, facing the outside world.

What they're all striving to achieve, though, is something else: Glasses through which you can see your real, actual surroundings and digital content at the same time, indoors or outdoors, hassle-free. There can be two different types of these glasses—a 2D, monocular smartglasses version to display rather sparse information, mostly text, and a 3D, binocular version for more immersive experiences that blend real with digital content.

Manufacturers have to meet a number of display-related challenges on the path to either one of the two types of AR glasses. This article defines those challenges and evaluates the different display solutions in this context. It explains how MEMS-based LBS technology is used in optical applications and discusses its advantages for AR displays.

Challenges in Building Displays for AR Glasses

Building truly all-day, wearable consumer AR glasses involves several requirements for the display technology.

There's the issue of social acceptance. The user wants to feel comfortable wearing the glasses among other people. This requires that the glasses look stylish, very similar to a normal pair of glasses, and offer design choices to the user.

Moreover, direct eye contact between the wearer and his/her environment needs to be possible, which calls for see-through lenses as opposed to a display facing the outside world, i.e., people looking at the wearer. The lenses must not project a large part of the light away from the user's eyes, lighting up the display and thus preventing direct eye contact, so-called eye glow.

Usability demands an operating time of at least eight hours, so that the user can wear the glasses for a long time without having to recharge them. For outdoor use, the projected images need to be very bright and high contrast to be able to compete with direct sunlight.

The wearer of the 3D, binocular version will want to experience a wide range of colors (color gamut) and high-resolution images with a large field of view (FOV), while the smartglasses version must deliver crisp text. The glasses' eye-box must be an acceptable size, meaning it should not be difficult to locate the glasses in the

1. MEMS-based laser beam scanning, combined with a waveguide, enables fashionable AR glasses with high-end displays. *Images courtesy OQmented*

right position on the nose whereby the user's eyes get to see the entire virtual image and not a cropped version. Consumer AR glasses also have to be a reliable product with an acceptable product obsolescence, especially if they were to be daily companions.

In terms of comfort, the glasses should not exceed a weight of 80 grams (adding only slightly to a pair of standard glasses). And the heat development in the temples must be kept to a minimum so that there's no discomfort for the user.

Lastly, the glasses need to have a reasonable price tag and be affordable to a relatively large number of consumers.

When combined, these requirements translate to the following challenges for AR display technology, where the display engine must:

- Be lightweight and small enough to fit into the temples of the glasses and leave enough room for other necessary components.
- Have very low power consumption for longer operating times and very high efficiency for minimal heat generation.
- Deliver sufficient brightness and contrast for outdoor use.
- Deliver high-resolution images with wide color gamut.
- Deliver fast image build-up.
- Deliver large FOV.
- Come with sufficient reliability for a long product lifespan.
- Use materials and a production process that provide for an affordable price (of the end product).

The issues of eye glow and eye-box size don't relate to the display engine, but rather to the used optical combiner.

Display Technologies for AR Glasses

Common display technologies for augmented reality are OLED, microLED, LCoS, and DLP:

- *OLED* (organic light emitting diode) is a self-emissive technology that can deliver high-resolution images. However, it doesn't deliver the necessary brightness for outdoor use and competition with direct sunlight, rendering it practically unfeasible for use in consumer AR glasses.
- *MicroLED* is another additive display solution, only creating light where it's needed. It's efficient for low-resolution images, but for a higher pixel resolution, it involves pixel pitch reduction. Aside from increasing in size, this means considerably lower efficiency and output brightness. The technology involves significantly high manufacturing costs and isn't producible in high yields.
- LED-based *LCoS* (liquid crystal on silicon) is an inherently subtractive technology. It involves a constant maximum backlight on top of a liquid-crystal matrix to subtract the amount of light that's not needed for the displayed image. The subtracted, black areas are converted into heat. This essentially wastes a lot of already generated light and energy.
- *DLP* (digital light processing) has the same shortcomings as LCoS in that it's also a subtractive technology. Both need an LED source and further illumination optics, adding to the system's size.

All of the above technologies require additional optics behind the panel, for projecting into a waveguide, and sometimes in front of it. This adds to the system's overall size.

In terms of resolution, these panel-based approaches have to increase size to boost resolution, meaning they must add more pixels to the panel. However, another, non-panel-based approach doesn't need to increase size.

MEMS-based laser beam scanning (LBS) systems offer several advantages for consumer AR glasses. The FOV or scanning angle of the MEMS mirror, hence the resolution, can be increased with the same chip size. The mirror needn't become larger to achieve more pixels *(Fig. 2)*.

LBS and MEMS enable a level of miniaturization that allows for more compact light engines, which can fit into smaller wearables without additional illumination or projection optics. LBS is an additive technology—the lasers aren't switched on for a dark image, which means a more efficient energy output. This efficiency is a key enabler for longer operating times.

Furthermore, LBS generates enough brightness for outdoor use of the glasses with very low power consumption.

MEMS-Based Laser Beam Scanning for Optical Apps

Microelectromechanical systems are used in a wide variety of applications, ranging from inkjet printers (using piezoelectrics for depositing ink on paper) to smartphones (e.g., MEMS microphones or accelerometers) to cars or airplanes (e.g., for airbag deployment, electronic stability control, or an airplane's autopilot).

In principle, MEMS incorporate all of the technologies and techniques needed to manufacture integrated electronic circuits. They use the same substrate—silicon—but as a mechanical instead of an electronic material. This enables components to move and have suspension; hence, MEMS structures can be used as sensors and actuators.

One main characteristic of MEMS for optical applications is the synchronization of their mechanical movement with a laser source. MEMS mirrors can be used in LBS systems to deflect laser beams and produce images. Three laser beams—red, green, and blue for the full color spectrum—get collimated and combined through lenses or beam combiners. The combined beam hits the mirror, the mirror scans back and forth (horizontally and vertically), and gives rise to an image.

In the case of AR glasses, this light is guided through an optical combiner component in the glasses, a waveguide. The waveguide displays the virtual image to the human eye, overlaying it on top of the real-world scenery.

2. The tiny OQmented LBS display engine generates 2 to 3 million nits for bright projections even in direct sunlight.

Depending on which type of waveguide is used, reflective vs. diffractive vs. holographic, there are tradeoffs between eye-box size and efficiency (eye glow), operating time, and heat development. This article concentrates on the display engine and will not discuss solely waveguide-related issues. The integration of the optical combiner with MEMS-based LBS solutions does require more research and development because of the focus on panel-based approaches.

LBS systems traditionally involve two oscillating mirrors on two single axes of two separate chips that need to be accurately aligned. However, the solution with both axes implemented on a single chip lowers the overall need for alignment of the optical system.

The one-chip solution requires a highly sophisticated MEMS design and manufacturing process to avoid dynamic deformation of the mirror plate. Typical scanning frequencies are in the range of 35 to 40 kHz, which involves rather high inertial forces acting on the mirror plate.

Benefits of MEMS LBS

The biggest benefit vs. the two-chip solution is a significant reduction of the system's size. There are optical advantages, too. Operating the single 2D mirror with two resonant axes at high frequencies results in a very particular scan pattern (Lissajous as opposed to raster scanning), allowing for much smoother motion rendering, faster image build-up, as well as greatly reduced artifacts in the 3D perception of fast-moving objects.

Encapsulating the mirror in a miniature vacuum ensures long-term reliability. Furthermore, it reduces damping or friction losses, resulting in increased achievable oscillation amplitude and optical resolution that in turn leads to lower power consumption and better optical performance.

There are many overall advantages of this solution. MEMS connote mass producibility and low manufacturing costs. MEMS-based LBS display engines don't need additional illumination or projection optics, which leads to a lightweight engine that's not even the size of a sugar cube.

Furthermore, the MEMS mirror and driver can be designed to consume less than 10 mW, ensuring minimal heat generation and enabling long operating times while guaranteeing the mirror moves very fast and with a very high FOV. And MEMS mirrors developed for this particular application can support a FOV of up to 110 degrees diagonally, enabling a 4K display.

The LBS system only produces light where it's needed, resulting in extremely high contrast. Plus, there's no energy waste due to absorption or subtraction. Certain algorithms and video electronics synchronize the intensity modulation of the red, green, and blue laser diodes according to the instantaneous position of the deflected laser beam. This generates a high-resolution, high-contrast, and high-brightness image, pixel by pixel. A safety shutdown and adjusted laser power ensure eye safety at all times.

With a display brightness of 2 to 3 million nits, this system delivers enough brightness whereby it can be used outdoors. For comparison, the sun at noon is rated at 1.6 billion nits and you need at least 3,000 nits to the eye for outdoor use of a display. For a diffractive waveguide to deliver these 3,000 nits, you need an estimated 2 to 3 million nits from the display.

Conclusion

Laser beam scanning shows considerable advantages over the OLED, microLED, LCoS, and DLP panel-based approaches in terms of achievable engine form factor and weight, energy efficiency, brightness, and contrast. This makes MEMS-based LBS display engines key to enabling stylish, lightweight, affordable, and powerful consumer AR glasses.

The technology provides high-quality projections of text and images with a large field of view, making it suitable for different types of AR spectacles, 3D binocular glasses, or 2D monocular smartglasses. It's the only technology delivering enough brightness to enable outdoor use of these glasses.

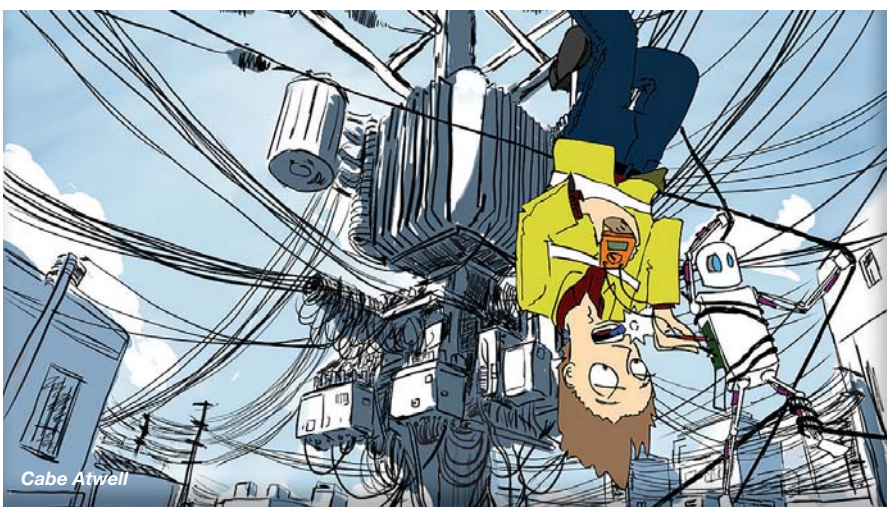
MEMS-based LBS display engines offer reliability and mass producibility. They will likely be adopted for different products beyond consumer wearables, too, including automotive applications like head-up displays, or advertising panels. Another use case is 3D scanning of the environment, either in 3D cameras or 3D sensors for MR/AR glasses.

Augmented-reality glasses through which you can see your real, actual surroundings and digital content at the same time, indoors or outdoors, hassle-free, are possible with MEMS-based LBS. ed

CABE ATWELL | Technology Editor

Celebrating Field Engineers: The Unsung Heroes of Innovation

Field engineers help implement, deploy, and maintain technology in the field, driving innovation in areas primarily unseen.



THE WORLD DOESN'T FIX ITSELF. Doesn't set itself up. It hardly ever changes—not until a field engineer shows up. Day, night, cold, or hot, these unsung heroes of engineering will answer the call not just because they get paid, but because they love the job. What's not to love. While most engineers hardly leave their offices, field engineers rarely spend any time in one.

They're the individuals who bridge the gap between theory and reality, ensuring that technologies are seamlessly integrated into our daily lives. It's with this that we delve into the narrative of celebrating field engineers and unravel the pivotal role they play in the ever-changing world of innovation and progress.

Field engineers are the problem solvers, the troubleshooters, and the architects of the seemingly impossible. They're the ones outside of the limelight who ensure those technologies keep functioning behind the scenes.

Adaptable to All Environments

One of the defining characteristics of field engineers is their adaptability, seamlessly traversing through diverse environments to address challenges. Climbing cell towers to optimize network signals or navigating through machinery to conduct maintenance—they overcome every obstacle.

You can find them in the energy industry, from remote ocean oil platforms to nuclear power plants, working to keep the lights on and maintaining power to critical infrastructure such as hospitals and care centers. Other field engineers will in turn make sure the equipment in those hospitals remains up and running, like MRI machines and remote robotic surgery systems, to name a few.

Manufacturing, with its vast machinery and automated systems, relies on field engineers to keep those wheels of industry turning. They're the first responders to answer breakdowns, keeping downtime minimal and production lines humming. Implementing and maintaining Industry 4.0 technologies and beyond, setting up IoT-enabled devices and smart manufacturing systems, they're pivotal in shaping the future of production.

A Celebration on Multiple Fronts

The celebration of field engineers isn't just about acknowledging their technical abilities, but also about recognizing their adaptability in the face of challenges. It's not uncommon to find them working in adverse conditions, extreme weather, hazardous environments, and challenging terrain. They're the ones that scale heights and descend into depths to make sure that technology runs flawlessly. It's also a celebration of their commitment to the job, their ability to improvise solutions, and their dedication to solving complex problems on the go.

As we celebrate field engineers, it's important to highlight the symbiotic relationship they share with technological innovation, too. While being the architects of those technologies, they're also the eyes and ears on the ground, providing invaluable feedback for continuous improvements. Their experience in the field often leads to new enhancements pushing industry forward. Plus, they're one of the few in the sciences that will never be replaced by artificial intelligence.

So, here's to you field engineers, the unsung heroes dedicated to keeping the lights on and propelling new technologies that make life better for everyone. Thank you for making it all work. ED

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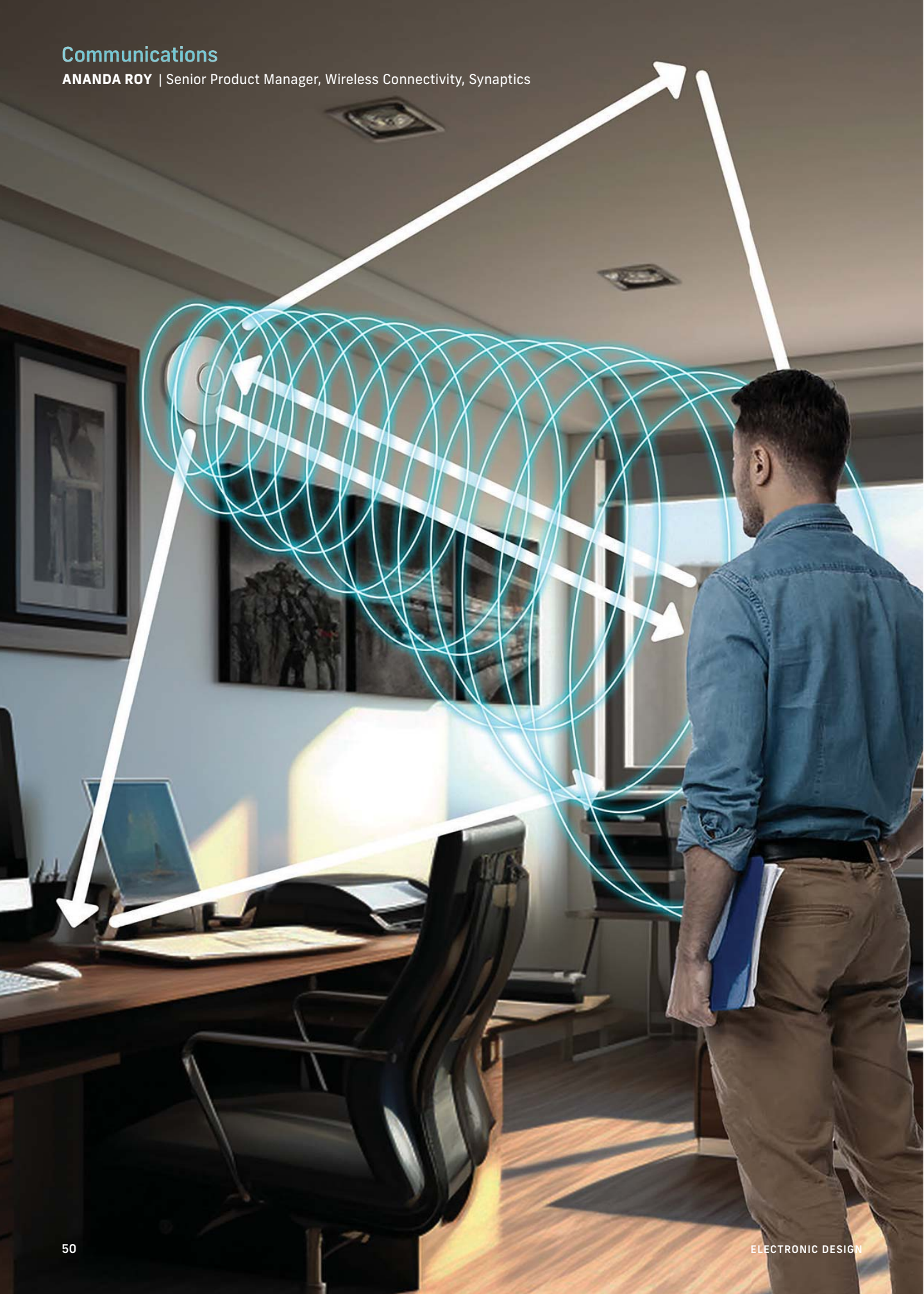


Wi-Fi Sensing:
A Crucial Capability Assisted by Edge AI Processing

Today's connected society is immersed in radio waves. Literally a "sea of RF" and Wi-Fi sensing, enabled by advanced processing techniques, is emerging as a critical feature for connected IoT devices.

WI-FI SENSING IS becoming the latest big idea in applications ranging from smart-home automation and home security to industrial security to child safety in cars. However, these applications are all served today by a variety of sensor technologies, including passive infrared detectors, ultrawideband (UWB) radios, ultrasonic sensors, smart cameras, and even radar.

So, what's all this buzz about Wi-Fi sensing? Why is it important, how does it work, and—especially—what does it mean for the Internet of Things (IoT) and edge computing?

The Sea of RF

The concept of Wi-Fi sensing begins with a realization about the world we have built. Virtually every enclosed space is bathed in Wi-Fi signals. Our homes, for instance, are soaking in Wi-Fi transmissions as Wi-Fi routers and gateways exchange packets with smartphones, notebook computers, TVs, thermostats, and doorbells *(Fig. 1)*.

The secret behind Wi-Fi sensing is that while all of those radio transmissions are flying about, each receiver is keeping a detailed record of the signal characteristics it's receiving. At a coarse level, this is just a measure of signal strength, recorded as the received signal strength indicator (RSSI).

In early Wi-Fi systems, RSSI could tell the receiver whether to request the transmitter to turn up the transmit power for better signal strength or turn it down to save power. The receiver interface could report the RSSI data to the receiving device—be it a smartphone, notebook, or another device—and software running on the device could make some inferences about what was going on in the room. If the RSSI value suddenly dropped, you could infer that some object had passed between the hub and the receiver.

Boosting Wi-Fi with MIMO

Today's Wi-Fi, carrying vastly more data, is far more complex than those early interfaces. Now, most Wi-Fi routers and gateways and the devices that connect to them usually have two or more independent antennas each.

These multiple antennas can be used to form beams, directing the energy for a particular set of frequencies in a particular direction or increasing the sensitivity of the receiver antennas in a particular direction. This is called multiple-input, multiple-output (MIMO) beamforming. The Wi-Fi interfaces use multiple frequencies—subcarriers—simultaneously to exploit the available bandwidth as fully as possible.

Managing all of these variables—the amplitudes, phases, frequency response, and signal-to-noise ratio (SNR) of potentially dozens of separate signals—to most efficiently utilize the bandwidth in the physical space requires a lot more information than just RSSI. The collected dataset aggregating all of this information is called the channel state information (CSI). Technically, it's a matrix of complex numbers, updated every time a subcarrier is activated.

With some computation, the CSI can inform the transmitter and receiver how to best aim their antenna patterns as well as allocate subcarriers for the best bandwidth. But there's more that can be done using CSI.

Those subcarrier signals will not only head for the receiver antennas, but they will get blocked by intervening objects and bounce off reflecting surfaces, creating multiple beams that will arrive at the receiver at different times and from different directions. The signal amplitudes and phases the receiver gets on its multiple antennas will reflect what's going on in the paths taken by the signals between transmitter and receiver. Therefore, the software can mine the CSI data to create a rather detailed picture of the world around the receiver.

A significant and abrupt change in CSI would indicate that something has physically changed in the ambient environment. This could be a sudden motion,

1. Today's connected homes and offices take advantage of nearly ubiquitous Wi-Fi to improve communications and boost productivity.
Images courtesy of Synaptics

a human falling, or even something as subtle as a heartbeat.

The CSI can also record relatively small phase shifts in the received signals—small enough to detect the shift in reflections from moving objects. This all adds up to a fair amount of information about the presence, location, and motion of objects in the area.

Inferring the World

So what?

This ability to make inferences about the environment may seem a rather abstract benefit. However, researchers exploring the richness of CSI data have demonstrated a number of practical uses. CSI processing can infer the presence or motion of people in an area. This information can be applied to safety and security, or simply for smart-home convenience features.

One important use case is preventing parents from accidentally leaving small children in the back seats of cars. But further processing can yield more information, such as the location of objects near the receiver, their motion, and even subtle movements like finger gestures or respiration. Applications abound in the realms of health, safety, and convenience.

How It Works

Given enough budget, all of these examples could be done with existing sensor technology—ultrasonic, UWB, radar, or even LiDAR. But Wi-Fi sensing has an enormous advantage because it doesn't require additional hardware beyond a modern Wi-Fi device. And Wi-Fi is nearly ubiquitous today. It's included in almost all electronic devices deployed in the smart home. All of the sensing is done by importing and analyzing the CSI data from the Wi-Fi system-on-chip (SoC) in a connected device.

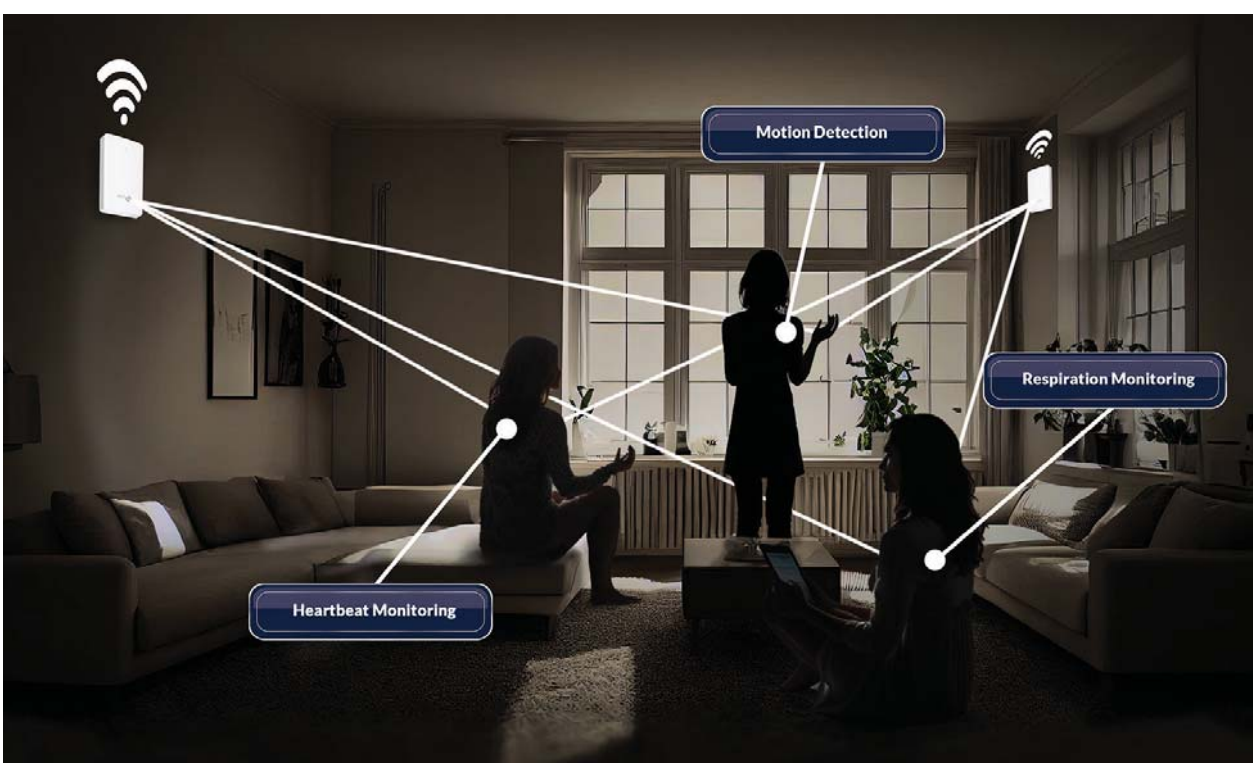
It's the analysis that can be challenging. First, the data must be filtered to remove noise—random variations in channel state—and to extract the amplitude and/or phase data for each subcarrier. This can be accomplished with ordinary digital-signal-processing (DSP) algorithms.

Then, the analysis must identify patterns in the data that might indicate human presence, objects, or events. This may be done with relatively simple statistical calculations or require quite elaborate pattern recognition, depending on what designers want to identify. Finally, the extracted features must be interpreted to infer objects, classify them, and identify motion or gesture *(Fig. 2)*.

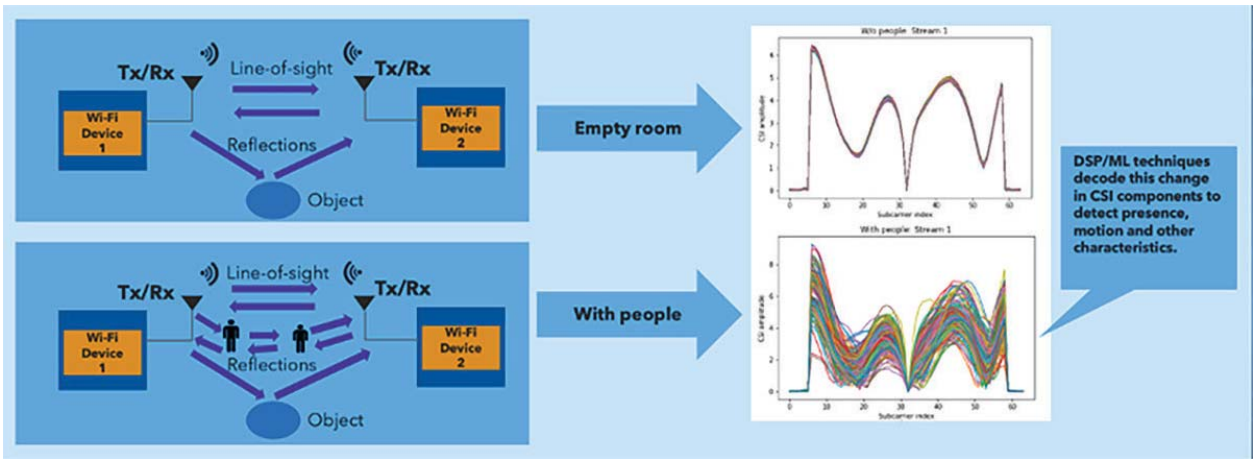
Recent advances in artificial intelligence (AI) and machine learning (ML) can simplify the data processing and inferencing from CSI. The marriage of advanced Wi-Fi sensing algorithms grounded on CSI and ML using neural networks has the potential to yield excellent results.

Wi-Fi Sensing and the IoT

But deep-learning networks, with their robust appetite for computing and memory resources, raise an important issue.



2. The connected living room is awash with Wi-Fi signals that can be used to sense human presence, motion, and gestures, as well as finer-resolution characteristics such as heartbeat and respiration.



3. Wi-Fi sensing analyzes Wi-Fi CSI data to detect human presence and motion.

For the IoT, the ground rules are minimum cost and, since many IoT devices are battery-powered, minimal energy. And many applications need results at once, not after a night of cloud computing.

Identifying changes in the environment locally is essential to reduce latency, minimize bandwidth usage, and keep power to a minimum. Doing so also allows the host device to remain in quiescent mode most of the time, just doing enough processing to detect a shift in the environment. The device can then use a higher-order sensor, such as a camera, to perform more analysis.

If the IoT device has a modern Wi-Fi interface, Wi-Fi sensing can be a solution. The sensing process requires no additional power or hardware beyond what's already consumed by the Wi-Fi interface. And monitoring can be done with a low-level software routine running in near-zero-power mode—sleeping with one eye open.

Consider, for example, a wireless smart security camera. To capture even stop-frame images every second or so and run them through vision-processing algorithms would be a significant drain on a battery.

However, equipped with Wi-Fi sensing, the camera could remain asleep until the Wi-Fi sensing software—running in low-power mode—detected a shift in the CSI data. Then, the device could power up its CPU and analyze the CSI data more thoroughly to determine whether the situation merited turning on the security camera and streaming video to the vision-processing hardware.

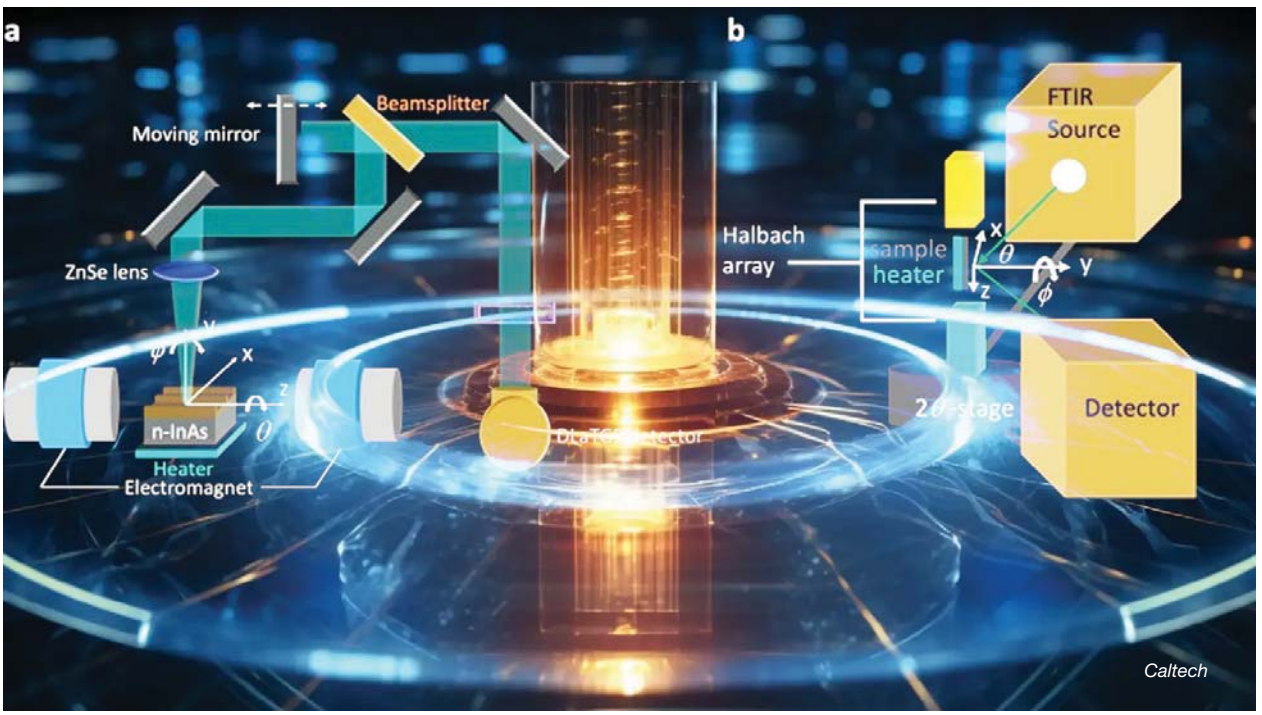
If the IoT device has a modern Wi-Fi interface, Wi-Fi sensing can be a solution. The sensing process requires no additional power or hardware beyond what's already consumed by the Wi-Fi interface.

Or consider a fall detector in a home safety system. Using ambient Wi-Fi signals—even the beacon if there's no other activity—the detector could monitor the CSI data for the arrival of a person using a low-power computing mode. When someone arrives, the system could activate a low-power neural-network inference engine and begin monitoring the CSI data for a pattern that would imply a fall.

The key to these Wi-Fi sensing use cases is to process the CSI data locally, with an absolute minimum energy expenditure for the situation *(Fig. 3)*. This requires access to robust Wi-Fi SoCs, energy-efficient DSP cores, and—with the increasing use of ML—access to low-energy neural-network accelerator hardware. It also requires extensive experience with power-management techniques. And most importantly, it depends on a synergistic engineering relationship between elite Wi-Fi and AI/ML engineering teams.

Synaptics, for instance, is uniquely placed for this opportunity with its portfolio of products, including both Wi-Fi connectivity and AI/ML processors. The company also has leading scientists and engineers working in these areas, as well as in developing RF hardware, PHY, baseband, and MAC layer software embedded in all Synaptics wireless SoCs. ed

BILL SCHWEBER | Contributing Editor



Researchers Poke a Hole in Kirchhoff's "Other" Law—or Maybe Not

Kirchhoff's thermal law relating absorptive and emissive efficiencies has stood for over 150 years, but it may have some violations under specific circumstances.

ENGINEERS OF ALL disciplines and especially electrical engineers are familiar with Kirchhoff's voltage and current laws (promulgated in 1847). They quantify how voltage varies around a loop in a circuit and how current flows through a circuit. Though obvious to us, they were critical and insightful revelations at the time.

Kirchhoff's Voltage Law (KVL) states that "the sum of the voltage differences around any closed loop in a circuit must be zero" (conservation of energy) while his Current Law (KCL) says that "the sum of the voltage differences around any closed loop in a circuit must be zero" (conservation of charge). The two laws are used extensively and almost subconsciously, as they're at the foundation of system and circuit design and analysis.

But Gustav Kirchhoff did not stop with these laws. This German physicist also contributed to the fundamental understanding of spectroscopy as well as blackbody energy radiation and absorption. The latter is a concept to which he contributed (he coined the term "black body"), and it was critical to the development of quantum theory in the early 1900s.

He developed his thermal law in 1860, which states absorptive and emissive efficiencies are equal at each wavelength and angle of incidence (more explanations of Kirchhoff's thermal law can be found in the References section below). It's roughly analogous to the reciprocity principle for antennas.

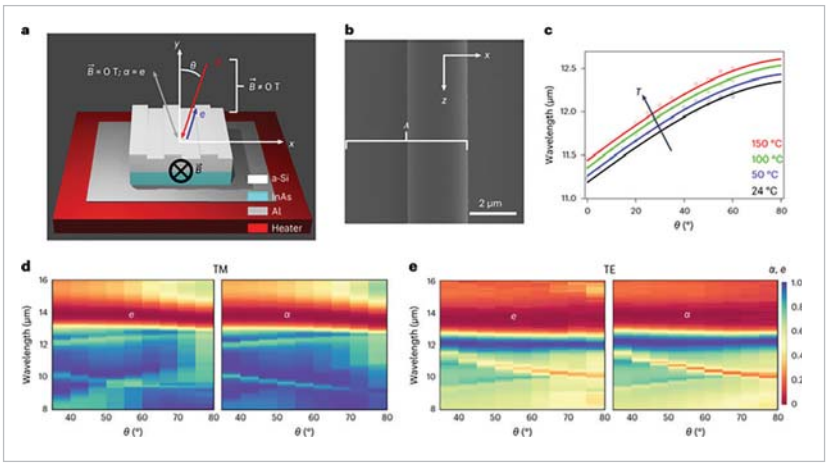
Decoupling Absorbed and Emitted Efficiency

Now, a team based at the California Institute of Technology (Caltech) has devised a device that they say breaks

this normally tight relationship between the absorbed and emitted efficiencies of an object. The invention may also have important implications for sustainable energy-harvesting systems.

Why try to decouple the two? For example, if an energy-harvesting object such as a photovoltaic source (solar panel) is re-emitting some of its absorbed energy back toward the energy source (the Sun) as heat, that energy is lost to other uses. In theory, if the photovoltaic source—or other energy-harvesting object—were to re-emit absorbed radiation away from the source and toward yet another energy-harvesting object, the system could reach higher energy-conversion efficiencies.

The Caltech study shows that it's possible to "break" the equality of Kirchhoff's law of thermal radiation with a device placed in a moderate magnetic field. The device itself combines a material featuring a strong magnetic-field response with a patterned structure that enhances absorption and emission in infrared wavelengths *(Fig. 1)*.



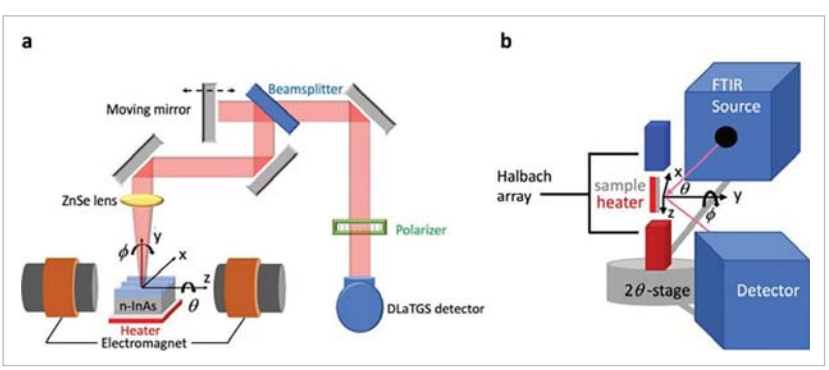
1. Schematic of magnetically tunable emission and absorption of GMR structure coupled to n-InAs and comparison of zero-field absorptivity and emissivity: Schematic of the GMR structure on InAs—the GMR structure has a grating periodicity Λ of 5.50 μm, groove depth of 0.50 μm and slab depth of 1.55 μm (a). In the case of no applied magnetic field, the absorptivity and emissivity channels are equal (left side, grey arrow). When a transverse magnetic field is applied along the z direction, the absorptivity and emissivity (red and blue arrows, respectively) are tuned away from being equal in the same channel to being equal in opposite channels. The grating periodicity Λ is confirmed with scanning electron microscopy images (b). Experimental data (points) of the +first-order guided-mode branch through absorptivity (24 °C, black) and emissivity (50, 100 and 150 °C; blue, green and red, respectively) measurements; the curves represent theoretical calculations (c). The red shift in the GMR for a given θ is a consequence of shifts in the refractive indices of a-Si and n-InAs as a function of temperature. TM-polarized (d) and TE-polarized (e) emissivity and absorptivity measurements taken at 100°C (left and right, respectively), showing the guided-mode dispersions. *Images courtesy of Caltech*

Measuring the Emissivity-Absorptivity Inequality

The situation is complicated. Their experimental measurement of an inequality between the thermal emissivity and absorptivity for a photonic structure supports a transverse magnetic guided-mode resonance (dubbed GMR, but not to be confused with giant magnetoresistance) coupled to a magneto-optic material.

This inequality occurs under the application of an in-plane magnetic field that changed the permittivity of the magneto-optic indium arsenide (InAs) to a non-diagonal tensor. The non-diagonal permittivity tensor resulted in an antisymmetric angular relationship in which the magnetic tuning of stronger thermal emission for a given angle of incidence correlates to stronger absorption in the opposite channel.

Using an angle-resolved thermal emission spectroscopy (ARTES) arrangement



2. For emissivity measurements, the sample is mounted on a heater at the rotation axis of a goniometer [a device that measures an angle or permits the rotation of an object to a definite position], centered between the pole pieces of an electromagnet (a). The goniometer allows for rotation of the sample around the z-axis and probes the outgoing radiation at an angle θ. The sample emission is collected through a zinc-selenide (ZnSe) lens and sent through an external port into an Fourier transform infrared (FTIR) spectrometer. A polarizer is placed in front of the detector to resolve the TM and TE emission. The absorptivity measurement system uses an FTIR source and detector mounted on a 2-θ rotation stage (b). Instead of an electromagnet, a Halbach array of permanent magnets [a special arrangement of permanent magnets that augments the magnetic field on one side of the array while canceling the field to near zero on the other side] to apply the magnetic field. The sample is still heated to the same temperatures as in the emissivity measurements so that there can be a direct comparison of the absorptivity and emissivity as defined by Kirchhoff's Law.

(Fig. 2), they observed that the Kirchhoff-violating behavior was most pronounced where the GMR and the InAs' Brewster-mode spectrally overlap (12.8–12.5 μm) over an angular range of 60 to 80 degrees *(Fig. 3)*. [Note: Brewster's angle (also known as the polarization angle) is an angle of incidence at which light with a particular polarization is perfectly transmitted through a transparent dielectric surface, with no reflection.]

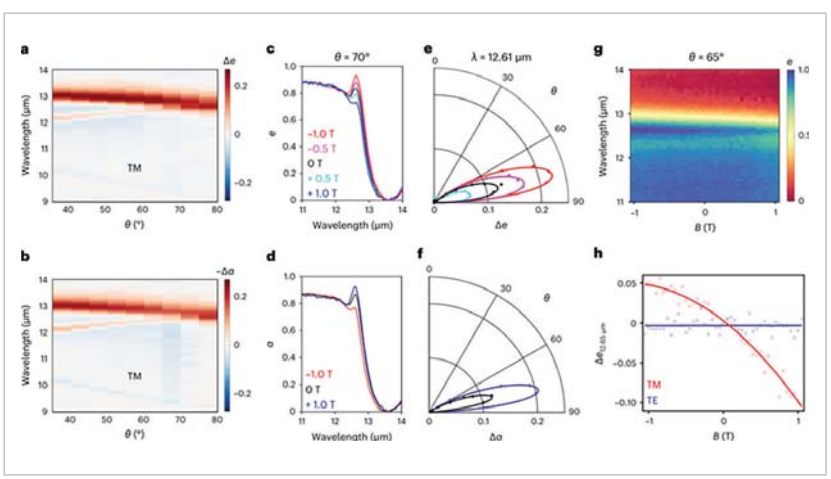
But wait…there's more to this story. The work was reported in their paper "Direct observation of the violation of Kirchhoff's law of thermal radiation" published in *Nature Photonics*, along with a Supplementary Information file. However, soon after it was published, two authors from academia and commercial interests posted a one-page rebuttal "Why Kirchhoff's Law of Thermal Radiation Has Not Been Violated" at OSF/Center for Open Science site. Scientific disputes of this type aren't unusual (it happened with quantum physics, relativity, and even heliocentricity), but they're still noteworthy.

What's the Takeaway?

My take on this claim by these researchers is multifaceted. I certainly don't have the advanced physics background needed to fully assess their claims of the Caltech researchers. I do know that when materials are subject to extreme conditions—here, a magnetic field—conventional principles may bend and break. Think of the effects of ultra-low temperatures (cryogenics) or ultra-high ones (plasma states) on materials.

In addition, this linking of the apparent violations of Kirchhoff's thermal law to solar panels and photovoltaic efficiency has some aspect of using what marketing folks call "borrowed interest" to gain attention.

It seems that nearly every research project I read about these days—and I read summaries of lots of them—claims some connection, however tenuous, with climate change, CO_2 emissions, sustainability. carbon footprint, and similar themes. Perhaps the reason for all of this keyword connectivity is perhaps that's where the bulk of the all-important grant funding and public-relations attention is focused these days. ed



3. Violation of Kirchhoff's law in absorptivity and emissivity measurements: Change in the absolute emissivity and absorptivity as the applied magnetic field is switched from +1.0 to −1.0 T: Δe = e−1.0 T − e1.0 T and Δα = α−1.0 T − α1.0 T (a,b). The magnetic field has an opposite effect for absorptivity and emissivity. Note that Δe is plotted in (a) and −Δα in (b). Shown is spectral emissivity (c) and absorptivity (d) at θ = 70° for varying magnetic fields. Directivity plots demonstrate the effect of the magnetic field on the resonant directional emissivity (e) and absorptivity (f) coupling through the GMR structure. The least resonant magnetic field is subtracted for both emissivity and absorptivity: Δe = e − e1.0 T and Δα = α − α−1.0 T. Although the directionality is imposed by the GMR structure and unchanged by the magnetic field, the outcoupling intensity is modulated by InAs. Equal and opposite tuning is observed for emissivity and absorptivity. Here, measured emissivity is a function of wavelength and magnetic field for θ = 65° (g). The emissivity resonance is shown as the dark-blue region near λ = 12.7 μm for large negative magnetic fields. The resonant emission is tuned to a narrower linewidth and smaller amplitude with increasing magnetic field. This is a consequence of the InAs emission edge (yellow line starting at λ = 13 μm for −1 T) shifting to shorter wavelengths for increasing magnetic field. Also depicted is the change in emissivity near the resonance wavelength (λ = 12.65 μm) for θ = 65° as a function of magnetic field (h). The TE-polarized emission shows no magnetic-field dependence, whereas the TM emissivity change is fit quadratically. This captures the beginning of the saturation effect for large negative magnetic fields. All of the data was taken with the sample heated to 100°C.

REFERENCES

SPIE, "Kirchhoff's Law and Emissivity"
Caltech, "Radiative Transfer"
Wikipedia, "Kirchhoff's law of thermal radiation"

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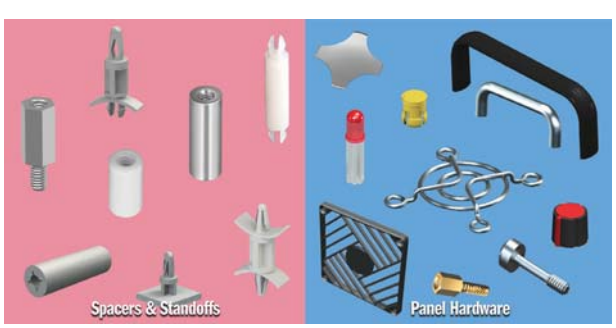

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