ideas for design

Build Your Own RC-Programmable, Wide-Bandwidth Bandpass-Filter Comm Apps

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MANY COMMUNICATIONS AND SENSOR applications require a bandpass filter with wide bandwidth. This filter typically requires precision resistors and capacitors to obtain an accurate filter position and response.

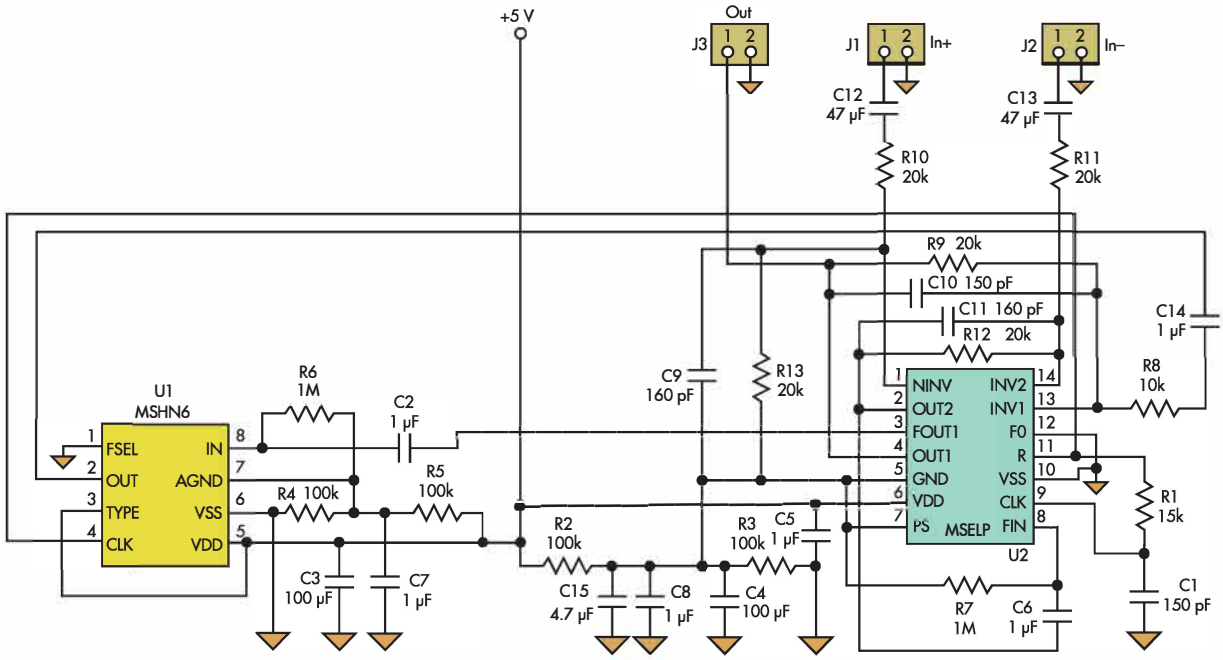
Switched-capacitor filters eliminate the need for precision components, but require a clock from a microcontroller to set the center frequency. With the limited number of outputs and timers on popular low-cost microcontrollers, there may not be a clock timer or digital output to dedicate to the filter's clock function.

The solution is to use a filter with a built-in clock oscillator, such as the MSELP fifth-order elliptic low-pass filter from Mixed Signal Integration. Similar ICs like the higher-current (5 mA) LMF60 are available from Texas Instruments, under the legacy National Semiconductor designation.

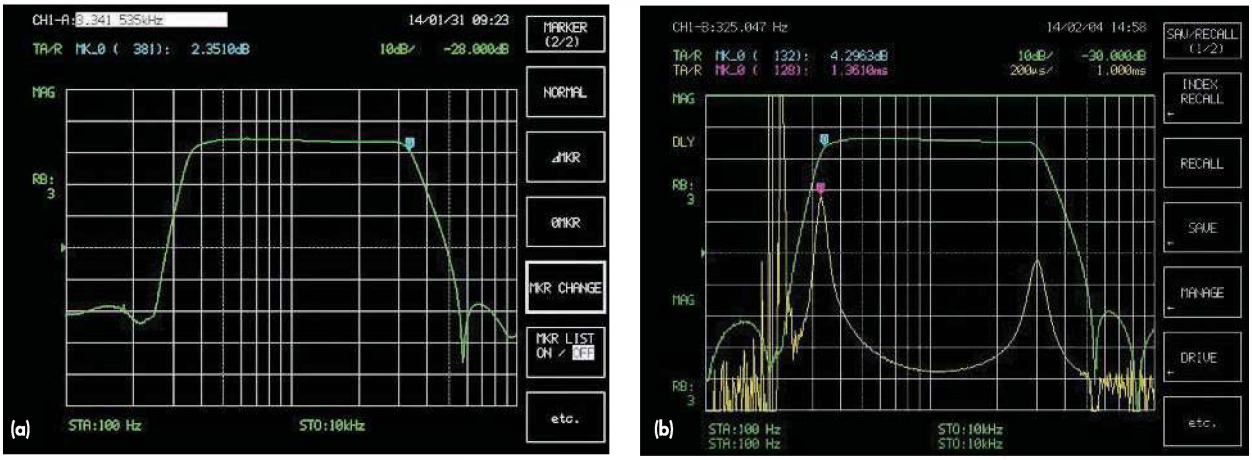
With the selectable 50:1/100:1 clock-to-corner-ratio pin and two uncommitted op amps, the clock-oscillator IC provides both an anti-aliasing filter and a reconstruction filter. Furthermore, the clock output of the MSELP can drive another switched-capacitor high-pass filter. Armed with a clock-to-corner frequency ratio of 1000:1, the MSHN6 sixth-pole high-pass/notch filter puts a decade between the corners of the bandpass filters.

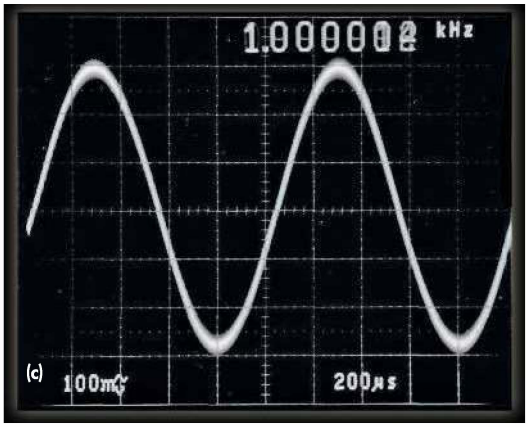
The circuit of Figure 1 is a 330-Hz to 3.3-kHz bandpass filter for Family Radio Service (FRS) radio or telephony. FRS radios are low-power, low-cost, point-to-point units providing direct voice links between users without the need for an intermediate basestation or control node. They are especially useful in remote areas that lack cell-signal coverage or cell towers.

The corner of the reconstruction filter and the anti-aliasing filter is set for approximately 50 kHz. The design uses both anti-aliasing filters and reconstruction filters. The MSELP's op-amp input provides both positive and negative inputs to the



1. This circuit provides a wideband bandpass filter optimized for FRS applications, with a 10:1 ratio in its corner frequencies.





2. The network analyzer output shows the filter's 3-dB points, roll-off, and attenuation through the anti-aliasing filter, two switched-capacitor filters, and the reconstruction filter (a); the amplitude (green trace) and group delay response (yellow trace) (b); and the reconstructed time-domain filter output at 1 kHz (c).

filter input. The MSHN6 and MSELP work down to 2.7 V dc. The circuit draws less than 1 mA. R1 and C1 set the oscillator frequency. With a 5-V supply, the frequency is:

$$F_{Clock} = 1/(1.42 \times R \times C)$$

For a 312-kHz clock, R1 equals 15 kΩ and C1 is 150 pF (3.12-kHz low-pass and 312-Hz high-pass corners).

Figure 2a is a screen capture of the network analyzer showing the complete response through the anti-aliasing filter, two switched-capacitor filters, and the reconstruction filter. Figure 2b shows the amplitude and group delay response. Note that due to its group delay response, this filter would not be suitable for telecom use, but it is a fit for radio and telephony applications. Figure 2c is the filter output at 1 kHz in the time domain. Clock feed-through is minimal, as seen at the reconstruction filter output.

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Accurately Determine Steady-State Output for a Periodically Driven RC Filter

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A RECENT IDEA FOR Design showed a graphical technique for determining the output of an RC filter driven by a pulse-width modulation (PWM) pulse train.[1] It requires the manipulation of infinite series with a limit. Therefore, it does not yield steady-state results with confidence.

A better approach uses the concept of continuity of states and steady-state "wrap-around" to eliminate this shortcoming, since current and voltage values in a real circuit cannot change instantaneously. Current and voltage are variables with continuous values in time, from moment to moment. For a circuit structure that is switched periodically among several states repeatedly, the end state of one structure serves as the starting state of the next.

Using the same RC filter, periodic-input pulse train, and designations as the referenced Idea for Design, Equation 1 shows the filter output when the driving source V_A is non-zero:

$$v_a(t) = [V_{0a}e^{-\frac{t}{\tau}} + V_A(1-e^{-\frac{t}{\tau}})][u(t)-u(t-D\cdot T)] \quad (1)$$

When the driving source drops to zero, the output will be given by:

$$v_b(t) = V_{0b}e^{-\frac{t-DT}{\tau}}[u(t-D\cdot T)-u(t-T)] \quad (2)$$

In Equation 1 and Equation 2, the two starting conditions V_{0a} and V_{0b} are yet to be determined. A gating function with unit steps is also employed. At steady state and at the switching boundaries, t = DT and t = T; therefore Equations 3a and 3b must hold:

$$V_{0a}e^{-\frac{DT}{\tau}} + V_A(1-e^{-\frac{DT}{\tau}}) = V_{ob} \quad (3a)$$

$$V_{0b}e^{-\frac{(1-D)T}{\tau}} = V_{oa} \quad (3b)$$

This indicates that the end state of active duration with non-zero driving source must act as the starting state, V_{0b}, of the inactive duration with zero drive. Similarly, the end state of the inactive interval must return to the same starting state, V_{0a}, of the active segment. Using these facts and Equations 3a and 3b, it results in:

$$V_{0a} = \frac{V_A(1-e^{-\frac{DT}{\tau}})e^{-\frac{(1-D)T}{\tau}}}{1-e^{-\frac{T}{\tau}}} \quad (4a)$$

$$V_{0b} = \frac{V_A(1-e^{-\frac{DT}{\tau}})}{1-e^{-\frac{T}{\tau}}} \quad (4b)$$

In other words, cyclic starting states are actually known functions of driving source V_A, duty cycle D, pulse period T, and time constant RC = τ. The steady-state output in one cycle can be written as:

$$v_1(t) = [V_{0a}(V_A, D, T, \tau)e^{-\frac{t}{\tau}} + V_A(1-e^{-\frac{t}{\tau}})][u(t)-u(t-D\cdot T)] - [V_{0b}(V_A, D, T, \tau)e^{-\frac{t-DT}{\tau}}][u(t-D\cdot T)-u(t-T)] \quad (5)$$

where the multiple-cycle output is given by:

$$v_o(t) = \sum_{n=0}^{m} v_1(t-n\cdot T) \quad (6)$$

Using the example of the previous Idea for Design, with V_A = 1, D = 0.6, T = 20 µs, and τ = 50T, produces the steady-state results of the figure. The output dc level *(Equation 7)* is obtained by taking the average of Equation 5:

$$V_{DC} = \frac{1}{T}\int_0^T v_1(t)dt = 0.599999632129 \quad (7)$$

and confirms Equation 16 of the previous approach.

The approach presented here gives the true steady-state output in compact, closed form with a high degree of confidence. The technique can be extended to a number of other second- and higher-order circuits that are switched periodically among multiple states.[2, 3]

REFERENCES
1. "Graphically Determine The Output Signal Level Of An RC Filter," ***Electronic Design***, Oct. 3, 2013.
2. ***Switch-mode Power Converters***, Keng Wu, Elsevier, 2005, ISBN 13:978-0-12-088795.
3. ***Power Rectifiers, Inverters, and Converters***, Keng Wu, Lulu.com, 2008, ISBN 978-1-4357-2023-7.

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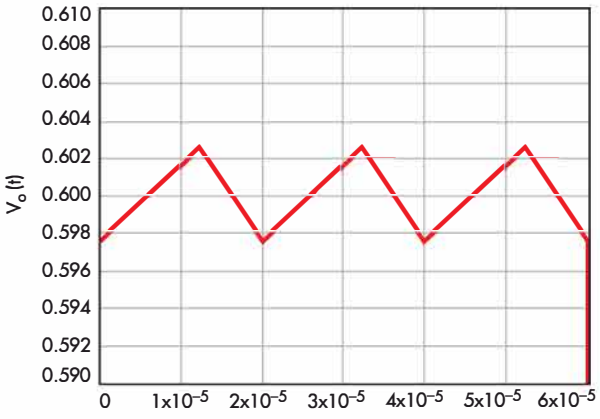

Analysis shows that the steady-state output of this RC filter, when driven by a 50-kHz, 1-V, 60% duty-cycle PWM wave, is also periodic and stays within a narrow amplitude band.