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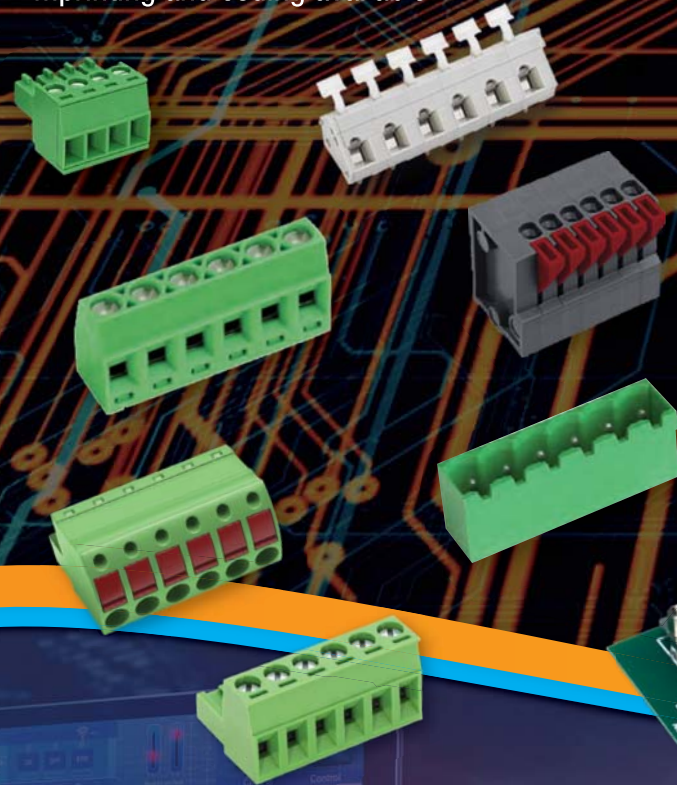
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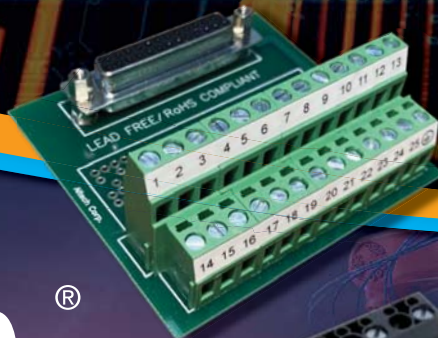
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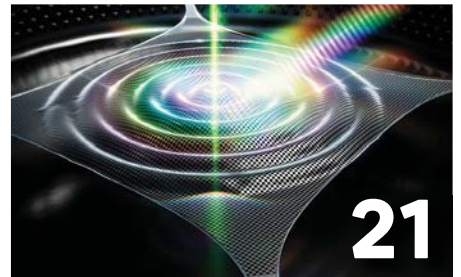
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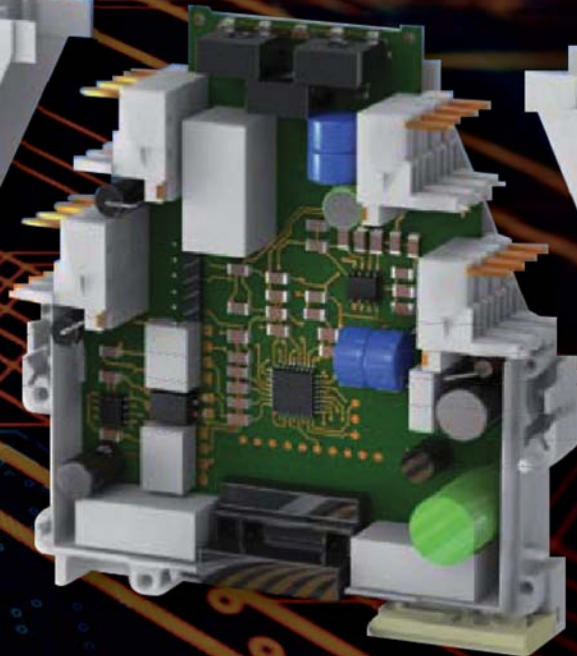
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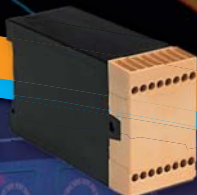
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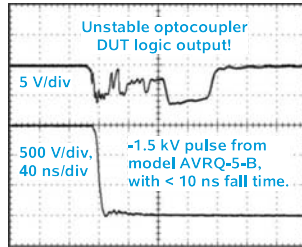
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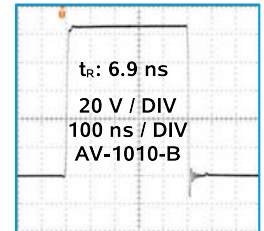
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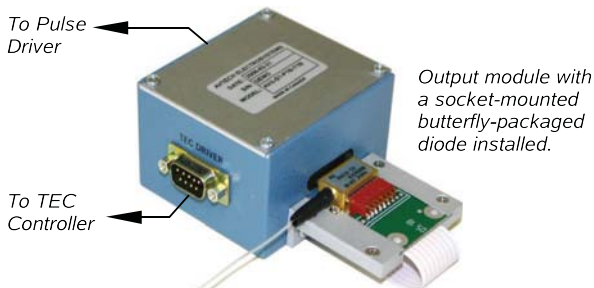
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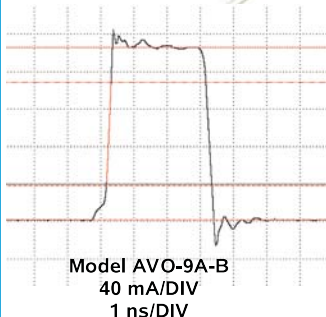
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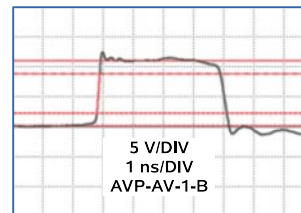
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50 V	500 ps	1 MHz	AVR-E5-B
100 V	500 ps	100 kHz	AVR-E3-B
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Editorial

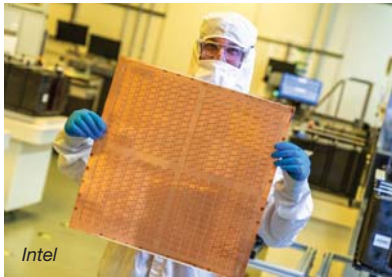
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Keeping Up with the Never-Ending Innovation Train

Electronic Design wants to make sure you don't miss a thing, be it glass substrates or chatbots.

EVEN WITH ALL OUR advanced tools from chatbots to smartphones, we still need to locate, understand, and utilize the latest technology innovations to stay ahead of the competition. These days, this isn't easy. It's simply not possible to chase down all of the options and incorporate them into a product or service. However, making the wrong choice or ignoring advances can result in falling behind or getting pushed out by the competition.

I've been writing about electronic and computer technology for decades and it's a challenge for me to keep abreast of everything that's cropping up. Having degrees and a background in electronics and computers has helped a lot. But, for example, changes in artificial intelligence (AI) from rule-based systems that I started with, to the various neural networks, and, lately, large-language-model (LLM) chatbots, are radically different.



The challenge for engineers and programmers is not just learning about what's new, but also how things go together. I recently did a video and article entitled "Through the Substrate Looking Glass" (<https://electronicdesign.com/21275763>) about Intel's use of glass substrates (see figure). This technology is important because of its relationship to chiplet-based solutions as well as supply-chain issues with currently employed substrates. It's the relationship between new technologies and methods that we try to highlight at *Electronic Design* and more broadly in our Endeavor Design and Engineering Group that includes publications like *Microwaves & RF* and *Power and Motion*.

Another example shows up in one of our sponsored webinars: "Utilizing the Best Switch Technology for Power Supplies" (<https://electronicdesign.com/21274454>). Power Integrations' Andrew Smith talks about GaN and SiC wide-bandgap technologies.

The one thing I found most interesting was the charts showing the overlap of silicon, SiC, and GaN, and the amount of overlap that exists, which means many applications can utilize two or more technologies. Trying to figure out the tradeoffs, advantages, and disadvantages are what developers need to contend with even as improvements are being made.

One can't assume existing solutions are the best either, as noted by Lee Goldberg's cover story, "New Motor Designs Help EV Makers Kick the Rare-Earth Habit" ([online at https://electronicdesign.com/21270762](https://electronicdesign.com/21270762)). This ties in with the supply chain, as rare-earth magnets have advantages for motors but don't do well if the materials are no longer available or become more expensive.

Being an engineer and programmer now is more interesting and more exciting than ever, with so many tools and devices readily available. However, keeping up with them is no easy task. **ed**

First Takeaways from Our 2023 Career & Salary Survey

Beyond coverage of key elements of your job, this year's *Electronic Design Career & Salary Survey* takes a deeper look at the impact of AI and its regulation.

WE JUST WRAPPED UP OUR group-wide salary survey and I have a few tidbits to get things started. A bunch of articles coming up will delve more into the details. Our editors will present different aspects of the results, such as continuing education, how collaboration is changing, and where we're working. An eBook containing all of the articles will be available soon.

In general, things are looking up, with many of the same concerns as last year, such as supply chain and hiring issues. The outlook remains promising, but challenges remain. The technologies impacting your designs include perennial favorites—power management, wireless networks,


and test equipment—though areas like security are becoming more important.

We asked a few questions about artificial intelligence (AI) and machine learning (ML). They're having a major impact on the tools and platforms we use regardless of whether we're designing products targeting image processing or motor control.

There's definitely a concern about AI/ML regulation (Fig. 1), but the technology is having a positive effect for those who are using it. AI/ML is also acknowledged to offer a competitive advantage in a variety of applications. That's not to say its use is pervasive because engineering and software designs address a wide array

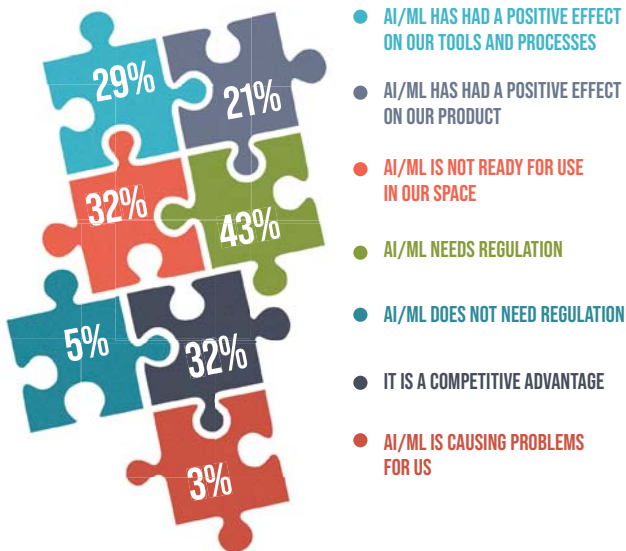
of application areas—not all need or can use the current crop of AI/ML tools or middleware.

Moreover, a sizable group still doesn't implement AI/ML anywhere, although it's creeping into search engines whether we like it or not (Fig. 2). It's also being added to our office and collaboration tools, but we tend to have more control over what's used and how we take advantage of it.

Our Annual Salary Survey page (<https://electronicdesign.com/21128128>) is where you will be able to find the in-depth articles. Thanks to all those who participated. Also let your voice be heard by leaving a comment or two once you read the articles. 

What do you think about artificial intelligence/machine learning?

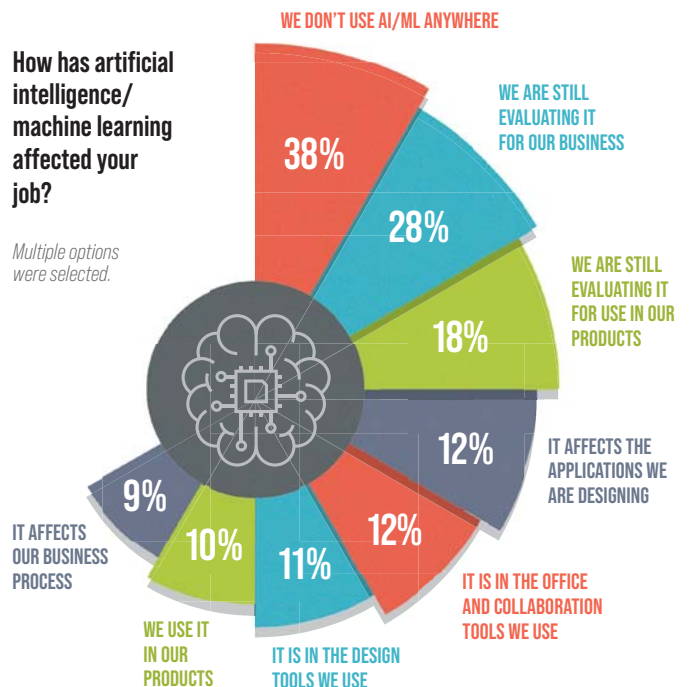
Multiple options were selected.



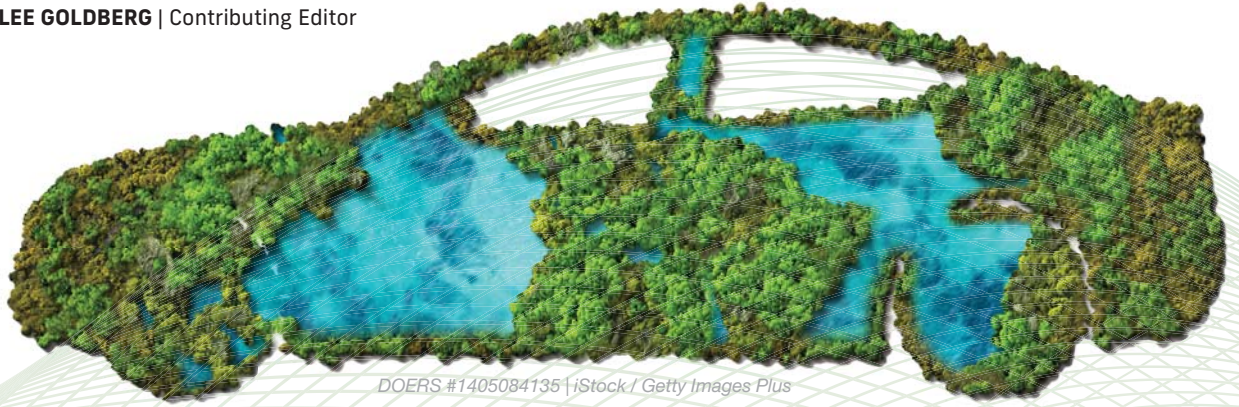
1. A significant number of people think that AI/ML isn't ready yet, but not by the majority of who responded. Still, the number of people think the tools and middleware are progressing well.

How has artificial intelligence/machine learning affected your job?

Multiple options were selected.



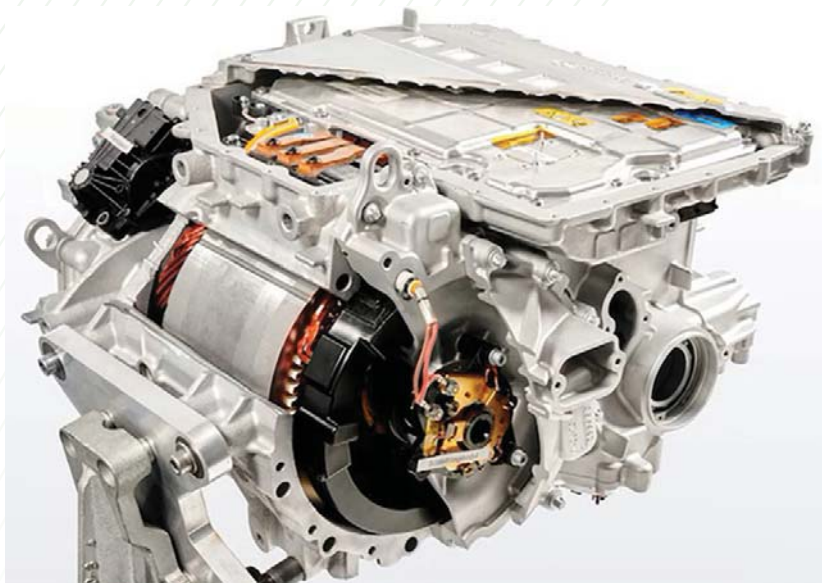
2. Most respondents either aren't using or evaluating AI/ML at this point. We'll see how this trend changes over the year.



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New Motor Designs Help EV Makers Kick the Rare-Earth Habit (Part 1)

The latest motor architectures assist in curtailing or eliminating the economic, environmental, and geopolitical costs associated with the rare-earth materials used in most electric motors.



1. BMW's 5th-generation EV motor is an example of how automakers are developing new motors that don't depend on rare-earth magnets to achieve high performance and efficiency in a compact form factor. *BMW*

AT PRESENT, ROUGHLY 90% OF the electric vehicles on the road are powered by permanent-magnet synchronous motors (PMSMs). All PMSMs rely on significant amounts of so-called rare-earth (RE) minerals to make them compact, practical, and powerful enough to compete with internal combustion engines. Although the unique properties of REs such as neodymium, terbium, and dysprosium have played an important role in the success of EVs, there's a growing trend within the industry to reduce their use or eliminate them entirely.

The shift is being motivated in part by the rising costs of RE materials,¹ but many manufacturers are also acutely aware of the environmental impacts associated with mining and refining them.² Furthermore, European and North American manufacturers are concerned about the geopolitical impact of their dependence on REs that, at least for now, are primarily sourced from China, Africa, and other sensitive parts of the world.³

On top of that, PMSMs must be carefully protected against overheating, which can permanently de-magnetize the motor. They must also be protected against failure modes that could produce "uncontrolled generation" conditions, leading to deadly power surges being sent through the motor and its drive electronics.

As a result, many manufacturers are developing innovative magnet-free motor architectures. Many of these are new twists on the wound-rotor synchronous motor (WRSM), which replaces the PMSM's permanent magnets with electromagnet coils (*Fig. 1*).

Others are developing improvements on reluctance-type motors that derive their torque from the attraction between electromagnets in the stator and a magnetically soft iron or steel rotor. In Part 1, we'll cover RE-free WRSMs.

WRSM on the Rise

WRSM motors are very attractive to some manufacturers because they can be near-drop-in replacements for their currently used PMSM units (Fig. 2).

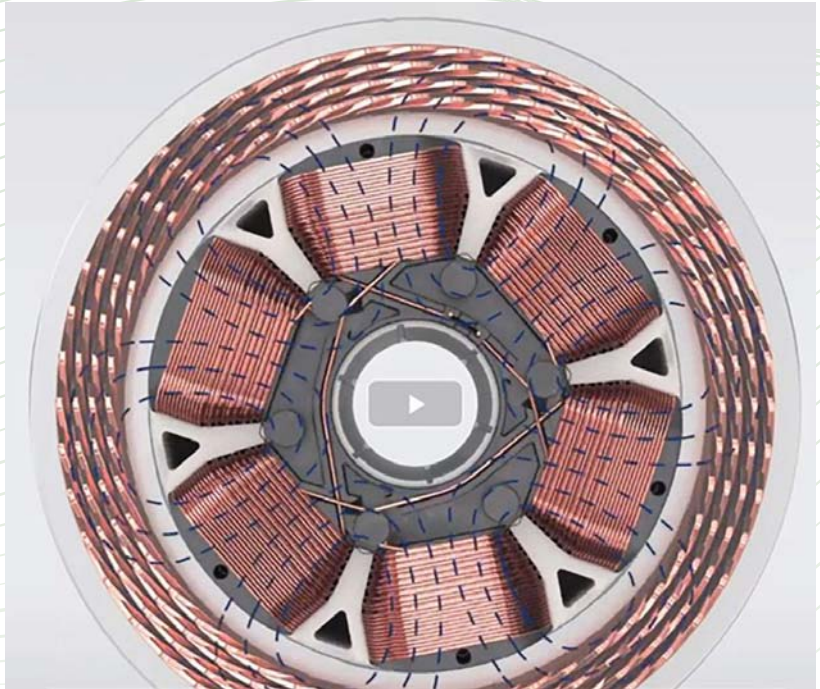
And because the rotor's field strength can be electronically adjusted (something that can't be easily done with fixed-strength PMs), the control electronics required for four-quadrant traction applications (i.e., motoring and braking in forward and reverse) are relatively straightforward.

But this simplicity comes at a price. Barring significant innovations in its design, a motor based on the basic WRSM architecture will suffer from somewhat lower power density than a comparable PM motor. In addition, the WRSM's wound rotor can be more expensive to assemble. However, much of that is offset because the copper windings don't need the costly RE minerals required in nearly all permanent-magnet-based rotors.

The other potential problem with WRSM technology is that it needs some way to deliver the power to energize its spinning rotor assembly, typically some sort of slip-ring assembly. Since slip rings and their associated brushes are susceptible to mechanical wear, they have the potential to introduce reliability problems—they slowly erode and introduce conductive particles into the area where the motor's high-voltage windings reside.

Some manufacturers have decided that WRSM's advantages outweigh the potential risks, and that they can overcome these issues. BMW, for example, applies slip rings to energize the rotor windings of its 5th-generation electric motor⁴ found in its iXM60 EV (Fig. 3).

The vehicle uses a pair of these slip-ring-energized WRSMs, with a 255-hp front motor and a 483-hp rear motor.



2. Wound-rotor synchronous motors (WRSMs) use the same stator assembly as PMSM machines but replace the permanent magnets that form their rotors with electrically energized inductors. Mahle



3. Shown is a close-up of the slip-ring assembly that powers the rotor of the motor used in BMW's iX-M60 electric SUV. BMW

The company says it's confident that its brush assembly, housed in an enclosed and sealed compartment, will be very reliable and eliminate the potential for dust contamination inside the stator/rotor assembly.

Vitesco, a German drivetrain component manufacturer, has also adopted slip-ring technology to develop an alternative

version of the permanent-magnet synchronous e-motor used in its EMR4 platform (Fig. 4). The original EMR4 platform is a scalable axle drive consisting of a PM synchronous machine, inverter, and reducer. Depending on the application's power requirements, the platform can now be used to build motors that use either PMSM or WRSM rotors of different lengths.



4. Vitesco's new WRSM rotor design is a drop-in alternative to the PMSM rotors originally used in its EMR4 EV drivetrain platform. Vitesco

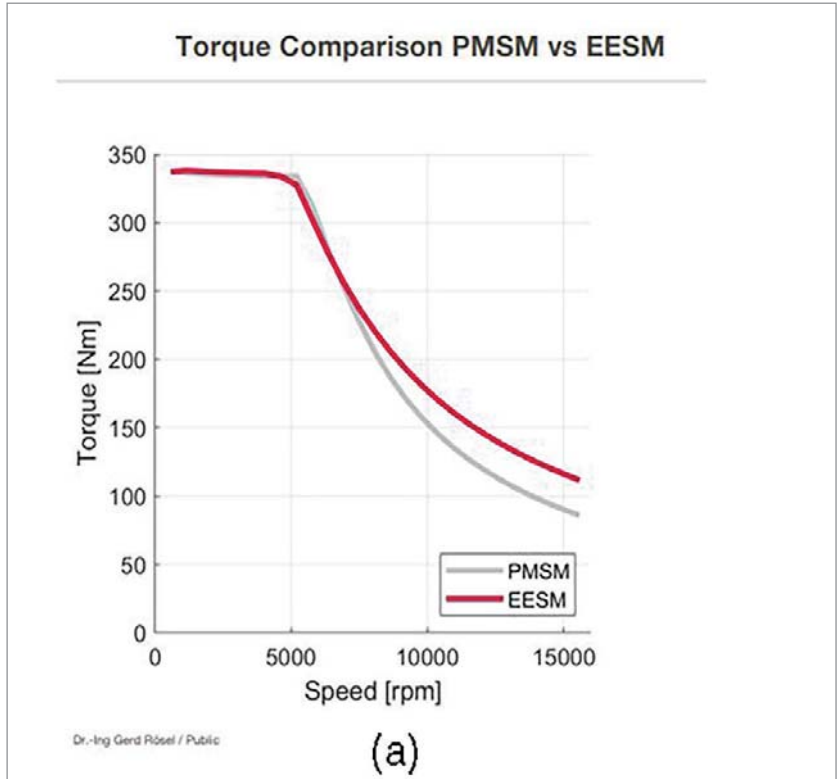
Both variants take advantage of Vitesco's unique "wave winding" process⁵ used to fabricate stators, providing a combination of excellent power density, efficiency, high-frequency operation, and cooling characteristics. Depending on the size of the WRSM rotor it's built to drive, the power unit can produce between 80 and 230 kW.

When configured to run with a WRSM rotor, Vitesco's integrated drivetrain appears to overcome some of the shortcomings associated with PMSM motors. Most notably, it maintains almost constant power output as RPMs increase (Fig. 5a). On the other hand, it exhibits slightly higher mechanical and electrical losses than a comparable unit running with a brushless permanent-magnet rotor (Fig. 5b).

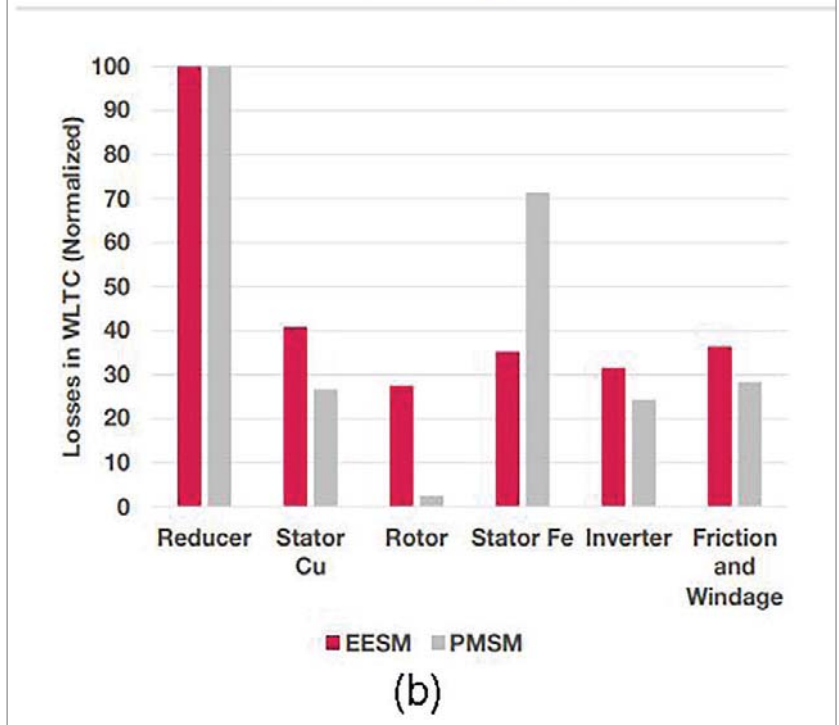
Some or all of these extra losses may be balanced out by the WRSM rotor's absence of magnetically induced drag, which PM motors exhibit during coasting. According to Vitesco, this reduction in drag lowers the drive's power requirement by up to 5%, all without necessitating a mechanical decoupling device.

Giving WRSM the Brush-Off

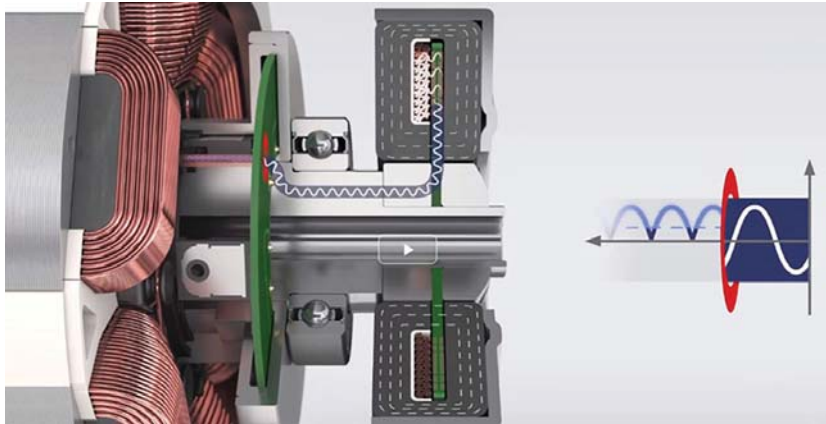
For those who feel that the downsides of rotating connections are unacceptable, several companies are developing brush-free WRSM architectures. Mahle, a Stuttgart-based automotive component manufacturer, has demonstrated a pre-



Detailed Loss Separation




5. The WRSM rotor developed by Vitesco produces a significantly better power curve at the expense of slightly higher losses. Vitesco



6. This is a close-up of the inductive power transmission system used to energize the rotor in Mahle's new WRSM motor. Vitesco

production WRSM drive unit that transmits power to the rotor inductively, using a pair of closely coupled coils (Fig. 6). The stationary transmitter coil, located in the motor body, emits an AC waveform that induces a current in the receiving coil, mounted on the rotor shaft, which is used to energize the rotating copper windings.

Martin Berger, Mahle's head of research, said that the new motor incorporates the best attributes of several existing motor architectures, such as delivering good efficiency at both low and high torque levels. In addition, Berger says that the motor achieves at least 95% efficiency in typical EV use and tops 96% efficiency in some use cases.

According to an article published in *IEEE Spectrum* in May of 2021,⁶ Mahle said that samples are already being delivered and mass production is about two-and-a-half years away. 

FOR PARTS 2 AND 3 of this series, go to <https://electronicdesign.com/21272244> and <https://electronicdesign.com/21273164>.

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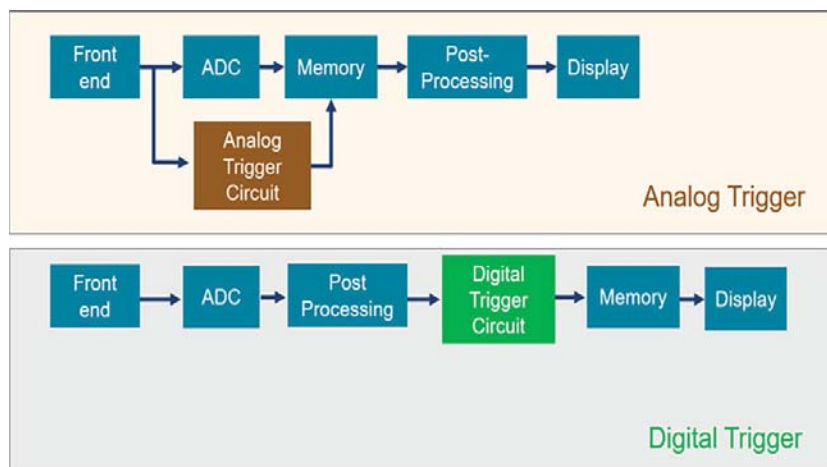


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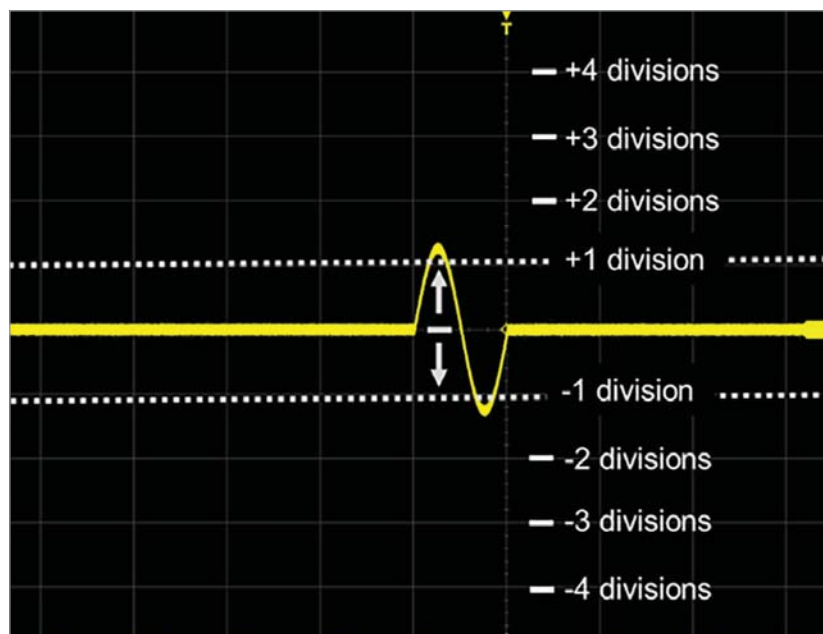
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Triggering: The Digital Edge Over Analog

Oscilloscopes with digital triggers have many advantages. Understanding them can help you make an informed choice when purchasing your next scope.



1. Analog triggering architecture vs. digital triggering architecture. Images courtesy Rohde & Schwarz



2. Trigger sensitivity is the signal amplitude required to guarantee that the signal will be considered a trigger event.

AN OSCILLOSCOPE'S TRIGGER

function, which synchronizes the horizontal sweep with the input signal, is crucial for clear signal analysis. The better the triggering system, the less time you need to spend trying to isolate rare events. Basic trigger controls stabilize repetitive waveforms by repeatedly displaying a selected portion of the input signal. Advanced trigger controls allow you to isolate specific events, optimizing sample rate and record length.

Digital vs. Analog Triggering

Most oscilloscopes still have an analog triggering architecture. There's a data path for the incoming signal and a separate path for triggering. Newer oscilloscope architectures use digital triggering, which combines the two paths into one (Fig. 1).

Analog triggering relies on analog circuitry to analyze the incoming signal and determine when to trigger the acquisition. The signal path is separated from the trigger path to ensure that the trigger circuitry operates independently. Oscilloscopes with analog triggers typically detect events based on voltage levels, slopes, or pulse widths, using adjustable thresholds and trigger modes such as edge, pulse, or video.

Digital triggering architectures utilize a single shared path for both the signal and triggering functions. This means that the incoming waveform is digitized and digitally processed to determine the trigger condition.

The trigger circuitry operates directly on the digitized data, allowing for a more precise and flexible triggering

mechanism. Digital triggers can leverage advanced algorithms and sophisticated mathematical functions to detect events based on complex conditions, such as specific data patterns, glitches, or runts.

Advantages of Digital Triggering

Digital triggering holds a number of advantages over analog triggering, including:

- Greater trigger sensitivity
- User hysteresis control
- Wider range of filters
- HD mode applied on trigger
- Interpolation
- Lower trigger jitter

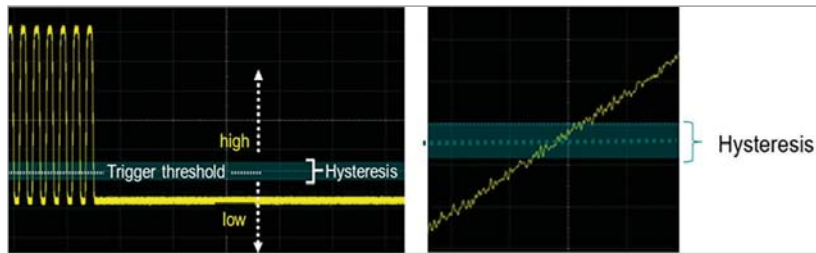
Trigger sensitivity refers to the minimum signal amplitude required for an oscilloscope to accurately detect trigger events (Fig. 2). This is important because superior trigger sensitivity allows you to isolate and trigger on small signals. It's typically specified in terms of vertical divisions on the oscilloscope display.

For example, modern oscilloscopes like Rohde & Schwarz's MXO 4 have a high trigger sensitivity of 0.0001 div. As a result, when the setting is 10 mV/div (and the full vertical height is 100 mV), the oscilloscope can trigger on a signal with an amplitude of 10 μ V.

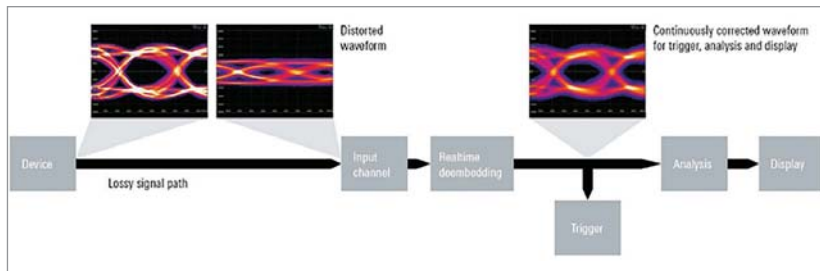
An oscilloscope's trigger threshold is the level a signal must exceed for the oscilloscope to recognize it as a trigger event. Hysteresis, or "window size," introduces a window above or below the trigger level. Analog oscilloscopes typically have preset hysteresis values, while digital oscilloscopes offer both automatic hysteresis settings and user-adjustable options.

With user-adjustable hysteresis, you can eliminate false triggers from noise by setting a higher value or trigger on small changes in signal amplitude by selecting lower values. This flexibility in hysteresis adjustment allows for greater control and improved triggering performance (Fig. 3).

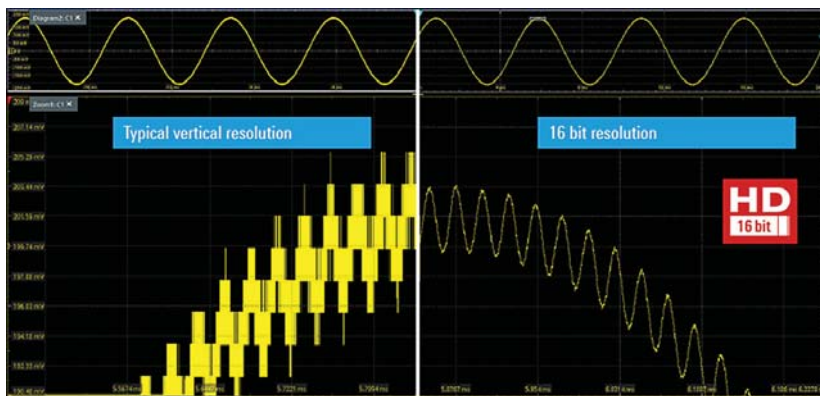
Oscilloscopes offer various signal filters for signal viewing. These filters can be implemented using analog hardware, digital-signal-processing (DSP) algorithms,



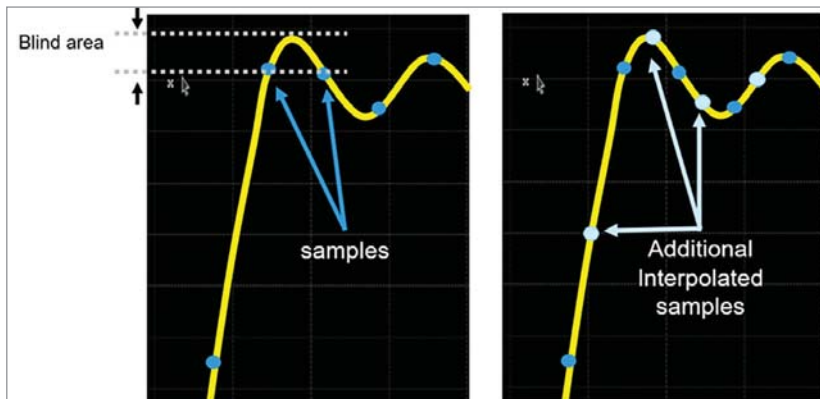
3. Hysteresis helps minimize false triggering that results from noise or signal jitter.



4. Real-time de-embedding is applied before the trigger enables you to trigger on the same de-embedded signal that's seen on the oscilloscope display.



5. Digital triggering architecture allows for the HD mode to apply in real-time to both the signal and trigger.



6. Digital triggers can use interpolation between sample points to eliminate areas that would otherwise be blind to triggering.

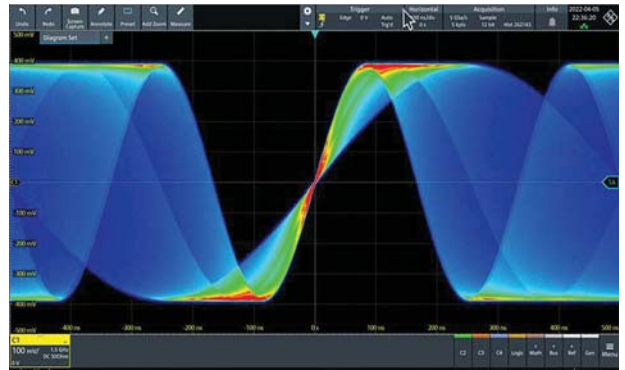
Digital Triggering

or software. Signal-path filters don't affect the trigger circuit for oscilloscopes with analog triggers. However, for oscilloscopes with digital triggers, filters can be applied to the trigger, the signal, or both.

An advantage of digital trigger architectures is that the displayed waveform on the oscilloscope precisely reflects what the trigger circuit is evaluating, ensuring accurate visualization and analysis. Functions like real-time de-embedding are applied before the trigger, enabling the oscilloscope to trigger on the same de-embedded signal that users see on the oscilloscope display (Fig. 4).

With most oscilloscopes, you can make tradeoffs between bandwidth and vertical resolution using acquisition modes. These modes average adjacent samples or apply DSP-based filters to increase vertical resolution while reducing effective sample rate. Oscilloscopes with analog triggers have a high-resolution mode, but it only applies to the signal path and not the trigger path. Scopes with digital triggers, on the other hand, offer HD mode, which allows you to improve trigger resolution and noise suppression by reducing the bandwidth (Fig. 5).

Analog triggers often have a limited threshold range with coarse increments. In contrast, digital triggers offer more flexibility—you can select any threshold value within the set vertical range. This is because the digital trigger architecture evaluates



7. Oscilloscopes with digital triggers are less subject to jitter than scopes with analog triggers.

the signal after the analog-to-digital conversion and isn't bound by bandwidth limitations.

Since the information is in digital form, the instrument can make decisions based on interpolation between sampled points. This enables you to isolate minute signal details by adjusting trigger threshold and sensitivity (Fig. 6).

Oscilloscopes with analog triggers need to determine the precise time in the signal path that corresponds to the detected trigger event. This may cause trigger jitter over successive acquisitions.



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Some oscilloscope manufacturers offer software correction techniques to mitigate trigger jitter. While effective in reducing jitter, these corrections need additional processing cycles, leading to slower trigger re-arm times and overall scope update rates. Oscilloscopes with digital triggers, on the other hand, have minimal trigger jitter without requiring software correction techniques (Fig. 7).

Digital or Analog: How to Tell?

Most oscilloscopes still use analog triggering. If “digital triggering” isn’t specified in the product datasheet, the oscilloscope likely uses analog trigger technology. You can also make a reliable assessment of the oscilloscope’s trigger based on other datasheet specifications.

An oscilloscope uses digital triggering if:


- It has a trigger sensitivity of less than 0.1 div. Analog triggers can’t achieve this sensitivity.
- The user can choose from a wide range of hysteresis values, from 5 div down to 0.01 div.

In addition, if an oscilloscope has a minimum trigger re-arm time in normal mode (not a special mode) measured in 10 to 100 ns, it likely has a digital trigger architecture. If you have any doubts or


questions about an oscilloscope’s specifications, you should always contact the manufacturer.

Summary

The oscilloscope trigger function plays a crucial role in synchronizing the horizontal sweep of the instrument with the signal and enabling clear signal characterization.

Digital triggering offers several advantages over analog triggering, including greater trigger sensitivity, user hysteresis control, a wider range of filters, the application of HD mode on triggers, interpolation capabilities, and reduced trigger jitter. You can determine an oscilloscope’s triggering technology by referring to its datasheet or asking the manufacturer. 

ISOLATING EVENTS WITH MORE PRECISION



The R&S MXO 4 series oscilloscopes feature a digital trigger that’s up to 10,000X more sensitive than the trigger systems of instruments using still using older analog trigger architectures. It’s claimed as the fastest oscilloscope with an update rate of 4.5 million waveforms/s. The 12-bit analog-to-digital conversion provides 16X the resolution of traditional 8-bit oscilloscopes, and it has 100X the memory of comparable instruments, according to R&S, ensuring ample storage space for in-depth analysis.

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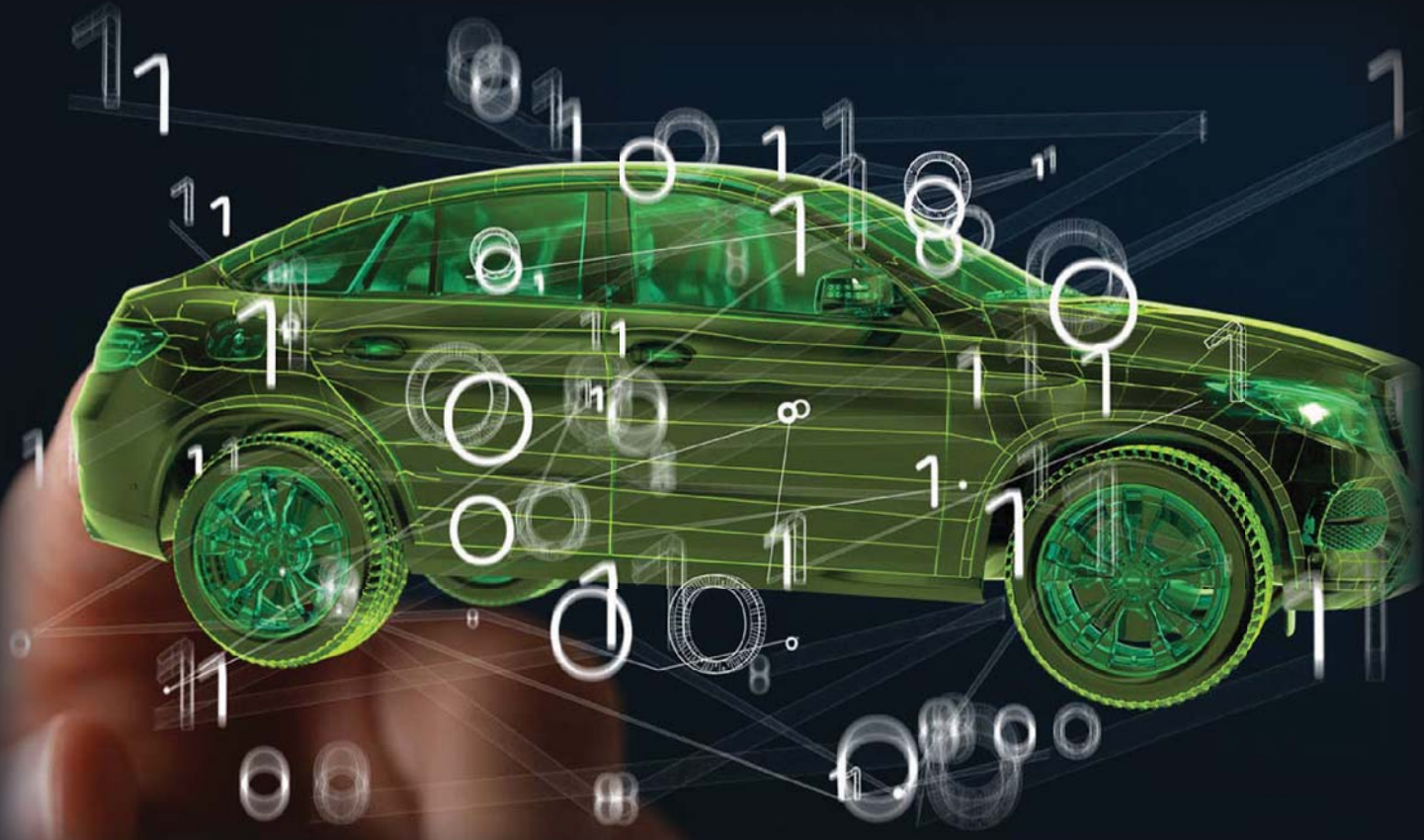
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Applying Exhaustive Static Analysis to Automotive Software Testing

Learn how mathematically proven code correctness and hardware awareness leads to 100% coverage and zero issues for automotive systems.

AUTOMOTIVE SOFTWARE DEVELOPERS hold the belief that verification, validation, and compliance activities can never approach 100% code and inputs coverage. This conviction is fueled by the rising complexity in vehicle systems, with distributed architectures, connectivity, virtualization, and other needs pushing

the envelope of testing capacity and compliance to standards like ISO 26262 and ISO 21434.

Recent advances in academic research and computing power have proven that 100% code and inputs coverage is possible, and its benefits are now available to safety- and security-critical automotive development teams.

Exhaustive Static Analysis Guarantees Code Correctness

To bridge the gap between “sufficient” code coverage and 100% coverage, exhaustive static-analysis tools use mathematical models and techniques to verify properties and behaviors of software against precisely defined specifications. Known in research circles as formal methods, these

techniques prove that code is free from issues like bugs and security vulnerabilities, and they overcome the key limitations of traditional tests and static-analysis tools:

- **Coverage:** As software complexity grows, it becomes increasingly harder for test teams and traditional tools to cover the code base in levels sufficient for compliance activities, including functions, statements, paths, decisions, and conditions.
- **Scale:** The more units under test—features, components, libraries, and functions—the more time and resources are required to test them.
- **Speed:** Shorter release cycles are often at risk due to the inability of traditional test development and execution practices to keep pace with software complexity, forcing a tradeoff between test scope and time.
- **Proof of compliance:** Identifying and eliminating undefined behaviors and security risks, as expected by the ISO 26262 and ISO 21434 standards, is difficult to achieve due to growing code complexity and the number of certification components.

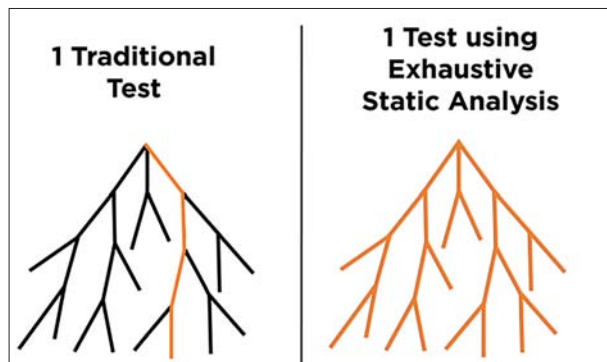
Exhaustive static-analysis tools are designed and proven to integrate the power of formal methods into the existing test and compliance processes of automotive teams. These tools hold several advantages over traditional testing and static-analysis methods:

- Up to 100% application coverage that includes all possible functions, statements, paths, decisions, and conditions.
- Up to 100% input coverage, including all possible values within the scope of the unit under test.
- A mathematical guarantee of the absence of undefined behaviors (errors and vulnerabilities) in code, resulting in zero issues at deployment time.
- Zero false negatives, ensuring all issues are found.
- Low to zero false positives such that developers aren't overwhelmed by analysis findings and don't waste time chasing non-issues.
- Provide proof that supports ISO 26262 and ISO 21434 certification.

Figure 1 illustrates how exhaustive static analysis improves test coverage, showing how traditional “best effort” test design executes only one code branch per run versus all branches in parallel per run. The use of formal methods enables the running of tests for all possible inputs and leads to 100% code and inputs coverage, with dramatically reduced test time.

How Exhaustive Static Analysis Identifies a Buffer Overflow

Memory buffer problems have long plagued embedded software developers, and the buffer overflow exploit remains a top automotive vulnerability. This exploit occurs when the



1. Code paths are compared between traditional testing methods (left) and exhaustive static analysis (right). Visited segments are in orange; unvisited segments are in black. Images courtesy TrustInSoft

bounds of allocated memory aren't checked during read and write operations. It leads to the application “overflowing” the capacity of the buffer, impacting areas not intended for data extraction or modification.

The following code sample illustrates a C function that increments cell values in an array:

```
void increment_array(int array[], int len)
{
    while (len >= 0)
    {
        (*array)++; // Increment the value of the array cell
        array++; // Move to next array cell
        len--; // Decrement counter
    }
}

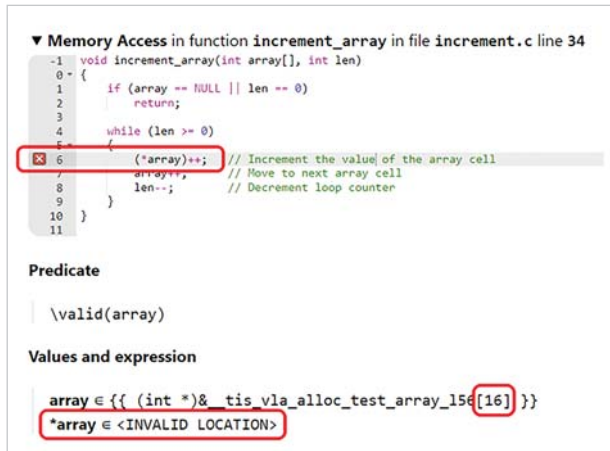
int main(int argc, char *argv[])
{
    int data[4] = {1, 3, 5, 7};
    char name[] = "foobars";
    increment_array(data, 4); // Increment array
}
```

A traditional test would validate the function's requirement to increment the cell values in the output array and report a pass or fail based on the result. The test designer may not consider checking whether the loop end condition—and therefore the array index—caused an out-of-bounds memory access due to unexpected or undesired side effects in the system. This does occur in this code sample due to an improper condition specified in the **while** loop.

A traditional test against requirements would miss the buffer overflow condition and report that the array is {2, 4, 6, 8} after calling the function. Thus, it would always pass, as shown in the console output from an example test run:

```
gcc -I. increment.c -o ub && ./ub
Run test_increment_array()
increment_array({1, 3, 5, 7}) = {2, 4, 6, 8}
--> PASSED
```

Unless the test designer considered the possibility of an out-of-bounds array access, the test would never report the buffer overflow. This subtle flaw could cause memory corruption, leading to a potential bug, crash, or application vulnerability in vehicle software. While traditional tests rely on the designer to remember and implement all possibilities, exhaustive static-analysis tools provide 100% coverage out of the box (Fig. 2).



2. This is a screenshot of a buffer overflow finding within the Trust-InSoft exhaustive static-analysis tool.

Here, the tool detects the application writing 16 bytes after the beginning of the array. This memory corruption is revealed by a more verbose test case where the out-of-bounds write condition affects the value of the variable **name**, even though it's not involved in the tested function, as shown in the following console output:

```

gcc -DVERBOSE -I. increment.c -o ub && ./ub
Run test_increment_array()
Address(data) = 0x7ffe8eb68f50 = 140731292749648
Address(name) = 0x7ffe8eb68f60 = 140731292749664
Before increment array = {1, 3, 5, 7} - name = foobars
After increment array = {2, 4, 6, 8} - name = goobars
increment_array({1, 3, 5, 7}) = {2, 4, 6, 8}
--> PASSED
    
```

While this is a simple example for illustrative purposes, applications with complex control and data paths can benefit from the use of exhaustive static analysis.

How Hardware Awareness Improves Testing Accuracy

Exhaustive static-analysis tools that take the actual vehicle computing hardware into account help to improve the accuracy and efficiency of software testing. Differences in compiler implementations, hardware architectures, and memory alignment between platforms can lead to drastically different code behaviors. For example:

- On 64-bit targets, **long** is typically 64 bits and **int** is typically 32 bits.
- On 32-bit targets, both **long** and **int** are typically 32 bits.

These implementation characteristics influence test design, as shown in this code sample:

```

long double_that(int i)
{
  return (long)i * 2;
}

double_that(0x7FFFFFF0);
    
```



3. Exhaustive static analysis offers multiple benefits across the automotive software V-cycle.

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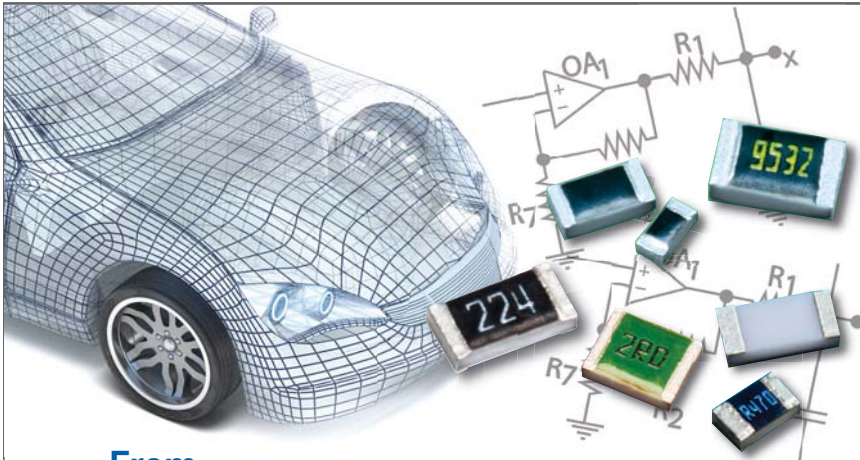
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The road to 100% code coverage starts with exhaustive static analysis. Automotive software development teams that prioritize exhaustive static analysis derive the greatest value from their testing and compliance investments.



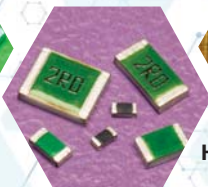
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Tests or static-analysis methods that are unaware of the underlying implementation would not know whether the last statement causes an integer overflow (32-bit target) or is safe behavior (64-bit target). This code would decrease the efficiency of test designs that assume a 64-bit data range when the target is actually 32-bit, and negatively impact accuracy when assuming a 64-bit target and potentially missing the integer overflow when it's actually 32-bit.

Hardware-aware exhaustive static analysis offers the perfect balance between 100% coverage and the minimum number of test cases necessary to achieve it. It also offers these benefits:

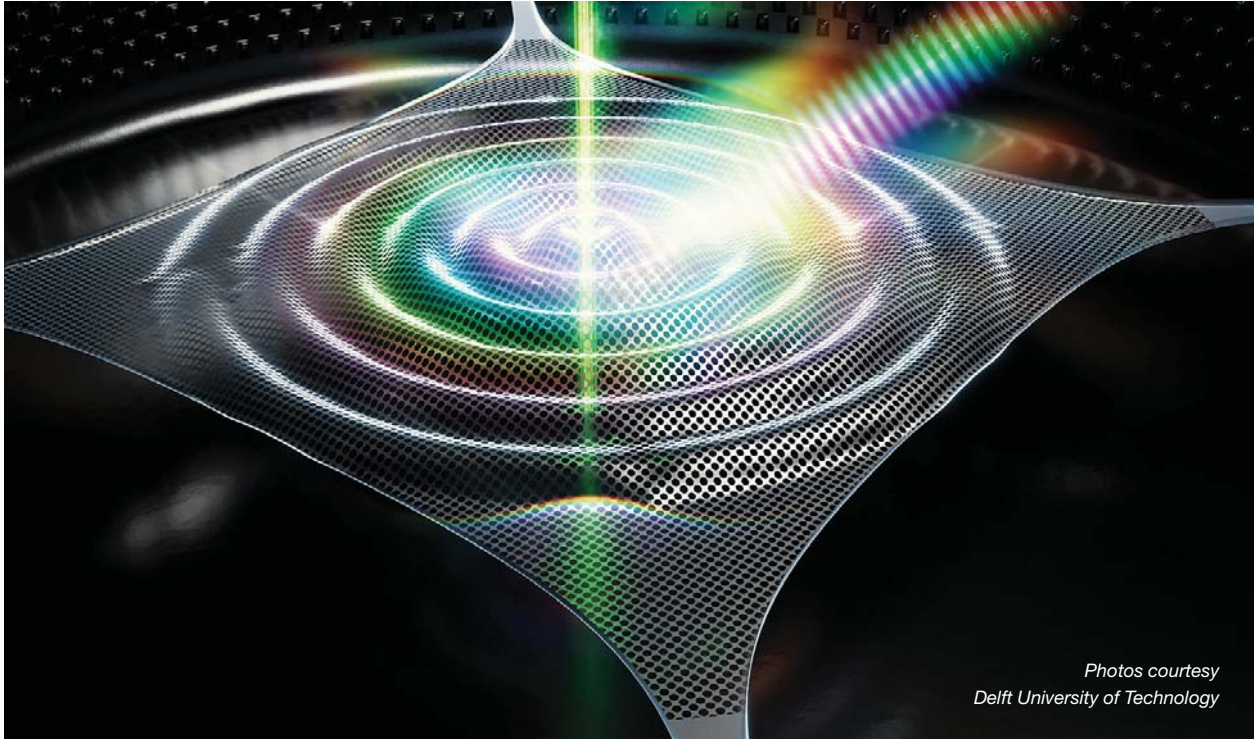
- Tests can be run without requiring a physical target connected to the host.
- Target tests can be run earlier in the development lifecycle before the physical hardware is available.
- Test capacity can increase while costs decrease as physical hardware isn't required for every developer.

Figure 3 summarizes the benefits of exhaustive static analysis throughout the automotive software V-cycle.

Conclusion

The road to 100% code coverage starts with exhaustive static analysis. Automotive software development teams that prioritize exhaustive static analysis derive the greatest value from their testing and compliance investments. Achieving up to 100% code coverage with a mathematical guarantee of the absence of undefined behaviors supports standards like ISO 26262 and ISO 21434, and positions manufacturers to deliver safer, more secure code.

Achieving a "zero issue" guarantee is a long-term objective that can only be met with formal methods-based testing practices. Being proactive with exhaustive static analysis now significantly reduces the likelihood of software bugs and vulnerabilities in the field, further enhancing the overall reliability and security of automotive software systems.



Photos courtesy
Delft University of Technology

Precision Distance-Measuring Microchip Blends Two Nobel Prize-Winning Techniques

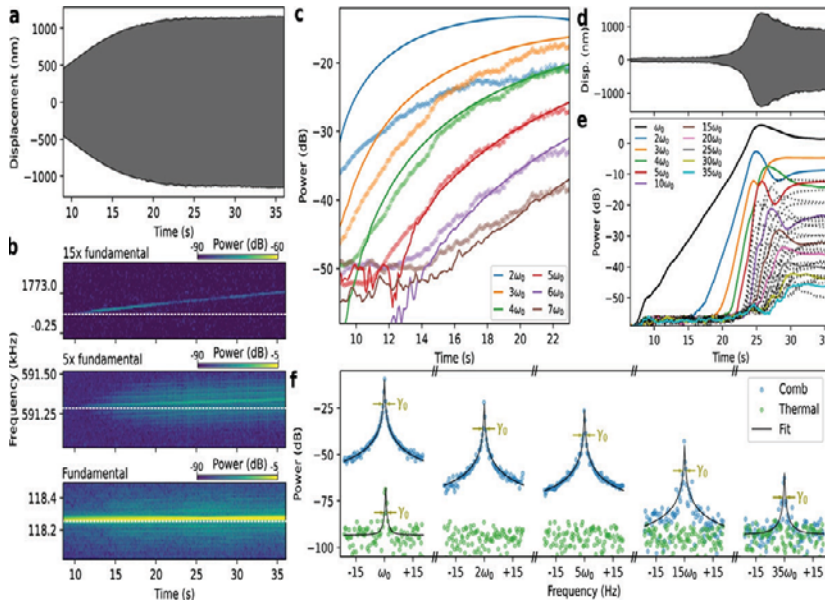
By combining optical trapping and frequency combs—two widely used but unrelated developments in advanced physics—researchers devised a way to measure micro-dimensions in opaque materials.

It's not unusual for a technical Nobel Prize to be awarded in recognition for an advancement that's already had practical applications, usually in well-defined scenarios, such as blue LEDs (2014) or optical fibers for communications (2009). Now, physicists at Delft University of Technology (Netherlands) have gone further, building a new technology on a microchip by combining two Nobel Prize-winning techniques—apparently the first time this has occurred.

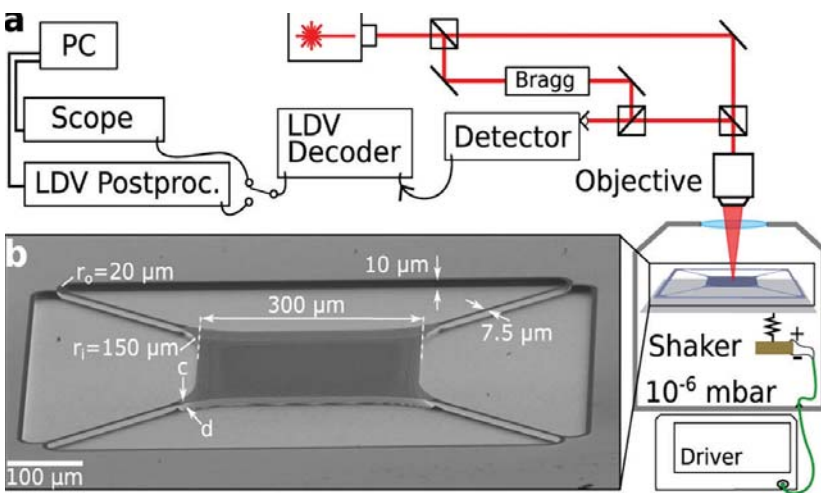
Their microchip could measure distances in materials at high precision, including for underwater or medical imaging. Because the technology uses sound vibrations instead of light, it's useful for high-precision position measurements in opaque materials. These mechanical frequency combs are poised to bring the

applications and utility of optical frequency combs into the mechanical domain. (This Nobel-prize “applicability” connection isn't always apparent, of course; *see the sidebar at the end.*)

The Delft team used two unrelated Nobel Prize-winning techniques. The first is optical trapping, which employs laser beams to trap even the smallest particles in one spot and then manipulate them with extreme, tweezer-like precision (2018). The second is a coherent optical frequency comb, where a laser is controlled to function as a broad-spectrum light source delivering equally spaced frequencies, while its time waveform appears as a sequence of ultra-short pulses (2005). Both “developments” have become invaluable tools across many unrelated research disciplines.



1. (a) Measured displacement of membrane, showing clear growth before reaching a plateau around $t=24$ sec. (b) Measured spectrum of membrane motion close to fundamental mode and two of its overtones (5th and 15th). A thermal shift of 9 Hz of the fundamental mode is visible as a 5×9 and 15×9 Hz shift in the overtones (white dashed lines are horizontal to guide the eye). (c) First six overtones increase in power as the membrane displacement increases (markers) in (a). (d) Membrane displacement of a different device (different chip) than (a), showing growth from close to the thermal regime to steady state. (e) Overtone amplitudes extracted from the spectrum of measurement of (d), showing all 35 overtones within the detection bandwidth (black, dotted lines are overtones with numbers between the labeled ones). (f) Spectrum showing measured fundamental mode and some selected overtones in the comb regime (blue) and thermal (green), along with Lorentzian fit with center frequencies $n\omega_0$ (n integer) and identical linewidths γ_0 .



2. (a) Schematic of the laser Doppler vibrometer (LDV) setup, where we access the chip containing the membranes using a microscope objective directly outside a vacuum chamber. (b) Scanning electron microscope (SEM) image of the suspended membrane, with nominal design parameters in white.

Microchip Construction

Their microchip consists of a thin ceramic sheet that’s shaped like a trampoline, patterned with holes to enhance its interaction with laser; they monolithically integrated the suspended dielectric membrane with a counter-propagating optical trap (Fig. 1). The laser’s impingement on this membrane created a frequency comb consisting of mechanical overtones (integer multiples) of a single frequency.

When measuring the reflected laser light from the vibrating surface, the team noticed a pattern of vibrations in the shape of a comb that they hadn’t seen before. They realized that the trampoline’s comb-like signature functioned as a ruler for precision measurements of distance.


“The interesting thing is that both of these concepts are typically related to light, but these fields do not have any real overlap. We have uniquely combined them to create an easy-to-use microchip technology based on sound waves.”

The setup applied in this work used a commercial laser Doppler interferometer (Fig. 2). Light from the vibrometer (LDV) goes through a microscope objective, which focuses it on the chip containing the membrane resonators. This chip is placed in a vacuum chamber and pumped down until the pressure is $<5 \times 10^{-6}$ mbar, to reduce gas damping. The reflected light from the membranes is Doppler-shifted due to their out-of-plane motion, which is then detected by the LDV.

The researchers claim that this mechanism unlocks the potential of mechanical frequency combs for sensing, timing, and metrology applications at the microscale, and provides integration with phononic circuits (elastic waves that propagate in solids). This combination of effects results in an easy-to-use mechanical frequency-comb

platform that requires no precise alignment nor additional feedback or control electronics, and it only uses a single, milliwatt-range continuous-wave laser beam.

Noted team leader Prof. Richard Norte, “The interesting thing is that both of these concepts are typically related to light, but these fields do not have any real overlap. We have uniquely combined them to create an easy-to-use microchip technology based on sound waves.”

The work is detailed in a seven-page paper with the surprisingly short and direct title, “Mechanical overtone frequency combs” published in *Nature Communications*, and bolstered by a 20-page “Supplementary Information” posting. 

NOBEL PRIZES AND EVENTUAL APPLICABILITY

You often can’t tell which Nobel prizes in the “hard sciences” will eventually lead to some practical result. For example, Isaac Isidor Rabi was awarded the Prize in 1944 for his “resonance method for recording the magnetic properties of atomic nuclei” (magnetically induced nuclear precession) and how the nuclei emitted electromagnetic radiation with uniquely characteristic frequencies when the field was removed. This provided interesting insight into quantum mechanics, but otherwise it was considered a “that’s nice, but so what?” discovery—until the 1970s, 35 years later.

That’s when Dr. Raymond Damadian, a physician and experimenter, realized that because tumors contain more water and thus more hydrogen atoms than healthy tissue, there might be a way to use an atomic-level response to see the difference and create images. He then proved this contention via a small-scale medical experiment. Subsequently, he built the first magnetic resonance imaging system (MRI, but at the time called nuclear magnetic resonance or NMR) and produced crude but viable images.

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Optical Trapping

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Damadian and MRI

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MRI, Part 2: Historical development (and lawsuits)



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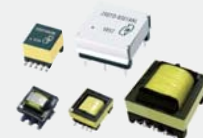
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How to Design for Longer IoT Battery Life with Emulation Software

Testing an IoT device at various charge levels is crucial due to varying battery characteristics, but it also creates multiple challenges. Using an emulated battery can help overcome those hurdles.

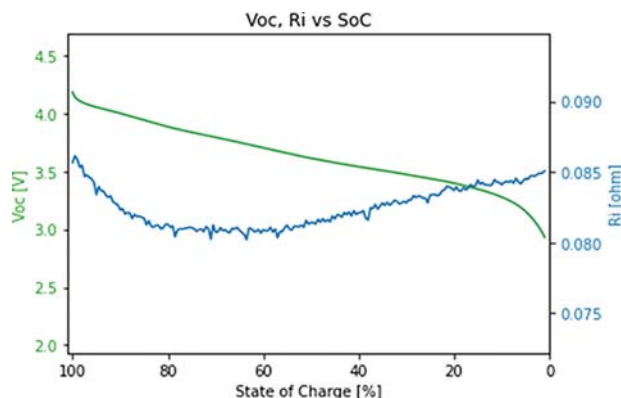
The Internet of Things (IoT) has led to an extraordinary transformation of consumer electronics and industrial applications. IoT enables intelligent, interconnected operations, changing everyday devices into smart systems that enhance efficiency and user convenience. However, the success and utility of IoT devices hinges on their battery runtime.

Consumer IoT devices, from smartphones to wearables, have transformed our daily lives, providing unparalleled convenience to enhance living standards. Yet, the user experience with these devices depends on battery life. Longer battery runtimes reduce charging frequency, providing a seamless, uninterrupted user experience.

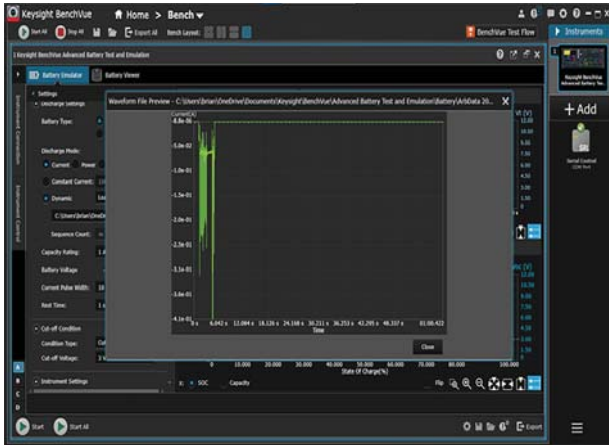
In the industrial sphere, IoT devices are integral in streamlining operations, improving safety, and enhancing productivity. These devices often operate in remote, hard-to-reach, or harsh

environments, making regular battery replacement or recharging unfeasible. Therefore, long battery life is essential for continuous, reliable data collection and system operation.

Emulation software lets you gain rapid insight into your IoT device's current drain and lengthen the battery runtime. In addition, battery emulation and profiling software enables you to accurately predict battery life and aging effects.



1. This battery model was created with Keysight BV9210B/11B PathWave BenchVue advanced battery test and emulation software. Images courtesy Keysight Technologies



2. The device current-consumption waveform is loaded into BV9210B/11B software.

Profiling Batteries to Create Unique Battery Models

Profiling and characterizing batteries helps you understand the amount of energy they can store and supply without needing a physical battery. A battery model created with profiling software maps out the open circuit voltage and internal resistance versus the state of charge (SOC). It's crucial to map out these characteristics for battery models to accurately reflect real-world performance. *Figure 1* provides an example of a typical plot.

Confirming the battery's performance under specific discharge conditions and operating modes is also essential. Parameters that affect battery behavior include:

- Temperature
- Load current profiles (constant/dynamic)
- Operating modes, including constant current, power, and resistance

Therefore, creating different battery models to match specific discharge conditions is vital.

Emulating Charge States to Reduce Test Time and Gain Insight to Extend Battery Life

Why use a battery emulator instead of a battery for device testing? There are several reasons:

- **To create a safer test environment.** It's not necessary to charge and discharge batteries when using an emulator. Charging and discharging batteries can become dangerous with repeated cycles.
- **To achieve repeatable results.** The characteristics of emulated batteries don't vary, while the characteristics of physical batteries can fluctuate after charging/discharging. Characteristics can also vary between batteries, even if they're the same model.
- **To reduce test setup times.** Instantly simulate any SOC rather than manually draining a battery to the desired level.



3. BV9210B/11B software is used for battery emulation.


A battery emulator works in multiple steps. The first step is loading a battery model that comprises the plot of the battery voltage and internal resistance versus the SOC (*Fig. 1, again*). You can create a battery model using battery profiling software or by receiving a profile from a battery supplier.

When using profiling software, the model will reflect the current consumption for a specific device, which is more accurate than a battery supplier's generic profile. For example, a generic

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Battery Emulation

profile isn't helpful if the battery supplier creates the profile based on a constant current draw when the device consumes a dynamic current.

Figure 2 shows a device's current-consumption profile loaded into a battery profiler. The software keeps repeating the waveform until it completely drains the battery and maps out a full battery model.

The next emulation step is to select the starting SOC and the cutoff voltage. Connect the device to the emulator and start the battery emulation.

It's necessary to understand the energy a battery can store and deliver for IoT devices. Battery test and emulation software simplifies this process by automating battery charging and discharging to determine capacity.

Battery emulators continuously measure the current, charging or discharging, and dynamically calculate emulated SOC. The emulator continuously changes its output (voltage and resistance) based on the SOC to conform to the loaded battery profile (Fig. 3). If the emulator is discharging, the test ends when the emulator reaches the cutoff voltage.

Emulating a battery at different SOCs provides deep insight into a device's behavior. Figure 4 shows insight into a device's current drain. You can quickly assess the effect of design or software changes and optimize your design to extend battery runtime.

Automating Charging/Discharging of Batteries to Determine Capacity

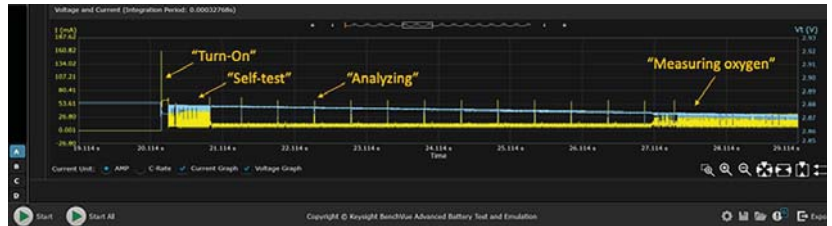
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devices. Battery test and emulation software simplifies this process by automating battery charging and discharging to determine capacity.

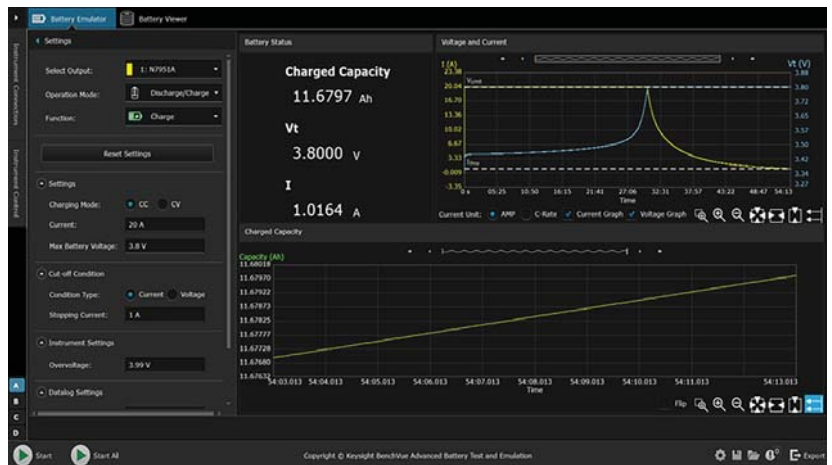
Software must support constant-current (CC) and constant-voltage (CV) modes for charging batteries. As the battery reaches full capacity when charging using CC mode, the software needs to

move from CC mode to a combination of CC and CV. This combination is necessary because you can't charge a battery at the same rate when it gets close to peak voltage or capacity.

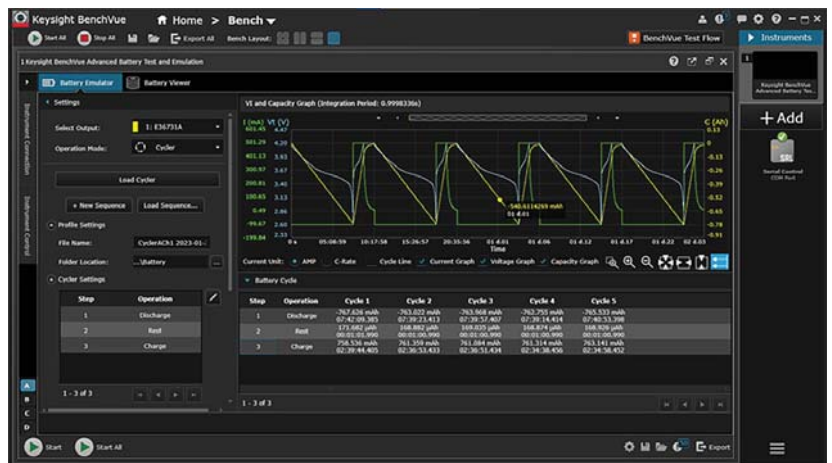
You can use constant-current, constant-resistance, and constant-power modes to discharge a battery. However, you can achieve a more accurate capacity estimate



4. Current drain analysis is performed for a pulse oximeter medical IoT device.



5. Battery charging is visually tracked using BV9210B/11B software.



6. Tests for battery cycling are conducted using Keysight's software.

using a dynamic current waveform for battery discharge.

Battery test software makes it possible to create a current-consumption profile directly from a device (Fig. 5). You can then use the profile to drain the battery via software to achieve a real-world estimate. Simulating this with the actual device is difficult as you must operate it throughout the rundown test. Therefore, it's much more practical to automate this process with software.

Cycling Batteries to Determine Loss of Capacity and Reduction of Battery Life

Battery performance can decline significantly over a lifetime of charging and discharging. This is why it's vital to simulate battery cycling. A battery-cycling software solution must support the ability to create varying charging and discharging profiles.

The software can combine disparate sequences to simulate complex charging and discharging cycling profiles (Fig. 6). Then you can confirm how a battery's performance degrades over time. Emulation software solutions are ideal for this as they can enable, for example, up to 1,000 cycle operations to determine the battery's aging effect and reliability under sequence test conditions. Software must offer data-logging capabilities to store all of the data.


Summary

Current drain and battery rundown testing present many challenges. The manual process of charging and discharging a battery is time-consuming, but testing your device at various charge levels is crucial due to varying battery characteristics.

Furthermore, battery parameters and charge levels must be identical when comparing test results. Achieving this is challenging with physical batteries. In addition, it can be difficult to determine how long a device can last on a single charge, and battery life claims often don't match reality.

Using an emulated battery can help you overcome these difficulties. First, a

battery model provides a known-good reference, boosting trust in your test results. Plus, you can quickly assess the effect of design or software changes on battery life by instantly transitioning the battery's charge state. These abilities enable you to enhance your designs to achieve longer battery life and smaller size.

On top of that, a software solution enables you to accurately estimate battery life by automating battery rundown using the simulated device's current drain. This method is more accurate than using constant current to drain a battery. The automated process is also more straightforward than manually draining a battery through device usage. 



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Optimize SoC Design with a Network-on-Chip Strategy

Utilizing physically aware interconnect IP from trusted third-party vendors can reduce design time and increase productivity.

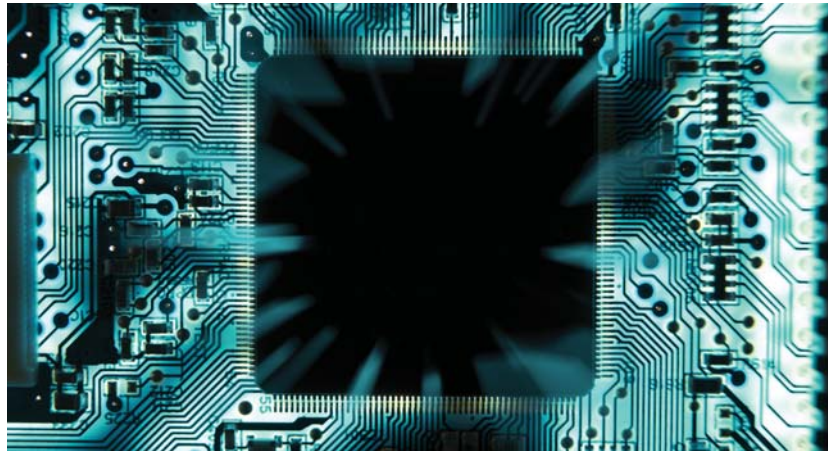
Today's system-on-chip (SoC) devices can contain hundreds of millions to over a hundred billion transistors, depending on the application. The only way to create designs of this complexity is to employ large numbers of functional blocks called intellectual-property (IP) blocks or IPs.

Many of these blocks embody well-known and standard functions, such as processor cores, communication cores (Ethernet, USB, I²C, SPI, etc.) and peripheral processes. Rather than spend valuable time and resources re-implementing these functions from scratch, SoC design teams acquire these IPs from respected third-party vendors.

Access to robust, tested, and proven IP speeds up the development process and reduces risk. Using third-party IP for common functions frees the SoC design team to focus on their own "secret sauce" IP blocks, which will differentiate their SoC from competitive offerings.

Making SoC Connections with NoCs

An important aspect of any SoC is how the IP blocks will communicate with each other. In the 1990s, it was common to use a bus-based interconnect architecture. By the 2000s, designers adopted crossbar, switch-based interconnect architectures to accommodate the increasing number of IP blocks. In the 2020s, the predominant SoC interconnect strategy involves at least one network-on-chip (NoC) implementation.



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When they hear the term "IP," most SoC designers think of register-transfer-level (RTL) representations at the front end and square or rectangular footprints on the silicon die at the back end. There's a certain category of SoC IP called "system IP." Examples of such IP are NoC interconnect, debug and trace components, and memory, cache, interrupt, security, and fault-detection controllers.

System IP enables designers to build high-performance, power-efficient, reliable, and configurable systems for many different applications. NoC system IP spans the entire SoC and interacts with almost every block in the design in some way.

Mitigating SoC Complexity

To lessen the complexity of connectivity in the SoC design, each IP block will typically implement an interconnect protocol. One challenge with purchasing third-party IPs is that, over time, multiple interconnect protocols have been defined and adopted by the SoC industry (OCP, APB, AHB, AXI, STBus, DTL, etc.).

Since an SoC may contain hundreds of IP blocks from various third-party vendors, the interconnect IP must

accommodate all of these standard protocols. Furthermore, different IPs may have distinctive data widths and run at varied frequencies.

The interface on an IP is known as a "socket." A network interface unit (NIU) connects the socket to the NoC. At the transmitting end, an initiator IP's associated NIU translates its interface and protocol into the internal NoC protocol, including packetizing the data. At the receiving end, an NIU translates the packet in the NoC protocol back into the required target IP interface and protocol.

Multiple packets can be in flight at the same time. The NoC also includes buffers to store data temporarily, switches to guide packets between initiator and target IPs, and pipeline stages to help the physical layout team close timing.

Saving Time and Money with Third-Party NoC IP

Remembering that a NoC is a complex system IP, the SoC development team now has a choice. The designers can create their own interconnect in-house or employ NoC IP from a trusted third-party vendor.

Srivi Dhruvanarayan, VP of hardware engineering at SiMa.ai, has experience creating a NoC in-house at a previous company. In a recent case study, Srivi noted that it took six people working for almost two years to architect, design, and verify an in-house NoC. As a result of that experience, Srivi now uses third-party interconnect IP from Arteris.

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There's much more to a NoC than its NIUs, buffers, and switches. Remembering that NoC interconnects traverse the entire chip, it's necessary to include pipeline stages to meet timing. Suppose engineers are forced to insert these pipeline stages by hand. They typically overengineer the problem using too many stages, thereby using more silicon die area while increasing latency and power consumption.

The reason for this overengineering is that it takes much time and effort to iterate between the front-end design and the back-end physical layout. With advanced physically aware NoC IP, the product can insert an optimum number of pipeline stages and provide placement suggestions to the downstream physical layout tools. In addition to speeding the physical layout process, it significantly reduces the


number of time-consuming back-end to front-end iterations required to achieve timing closure.

Conclusion

Managing today's complex SoC designs mandates using one or multiple NoCs. A trusted and reliable de facto industry standard, like FlexNoC 5 interconnect IP from Arteris, helps save time, reduce risk, and speed completion time.

At the time of this writing, interconnect IP and system IP from Arteris have

been employed in 600+ SoC design starts. As a result, 3+ billion SoCs featuring this IP have shipped in electronic systems worldwide.

In the case of safety-critical designs for which functional safety (FuSa) is a concern, the FlexNoC resilience option complements FlexNoC 5 interconnect IP. The product implements the hardware reliability and FuSa features required for automotive ISO 26262 or IEC 61508 compliance, along with enhanced enterprise SSD endurance. 

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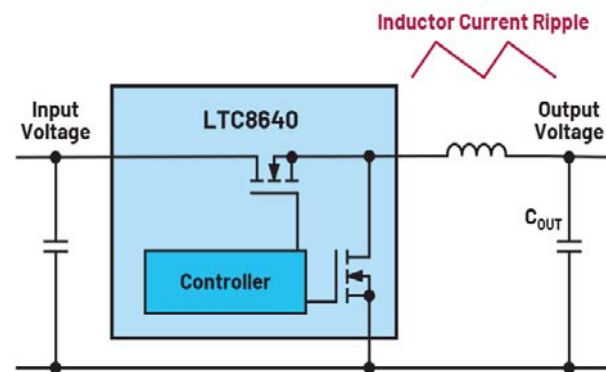
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Selecting the Right Inductor Current Ripple

How exactly is the correct inductance value chosen? Frederik Dostal looks at the considerations and what happens when selecting a current ripple that's too high or too low.

A switching regulator converts an input voltage to a higher or lower output voltage. For this, an inductor is used to store energy temporarily. The size of this inductor depends on the switching frequency of the switching regulator as well as the expected current flow through the circuit. How exactly is the correct inductance value selected? It can be done using a commonly used formula that contains the inductor current ripple.

In the datasheets for most switching regulators and in most application notes and other explanatory texts, an inductor current ripple of 30% during nominal load operation is given as a recommendation. This means that at the nominal load current, the inductor current peaks lie 15% above the average current and the inductor current valleys lie 15% below the average current. Why is this inductor current ripple, or current ripple ratio (CR), of 30% usually selected as a good compromise?



1. A buck converter with an inductor current ripple. Images courtesy Frederik Dostal

For a buck converter such as the one shown in *Figure 1*, Equation 1 applies:

$$L = \frac{V_{OUT} \times (1 - D) \times T}{CR \times I_{OUT}} \quad (1)$$

This equation calculates the required inductor value L for a buck converter based on the CR. This ratio is usually specified as 0.3, or 30%, peak-to-peak ripple. Here, D is the duty cycle and T is the cycle time, which depends on the respective switching frequency.

What Happens with Different Inductor Current Ripples?

Figure 2 shows the inductor current ripple of 30% in a circuit with an output current of 3 A (in red). This is the compromise that's usually selected in switching-regulator circuit designs. The waveform shown in blue has an inductor current ripple of 133%, and the waveform shown in green has an inductor current ripple of 7%.

Figure 3 illustrates what happens when the same circuit is operated with part of the nominal load as the output current, such as 1 A. At a high inductor current ripple, shown by the blue line in *Figure 3*, the energy in the inductor is completely discharged in every cycle. This mode is called discontinuous conduction mode (DCM). In this mode, the control-loop stability behavior changes and a higher output voltage ripple can occur.

A certain ripple current ratio is needed to avoid DCM. With a ripple current ratio of 30%, a good compromise is achieved. If the ripple current ratio is low, even at partial loads, the system is mainly operating in continuous-current conduction mode. The circuit can thus be optimized for operation in this mode.

What if the Selected Ripple Current Ratio is Too High?

At high ripple current ratios of greater than 30%, the inductor is smaller and thus cheaper. Unfortunately, the peak currents increase dramatically and generate more electromagnetic interference (EMI) than is absolutely necessary in a typical circuit. In addition, continuous conduction mode (CCM) can only be reached at higher load currents. This doesn't have to be a problem, but the operating behavior in this mode is changed and must be considered in the circuit design.


In addition, output-voltage ripple is higher than for a lower inductor current ripple.

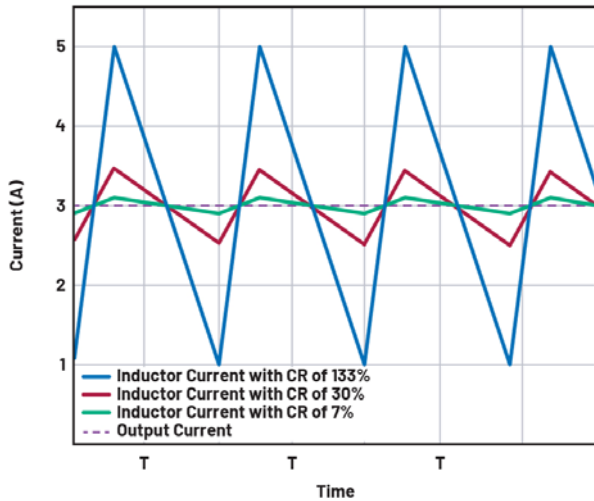
What are the Effects of Selecting a Ripple Current Ratio That's Too Low?

For low ripple current ratios of less than 30%, the inductor is large and accordingly expensive. The load transient response is also slower due to the large size of the energy-storage device.

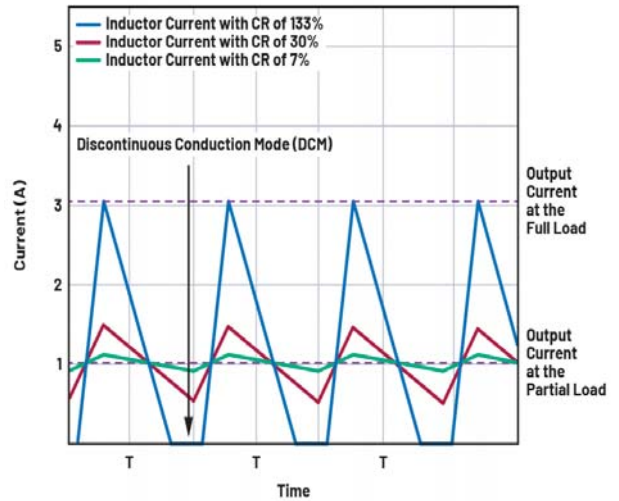
If, for example, a high load current is disconnected rapidly, the energy stored in the inductor has to go somewhere. This

increases the voltage across the output capacitor (C_{OUT}). The more energy in the inductor, the higher the output voltage excess. This excess voltage can damage the supplied circuit.

If the advantages and disadvantages of different inductor current ripple ratios are weighed, then values of around 30% seem to represent a good tradeoff for most applications. However, deviations are permissible in some cases as long as the resulting effects are acceptable. 



2. An inductor current ripple with a ripple current ratio of 30% shown in red, with a smaller inductor in blue, and with a large inductor in green at the nominal load.



3. An inductor current ripple with a ripple current ratio of 30% shown in red, with a small inductor in blue, and with a large inductor in green at the partial load.

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A Timer to Remember

Even in the age of MCUs, the NE555 remains useful decades after its inception.

NORMALLY I COVER a new product or technology in my Lab Bench section. However, since this is the last one to appear in a physical print issue, I thought I would look back at a technology that had a major impact on the electronics industry. I'm sure others will have their favorites, but one advantage of being the author of an article series like this one is I get to make the final decision.

My choice is the NE555 monostable multivibrator, often referred to as simply the 555 (Fig. 1). It has its own Wikipedia page and you can buy it from a number of sources. It comes in a variety of form factors (Fig. 2). One of our technology editors, Cabe Atwell, wrote a book about it: *Essential 555 IC: Design, Configure, and Create Clever Circuits*. It's probably the most often used device in our venerable Ideas for Design series. Cabe's article, "The Origin, Explanation, and Applications of Triple-Five Timers" (<https://electronicdesign.com/21252714>) provides a more detailed description of the 555.

What's so neat about the NE555 is that only a few external discrete components can make this little device do all sorts of things, from providing triggering to a clock. It can even be used in inductorless dc-dc converters.


Hans Camenzind designed the first one for Signetics back in 1971. Since then, we've had CMOS and bipolar versions. The 556 is a pair of 555 timers.

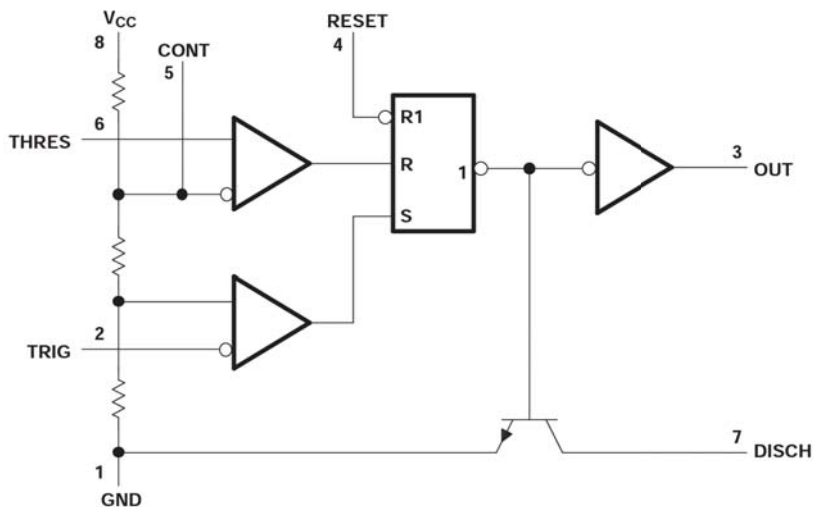
What stands out is the 555's longevity. It's equally applicable now even in the age of microcontrollers that fit in a similar package—though MCUs can do so much more, they require software to work. These days, a 32-bit Arm Cortex-M0+ might be the device of choice for timing applications that could be handled

by a 555. Hey, the microcontroller could even run a machine-learning model while it generates a clock.

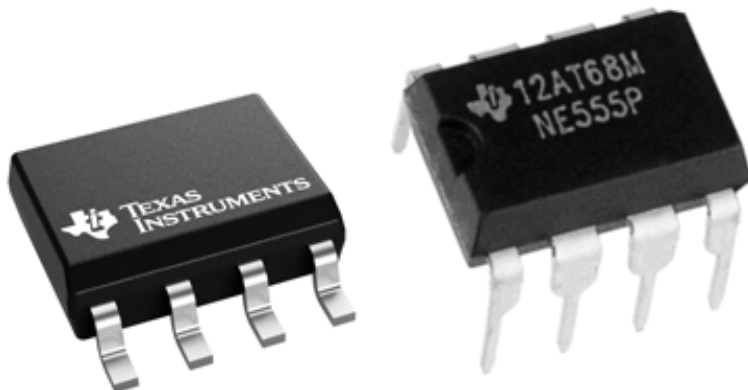
The 555 is one of those analog devices that's both useful and easy to understand. Hopefully it will keep the interest of a budding engineer or two who opt to take up analog design. Analog design crops up with power supplies and is really the basis for memories, micros, and more. How-

ever, we turn these into digital devices that put them into the realm of programmers. Not that I have anything against programmers, as I went to the dark, uh, digital, side long ago after playing with a 555 when they first came out (yes, I have been around that long).

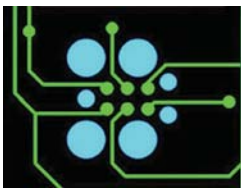
Our next issue will be all digital, so look for my next Lab Bench to hit on something new and different. 



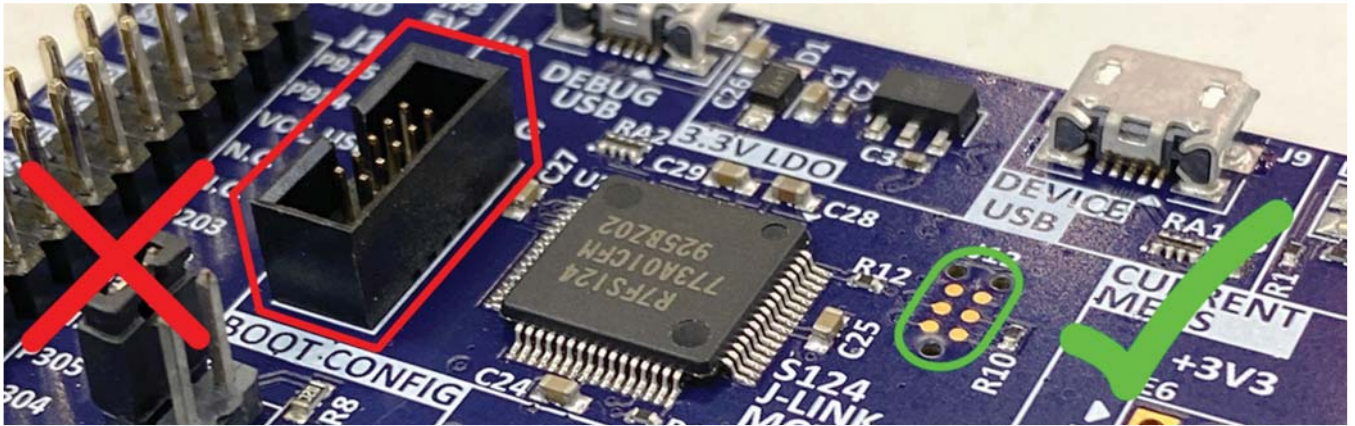
1. It's just an RS flip-flop, a transistor, and three op amps, but the NE555 can do so much with so little. Images courtesy Twexas Instruments



2. These are just two of the NE555's form factors.



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