Electronic Design

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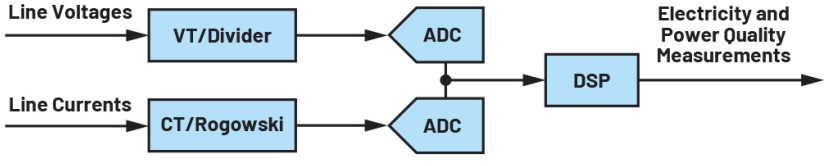
Power-Quality Monitoring (Part 2): Designing a Standards-Compliant Meter

This article discusses different solutions for designing a Class A and Class S power-quality meter, including a new Class S power-quality measurement integrated solution that significantly reduces the development time and costs.

The basic components of an instrument designed for power-quality measurement are shown in *Figure 1*. First, the current and voltage transducers must account for the operational range of the instrument and adapt the input signal to the dynamics of the analog-to-digital converter (ADC) input. Traditional transducers are the first source of uncertainty in the measurement. Therefore, correct selection is of great importance.

Next, the signal goes to an ADC. Its individual characteristics, such as offset, gain, and nonlinearity errors, create a second source of uncertainty. Selecting the correct ADC for this function is a demanding effort for designing a power-quality instrument. Lastly, a series of signal-processing algorithms must be produced to get electrical and power quality measurements from the input signals.



1. The main components of an instrument that handles power-quality measurements.

Table 1: Accuracy Requirements for Current, Voltage, and Power Measurements Specified by IEC 61000-4-7 Standard

Class	Measurement	Conditions	Maximum Error
A	Voltage	$U_M \geq 1\%\ U_{NOM}$	$\pm 5\%\ U_M$
		$U_M < 1\%\ U_{NOM}$	$\pm 0.05\%\ U_{NOM}$
	Current	$I_M \geq 3\%\ I_{NOM}$	$\pm 5\%\ I_M$
		$I_M < 3\%\ I_{NOM}$	$\pm 0.15\%\ I_{NOM}$
	Power	$P_M \geq 150$ W	$\pm 1\%\ P_M$
		$P_M < 150$ W	± 1.5 W
S	Voltage	$U_M \geq 3\%\ U_{NOM}$	$\pm 5\%\ U_M$
		$U_M < 3\%\ U_{NOM}$	$\pm 0.15\%\ U_{NOM}$
	Current	$I_M \geq 10\%\ I_{NOM}$	$\pm 5\%\ I_M$
		$I_M < 10\%\ I_{NOM}$	$\pm 0.15\%\ I_{NOM}$

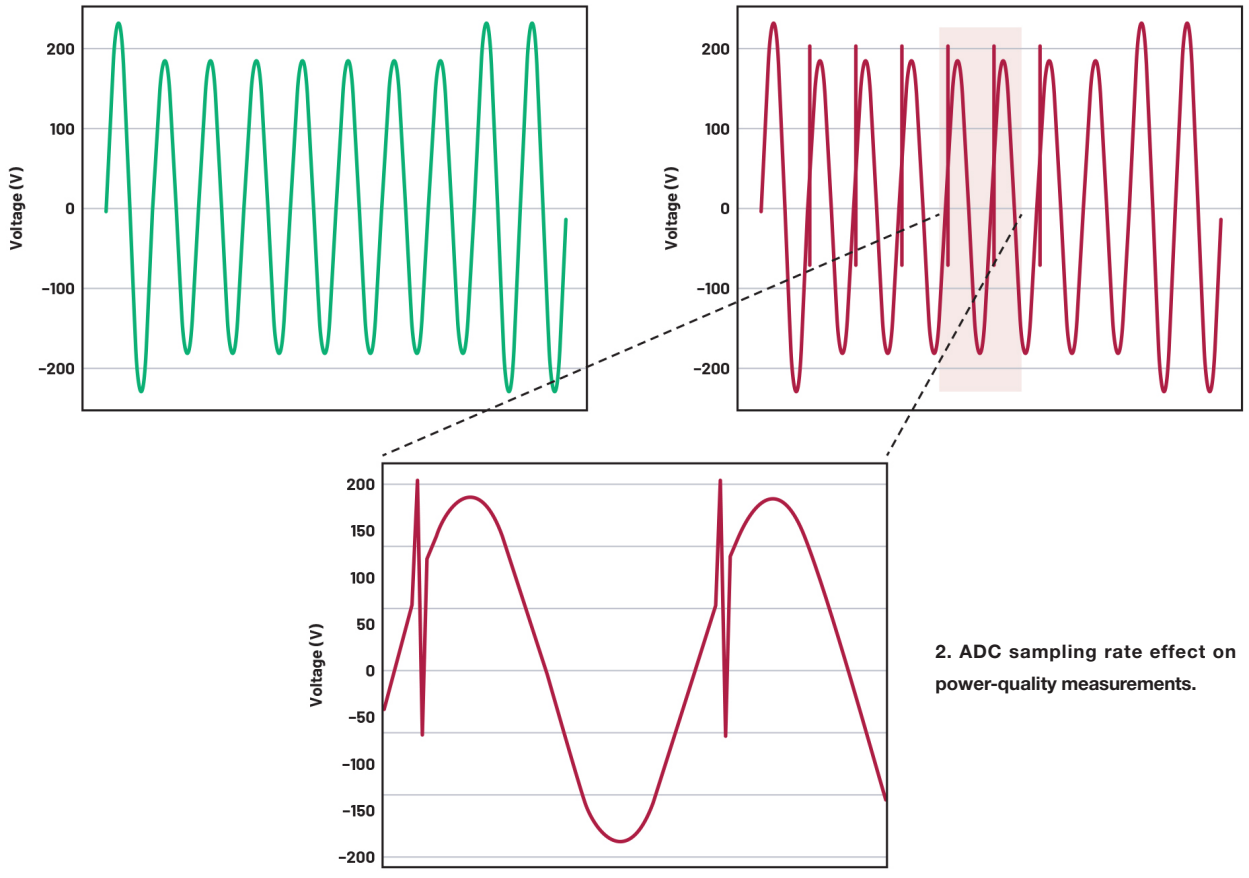
I_{NOM}: Nominal current range of the measurement instrument

U_{NOM}: Nominal voltage range of the measurement instrument

U_M, I_M, and P_M: Measured values

Voltage and Current Transducers

Depending on the location and application of the power-quality instrument, the nominal supply voltage (U_{NOM}), nominal current (I_{NOM}), and frequency varies. Independently of the nominal values measured by the instrument, the IEC 61000-4-7 standard requires power-quality measurement instruments to reach the accuracies presented in *Table 1*. Thus,



2. ADC sampling rate effect on power-quality measurements.

the transducers must be selected such that the instrument fulfills the accuracy requirements.

The IEC61000-4-7[1] standard recommends designing the input circuitry following these nominal voltages (U_{NOM}) and nominal currents (I_{NOM}):

- For 50-Hz systems: 66 V, 115 V, 230 V, 400 V, 690 V
- For 60-Hz systems: 69 V, 120 V, 240 V, 277 V, 347 V, 480 V, 600 V
- 0.1 A, 0.2 A, 0.5 A, 1 A, 2 A, 5 A, 10 A, 20 A, 50 A, 100 A

In addition, the transducers selected for measuring voltage and current must keep their characteristics and accuracy unchanged when a 1.2X U_{NOM} and I_{NOM} are applied continuously. A signal 4X the nominal voltage, or 1 kV rms, whichever is less, applied for one second to the instrument must not lead to any damage. Likewise, a 10X I_{NOM} current for one second shall not produce any damage.

Analog-to-Digital Converter

Even though the IEC 61000-4-30 standard doesn't specify a minimum requirement for sampling rate, the ADC must have enough sampling rate to measure some oscillatory and fast power-quality phenomena. An insufficient sampling rate could result in the misclassification of a power-quality event or the failure to detect one.

The IEC 61000-4-30 standard states that the instrument voltage and current sensors should be appropriate for up to 9 kHz. Thus, the sampling frequency of the ADC must be selected following the rules of signal analysis to perform a measurement of frequency components up to 9 kHz.

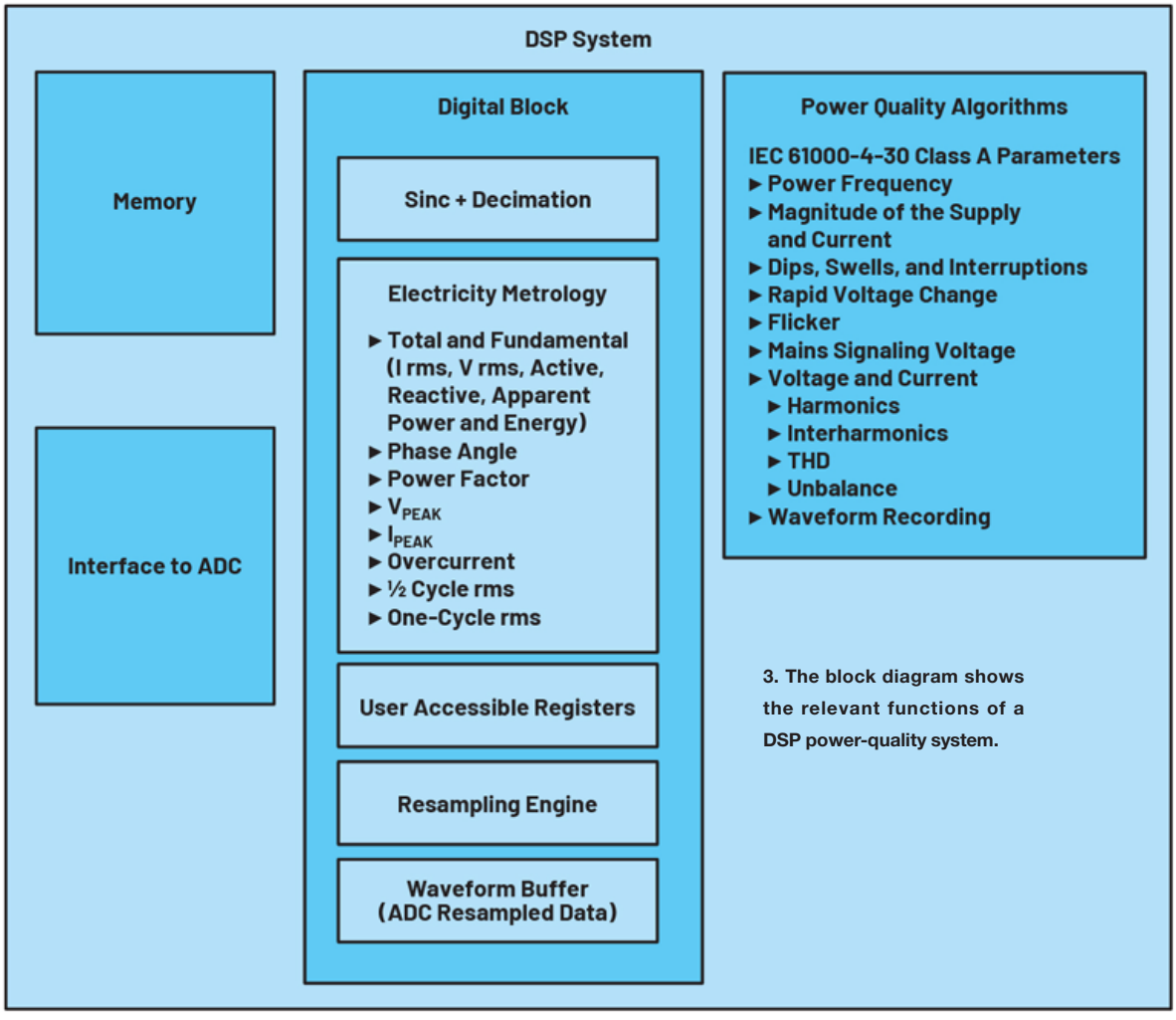
Figure 2 illustrates the consequences of when the sampling rate is insufficient. The top left waveform contains 64 samples per 10 cycles (200 ms) and the top right waveform has 1,024 samples per 10 cycles. The top left graph shows a voltage dip event while the top right graph reveals that the dip is transient induced.

The IEC standard applies to single- and three-phase systems. Therefore, the selected ADC must be able to sample the required number of voltage and current channels simultaneously. Having measurements for all of the voltage and current channels on the instrument at the same time makes it possible to examine all parameters and immediately trigger when a power-quality event occurs.

Digital Signal Processing (DSP)

Even though selecting the transducers and ADC for power-quality measurements requires a comprehensive engineering effort, developing the algorithms to process the raw ADC measurements is undoubtedly the task that demands most of the time and resources to make a power-quality instrument.

To implement a standard-compliant instrument, the right DSP hardware must be chosen and the algorithms to calculate the power-quality parameters from the waveform samples have to be developed and properly tested. The standard not only requires calculations, but also different time-depen-



3. The block diagram shows the relevant functions of a DSP power-quality system.

dent aggregations with time accuracies less than ±1 seconds per 24-hour period for Class A and ±5 seconds per 24-hour period for Class S. These algorithms must perform harmonic analysis.

In addition, power-quality parameters rely on fast Fourier transform (FFT) analysis (harmonics, interharmonics, mains signaling voltage, unbalance), which are challenging to implement. The FFT analysis requires the waveforms to be sampled at 1,024 samples per 200 ms (10 cycles) minimum. Performing resampling of the raw waveforms from the ADC to the required rate requires care to avoid harmonic distortion and aliasing.

After the algorithms are developed, the IEC standard requires a comprehensive list of more than 400 tests that the instrument must pass to be fully certified.

Figure 3 shows a block diagram with the most relevant functions that a DSP system needs to produce power-quality measurements.

Multichannel Simultaneous Sampling ADCs for IEC 61000-4-30 Class A

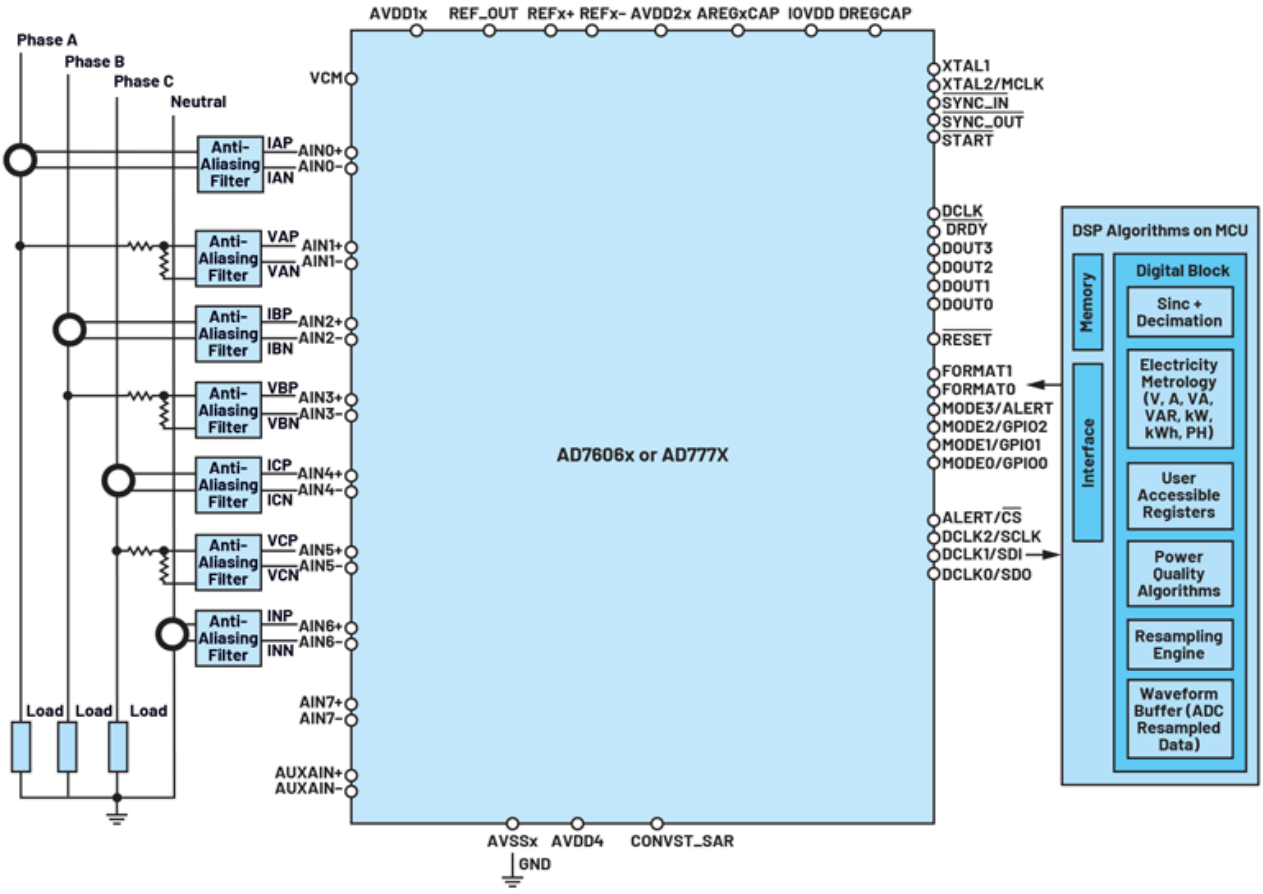
Considering the accuracy, number of channels, and sampling rate requirements to develop a Class A PQ instrument, Analog Devices' AD777x and AD7606x family of products are recommended for the ADC conversion of the signal chain/system. Note that these solutions provide just the raw digitized data from the input signals. A DSP system must be developed to get certified PQ measurements.

AD777x Sigma-Delta ADC

The AD777x is an 8-channel, 24-bit simultaneous sampling ADC family of devices. Eight full sigma-delta (Σ-Δ) ADCs are on-chip, providing sampling rates of 16/32/128 ksamples/s. The AD777x maintains a low input current that allows for direct sensor connection. Each input channel has a programmable gain stage, enabling gains of 1, 2, 4, and 8 to map lower amplitude sensor outputs into the full-scale ADC input range, maximizing the dynamic range of the signal chain.

The AD777x accepts a V_{REF} voltage from 1 V up to 3.6 V and analog input range: 0 to 2.5 V or ±1.25 V. The analog inputs can be configured to accept true differential, pseudo differential, or single-ended signals to match different sensor output configurations. A sample-rate converter is provided to allow for fine resolution control over the AD7770. It can be used in applications where the ODR resolution is required to maintain coherency with 0.01-Hz changes in the line frequency.

In addition, the AD777x provides large signal input band-



4. A power-quality three-phase applications system diagram for the AD777X and AD7606x families of ADCs.

width of 5 kHz (AD7771, 10 kHz). A data output and SPI communications interfaces are incorporated, although the SPI can also be configured to output the sigma-delta conversion data. Temperature range is from −40 to +105°C, functional up to +125°C with a power supply of 3.3 or ±1.65 V.

Figure 4 shows a three-phase typical applications system diagram for the AD777x family of ADCs involving a PQ instrument that uses current transformers as current transducers and resistor dividers for voltage.

AD7606x 16-/18-Bit ADC Data-Acquisition System

The AD7606x provides a 16-/18-bit, simultaneous sampling, analog-to-digital data-acquisition system (DAS) with eight channels. Each channel contains analog input clamp protection, a programmable gain amplifier (PGA), a low-pass filter, and a 16-/18-bit successive-approximation-register (SAR) ADC. The AD7606x also incorporates a flexible digital filter; low-drift, 2.5-V precision reference and reference buffer to drive the ADC; and flexible parallel and serial interfaces.

The AD7606B operates from a single 5-V supply and accommodates ±10-, ±5-, and ±2.5-V true bipolar input ranges when sampling at throughput rates of 800 ksample/s (AD7606B)/1 Msample/s (AD7606C) for all channels. The input clamp protection tolerates different voltages with user-selectable analog input ranges (±20, ±12.5, ±10, ±5, and ±2.5 V).

The AD7606x requires a single 5-V analog supply. The single-supply operation, on-chip filtering, and high input impedance eliminate the need for external driver op amps, which require bipolar supplies.

In software mode, the following features are available:

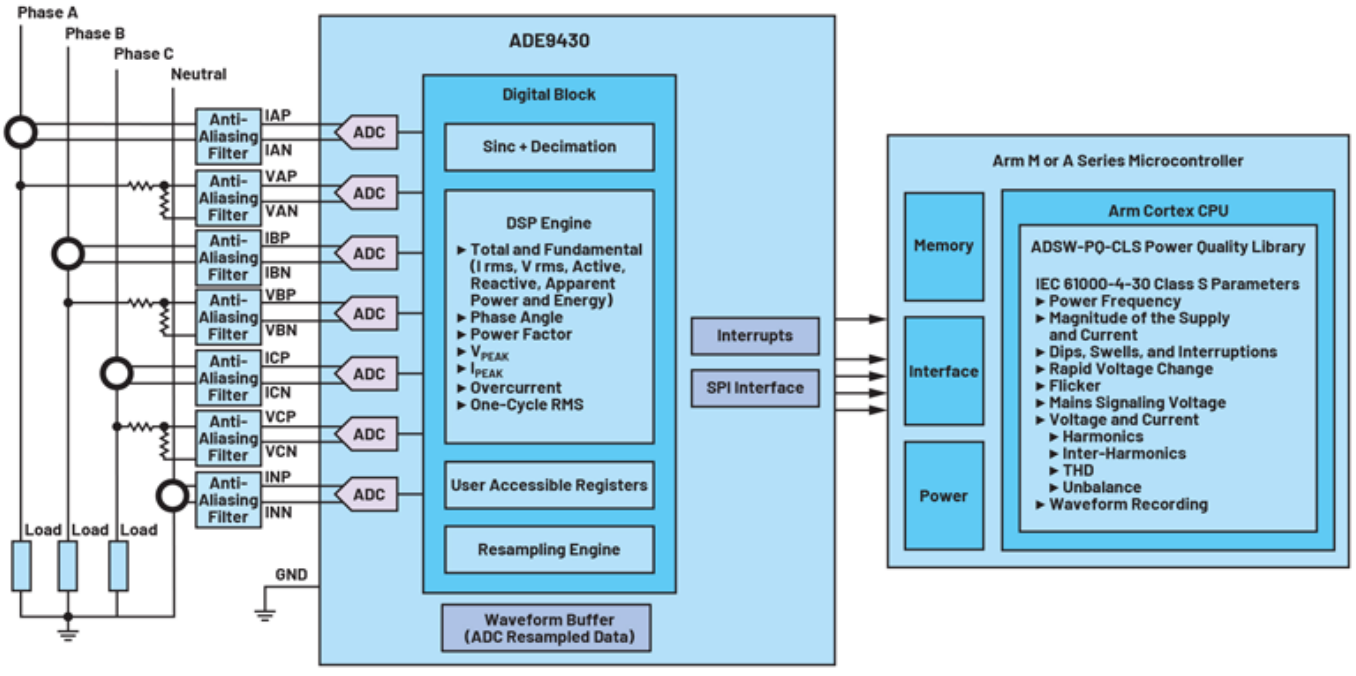
- Additional oversampling (OS) options, up to OS × 256
- System gain, system offset, and system phase calibration per channel
- Analog input open-circuit detector
- Diagnostic multiplexer
- Monitoring functions: SPI invalid read/write, cyclic redundancy check (CRC), overvoltage and undervoltage events, busy stuck monitor, and reset detection

Figure 4 shows a three-phase typical applications system diagram for the AD7606x ADCs for a power-quality instrument using current transformers as current transducers and resistor dividers for voltage.

Precertified IEC Class S Power-Quality Solution

The ADE9430, a fully integrated, polyphase energy-metering IC combined with the ADSW-PQ-CLS software library running on a host microcontroller, is IEC 61000-4-30 Class S standard compliant. This integration helps reduce the development time and costs for PQ monitoring products.

The ADE9430 + ADSW-PQ-CLS solution simplifies the



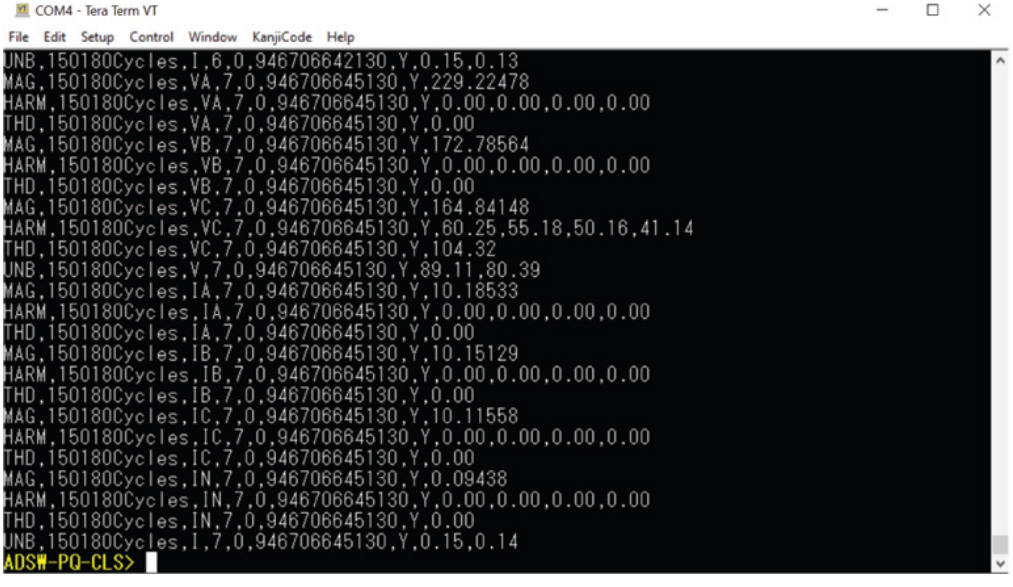
5. An ADE9430 and ADSW-PQ-CLS PQ three-phase system diagram.

implementation and certification of energy and PQ monitoring systems by providing a tight integration of acquisition and calculation engines. *Figure 5* shows a three-phase applications system diagram for the solution for a power-quality instrument that uses current transformers as current transducers and resistor dividers for voltage.

ADE9430 Class S Power-Quality Analog Front End

With seven input channels, the ADE9430 can be used on a three-phase system or up to three single-phase systems. Supporting current transformers or Rogowski coils with an external analog integrator for current measurements, it provides an integrated analog front end for power-quality monitoring and energy measurement. The ADE9430 is pin-compatible with the ADE9000 and ADE9078 with equivalent analog and metrology performance. Features include:

- Seven high-performance 24-bit sigma-delta ADCs
- 101-dB SNR
- Wide input-voltage range: ±1 V, 707 mV rms, full-scale at gain = 1
- Differential inputs
- Class 0.2 accuracy metrology
- One-cycle rms, line frequency, zero crossing, advanced metrology
- Waveform buffer
- Continuous resampled data: 1024 points per 10/12 line cycle
- Metrology covering 50- and 60-Hz fundamental frequencies
- Support of active energy standards: IEC 62053-21 and



6. Shown is the ADSW-PQ-CLS software library serial CLI interface.

Table 2: Energy and Power-Quality Features of the Class S ADE9xxx Energy-Metering ICs

Parameter	ADE9078 Utility Metering	ADE9000 Power Quality	ADE9430 + ADSW-PQ-CLS
Watt, watt-hr	✓	✓	✓
I rms, V rms, VA, VA-hr	✓	✓	✓
Total VAR, VAR-hr	✓	✓	✓
Fundamental VAR, VAR-hr	✓	✓	✓
Power factor	✓	✓	✓
Current phase angle	✓	✓	✓
Voltage phase angle	✓	✓	✓
Line frequency–three	✓	✓	Class S
Phase sequence detection	✓	✓	✓
1/2 cycle rms	—	✓	—
1 cycle rms	—	✓	Class S
10/12 cycle rms	—	✓	Class S
150/180 cycle rms	—	—	Class S
Dip/swell	—	✓	Class S
Interruptions	—	—	Class S
Overcurrent	—	✓	✓
Fundamental watt, watt-hr, VA, VA-hr	—	✓	✓
Rapid voltage change	—	—	Class S
Over/under deviation	—	—	Class S
Flicker	—	—	Class S
Voltage/current unbalance	—	—	Class S
Voltage/current harmonics, interharmonics	—	—	Class S up to 40th
ITHD, VTHD	—	✓	Class S

IEC 62053-22; EN 50470-3 OIML R46; and ANSI C12.20

- Support of reactive energy standards: IEC 62053-23, IEC 62053-24
- A high-speed communication port: 20-MHz serial port interface (SPI)

ADSW-PQ-CLS Software Library

The ADSW-PQ-CLS software library is designed specifically to be integrated with the ADE9430 to generate standard-compliant IEC 61000-4-30 Class S PQ measurements. It implements all parameters defined in IEC 61000-4-30 for Class S instruments. Users can decide which PQ parameters to use.

This library needs low CPU/RAM resources and is core/OS agnostic (Arm Cortex-M minimum). Supported MCU architectures include Arm Cortex-M0, Cortex-MO+, Cortex-M1, Cortex-M3, and Cortex-M4. For distribution to end users, the library is provided as a CMSIS-PACK file (.pack) compatible with Keil Microvision, IAR Embedded Workbench version 8.x, or Analog Devices CrossCore Embedded Studio. The license for the software library is included with the purchase of the ADE9430.

A PC serial command line interface (CLI) example is provided to evaluate the library and its features. *Figure 6* shows how PQ parameters are displayed by this CLI.

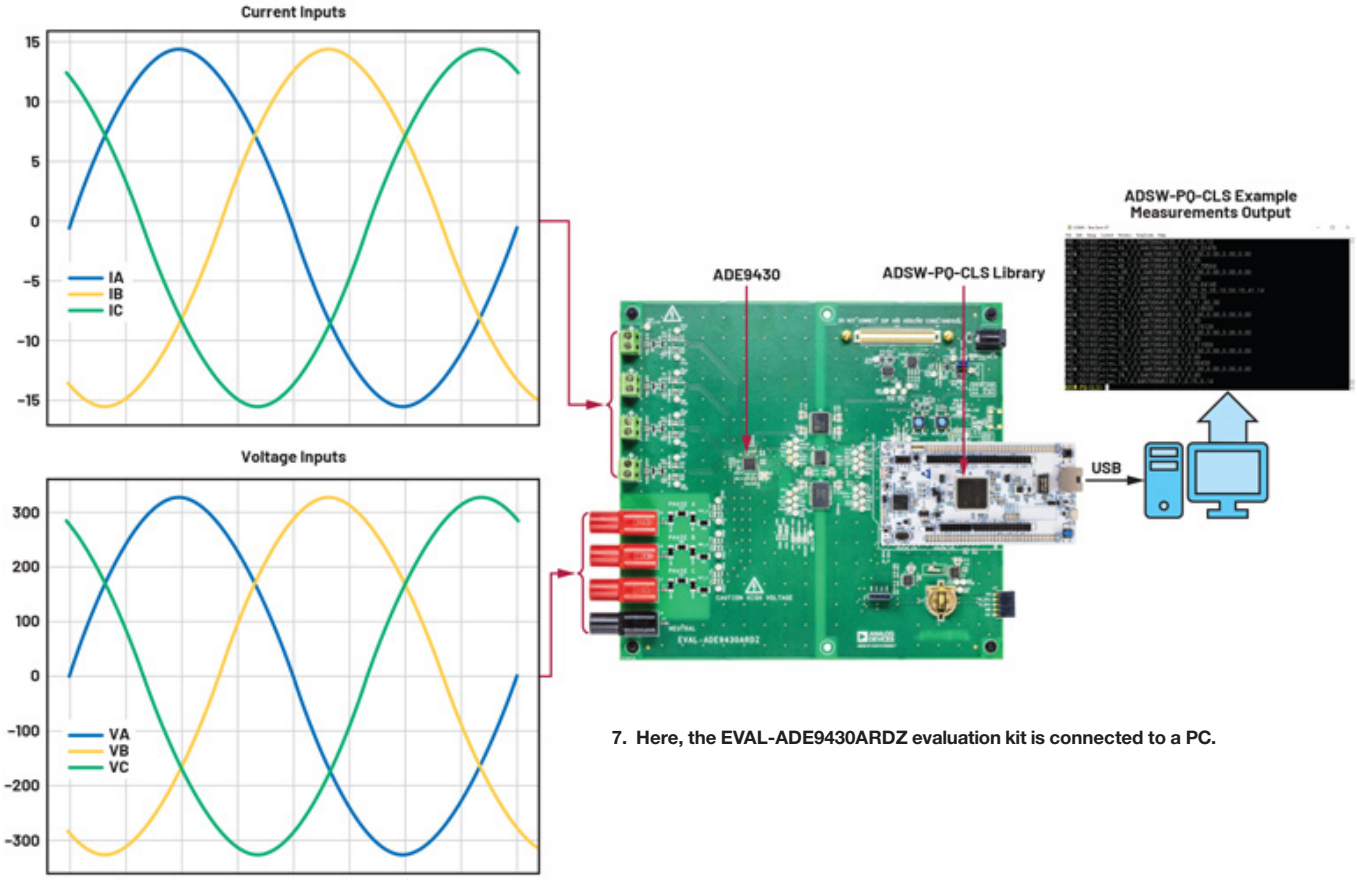
Table 2 runs down the power-quality and energy features of the ADE9xxx energy-metering ICs compliant with IEC 61000-4-30, Class S.

ADE9430 Evaluation Kit

The EVAL-ADE9430ARDZ enables quick evaluation and prototyping of energy and Class S power-quality measurement systems with the ADE9430 and the ADSW-PQ-CLS Power Quality Library. The power-quality library and application example are provided to simplify implementation of larger systems. This kit provides a plug-and-play type of experience that's easy to use to test the power-quality parameters of a three-phase electrical system.

The kit's hardware includes:

- Current transformer inputs
- High-voltage/current inputs
- 240 V rms nominal (with potential divider)
- 80 A rms max (with provided current-transformer sensors)



7. Here, the EVAL-ADE9430ARDZ evaluation kit is connected to a PC.

- 2.5-kV isolation
- On-board RTC to timestamp measurements
- Precertified for IEC 61000-4-30 Class S (requires user to calibrate)
- ADSW-PQ-CLS library and example application running on Arm Cortex-M4 MCU
- Serial CLI to PC for configuration and logging of power-quality parameters

Figure 7 shows the connections required to use the EVAL-ADE9430ARDZ with a PC.

The EVAL-ADE9430ARDZ consists of a PCB with four current and three voltages + neutral input connectors and on-board ADE9430, isolators, a real-time clock, a Cortex-M4 STM NUCLEO-413ZH development board with an ex-ample application of the ADSW-PQ-CLS library, and three current sensors.

Conclusion

Designing a standards-compliant power-quality meter is a challenging task. To reduce the time and engineering resources needed to produce an IEC 61000-4-30 Class S standard-compliant PQ measurement instrument, the ADE9430 + ADSW-PQ-CLS offers designers a ready-to-use platform to accelerate development and solve for many critical design challenges.

Reference

1. IEC 61000-4-30:2015: Electromagnetic Compatibility (EMC)-Part 4-30: Testing and Measurement Techniques-Power Quality Measurement Methods." International Electrotechnical Commission, February 2015.