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GENERATIVE AI: The Engineering Unknown

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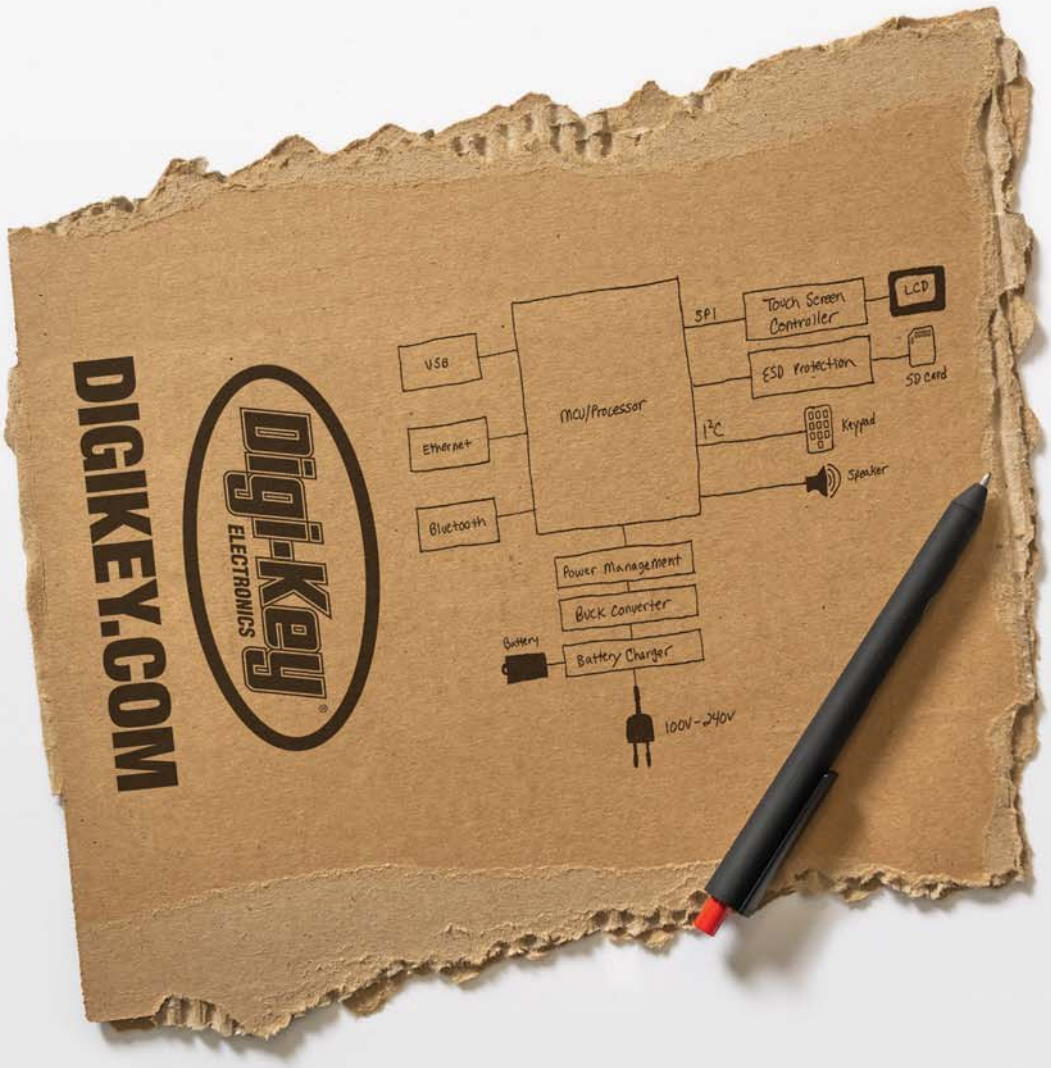

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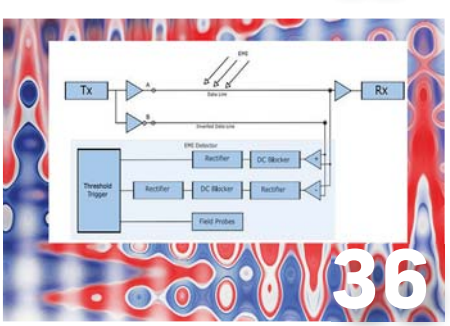

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ELECTRONIC DESIGN (USPS Permit 172-080), (ISSN 0013-4872 print, ISSN 1944-9550 online) is published quarterly (Spring, Summer, Fall, Winter) by Endeavor Business Media, LLC. 1233 Janesville Ave., Fort Atkinson, WI 53538. Periodical postage paid at Fort Atkinson, WI, and additional mailing offices. **POSTMASTER:** Send address changes to Electronic Design, PO Box 3257, Northbrook, IL 60065-3257. **SUBSCRIPTIONS:** Publisher reserves the right to reject non-qualified subscriptions. Subscription prices: U.S. ($75.00 per year); Canada/Mexico ($112.50 per year); All other countries ($150.00 per year). All subscriptions are payable in U.S. funds. Send subscription inquiries to Electronic Design, PO Box 3257, Northbrook, IL 60065-3257. Customer service can be reached toll-free at 877-382-9187 or at electronicdesign@omeda.com for magazine subscription assistance or questions.

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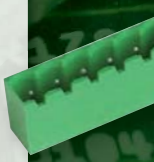

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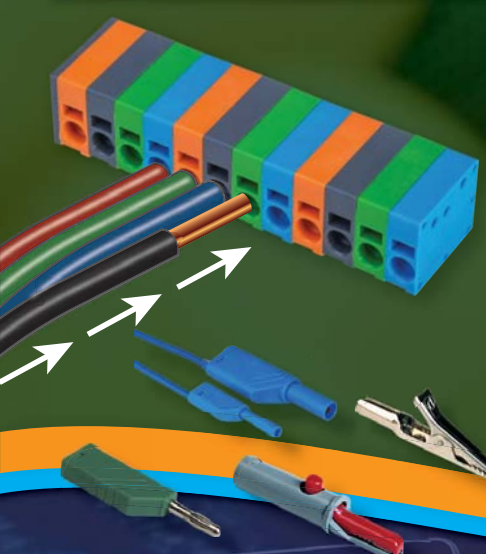

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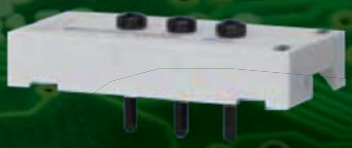

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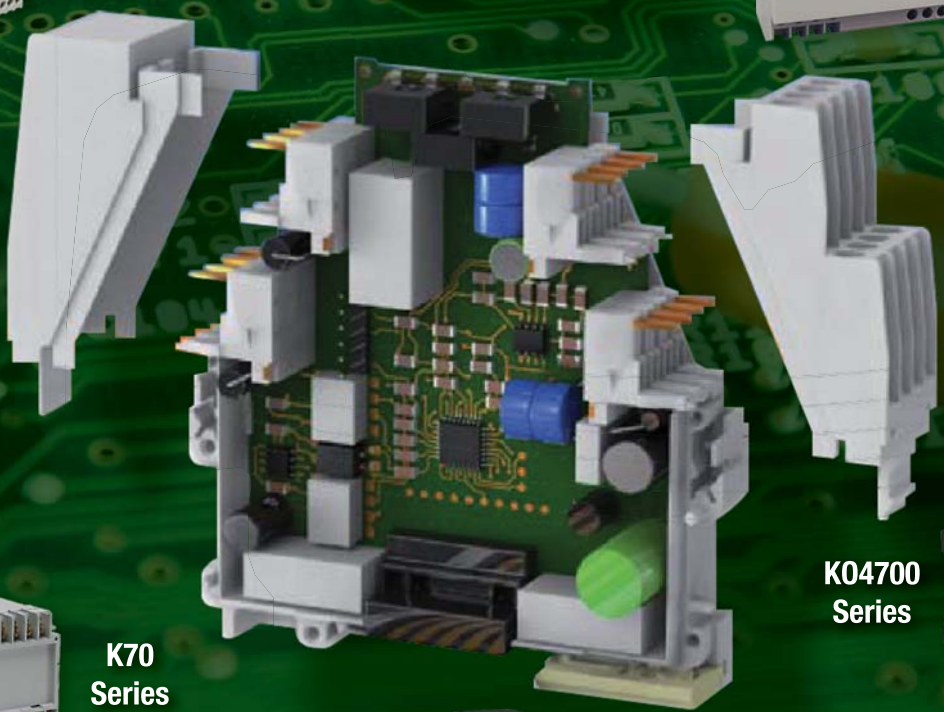

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Editorial

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Engineers Must Contend with **Generative AI**

Whether we like it or not, we need to deal with all sorts of machine-learning models, including generative AI.

IT SEEMS THAT artificial intelligence and machine learning (AI/ML) is becoming as ubiquitous as the internet. Even the U.S. Congress is talking about it, or at least around it. Bad actors use AI/ML to create more nefarious attacks while companies are incorporating it into their products and algorithms. People utilize it daily and often unknowingly to crop someone out of a photo or when searching for someplace to eat.

Much of what AI/ML does these days is improve on tasks that are performed daily, but faster and often better. The photo of my aquarium has two added fish *(see figure)*. One was from another photograph while the other was created using generative AI. Do you know which is which? I used the open-source Gimp image editor to create the final photo so that the two Siamese Fighting fish stand out. However, I could have done more to make them blend in or even used AI tools to accomplish that.

This type of graphic manipulation is only the tip of the iceberg, but one that almost anyone can use. The other tools garnering major interest are chatbots like OpenAI's ChatGPT and Google's Bard. A number of issues have arisen from the source of training material for these large-language-model (LLM) tools regarding bias and explainability. There are also discussions about legal, moral, and liability issues when it comes to using any output associated with these tools.

These days, we at *Electronic Design* are making sure we annotate the source of our images. However, that's not the case for many websites. Likewise, we're not using generative AI to create articles as some sites are doing. Some of those sites indicate when AI is utilized, though not always, and do you even care?

Engineers may be able to overlook these issues if it were limited to images, videos, and text, but the basic AI/ML technologies are part of the software we use to create applications and products from chips to software. Eventually, these aspects of the tool will not be something that can be avoided as these models and technologies are intimately included within the tool.

The technology in general has the potential to vastly improve the output and capabilities of engineers and programmers. Nevertheless, like the rise of security tools and technologies, taking advantage of AI/ML will require a better understanding of the capabilities and liabilities of AI/ML-based tools. Stay tuned for more on this subject. ed

The background is a photograph of my aquarium, but one of the two Siamese Fighting fish is AI-generated while the other is a from a photograph. *William Wong, AI Yupiramos Group – Dreamstime, Utalert - Dreamstime*

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WILLIAM G. WONG | Senior Content Director

Lions, Chatbots, and Generative AI, Oh My

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The population at large is enamored—and worried—about generative AI. Are you?

The challenge with artificial intelligence (AI) since its inception has been one of hyperbole versus actuality. AI in literature abounds with things like Asimov's three laws of robotics and positronic brains. Androids and intelligent machines were once stuff of science fiction, but these days we at least to appear to have this capability.

For instance, we have Working Dog[Bot]s that can operate autonomously. The Ghost Robotics Vision 60 quadruped robot can climb stairs and even slide across ice. It's able to recognize objects and knows how to find the charger when its battery runs low.

There are humanoid robots that can converse in multiple languages while maintaining eye contact. We have smart speakers that can answer questions and pull from a massive cache of data to let you know what time it is in Marrakesh.

The problem is that we are still light years away from anything close to an android like Data from *Star Trek: The Next Generation* or C3PO from *Star Wars*. This isn't to say we couldn't build something that closely resembles those androids, but the result is rather disappointing once you try to challenge them with even simple tasks.

Worrying About Generative AI

Machine learning (ML) is a subset of AI, although many use the terms interchangeably. I do, often to the chagrin of readers. ML tools cover a lot of ground, and different machine-learning models and methodologies have been created to address a host of different tasks. Models that work well to identify things in images don't necessarily work well when it comes to understanding the spoken word.

Utilization of focused ML models has changed the way we look at visual problems like advanced driver-assistance systems (ADAS), self-driving cars, and autonomous robots. Recognizing objects in real-time and providing this type of information is relatively simple these days. However, acting on that information is a bit more of a challenge, though it's being addressed albeit with different models and approaches.

Generative AI is one of these approaches. Generative pre-trained transformer (GPT) models are also referred to as large language models (LLMs). They're collectively known as chatbots, one of which is the well-known ChatGPT.

The approach can be used for many applications, but those of note tend to be based on very large data sets, often scraped from the internet, that can interact with queries posted by users. They provide a similar interactive interface that harkens back to the ELIZA computer therapist computer program created by Joseph Weizenbaum from MIT back in the 1960s. It didn't use a GPT model but rather a ruleset.

ELIZA garnered lots of interest due to its interactive nature and it could be convincing, to a point. Chatbots today are more effective and have a better understanding of some of the material they're trained with, but only within the limits of the model and training. The results from interacting with programs like ChatGPT range from insightful to silly.

Keep in mind that chatbot applications these days are doing quite a bit, from per-

forming natural language processing of input, to analyzing a request, to finding and forming a response and presenting it in a natural language format. It would be trivial to make this work with audio inputs and outputs, which would wow some users. From a technical standpoint, though, it's just a design exercise.

Jobs at Risk?

The more focused the application, training, training data, and models, the better the results. One worry carried by many is that a suitable training model could replace them. It could be anyone from a programmer to a tech support specialist to a bond trader.

It's not just generative AI that's at issue when considering whether to worry about AI taking over the world. Many "AI applications" are actually collections of different models, tools, and regular programming that perform a job. This might involve creating a new music score or software program, or handling an order for burgers and fries. The thing is that someone helped develop the application and used AI-related tools to create the application or incorporated the AI support into it to make it work.

Those creating the application tend to have an understanding about AI that ranges from minimal to expert level, but at the least, they understand the limits and capabilities of the system. Users and managers often have a much different view and understanding of these limits and capabilities and their potential impact.

I tend to be much more worried about the human side of the equation when it comes to utilization and deployment of AI tools and models due to the lack of understanding of those simply using a tool or application. It's akin to the meme "It's on the internet, so it must be true."

Unfortunately, most AI is not analogous to a calculator that will always provide a correct answer to a basic problem, like adding numbers. AI usually is related more to statistics, and we know how well most people understand statistics.

Fact or Fiction?

The challenge is that many will wind up using tools for less than noble reasons. The ability to generate a paper on a topic or create an image or video by specifying incorrect facts can result in data like a video that's completely false or skewed far from the truth. In fact, ML models are often used for optimization—optimizing for a lie works as well as optimizing for the truth.

There seems to a great deal of worry surrounding the misuse of AI technology, and that we should somehow slow down research in this area. I contend that the problem of people using the technology is at issue rather than the technology itself.

Creating videos of events that didn't occur is what most movies are all about. Writing stories that are fiction is the norm. The ability to do these things in the past was possible, but it was typically time-consuming and often required a level of expertise that would be beyond most people. Generative AI tools have simply lowered the bar of entry while drastically improving the quality of the results.

Not only are these tools being made available on a regular basis. but they're on platforms like smartphones. Editing someone out of a picture or adding someone else is now a tap or two away.

Taking Advantage of Generative AI

I regularly receive press releases about new products touting the fact that they utilize or present ML tech, especially generative AI or chatbots. This isn't surprising given the hype. However, it's also about the capabilities of these tools, since it's not just smoke and mirrors. Generative AI can be very useful and augment the users' use of an application or improve how the application works.

From a developer's perspective, the how and why become important. For example, can an interactive chatbot improve areas of a particular application? General help support comes to mind, but a host of other features could be readily apparent, from reducing the number of options presented to the user to finding possible solutions within a large list of possibilities (e.g., finding the right transistor or chip for a particular task).

Keep in mind that one needn't utilize generative AI tools or application support if it's not warranted. However, taking a new look at your development process or application with a better understanding of what's possible may be very worthwhile.

There are multiple areas in which a developer may find ML useful. These include application development, design, implementation, delivery, tech and user support, as well as long-term maintenance. Much of this tends to be application-specific, although the development and design is often more standard and utilizes third-party tools.

Incorporating ML into an application or its support requires a much better understanding of the ML support that's available. GPT may not be a good choice, but other ML models and tools might be better options.

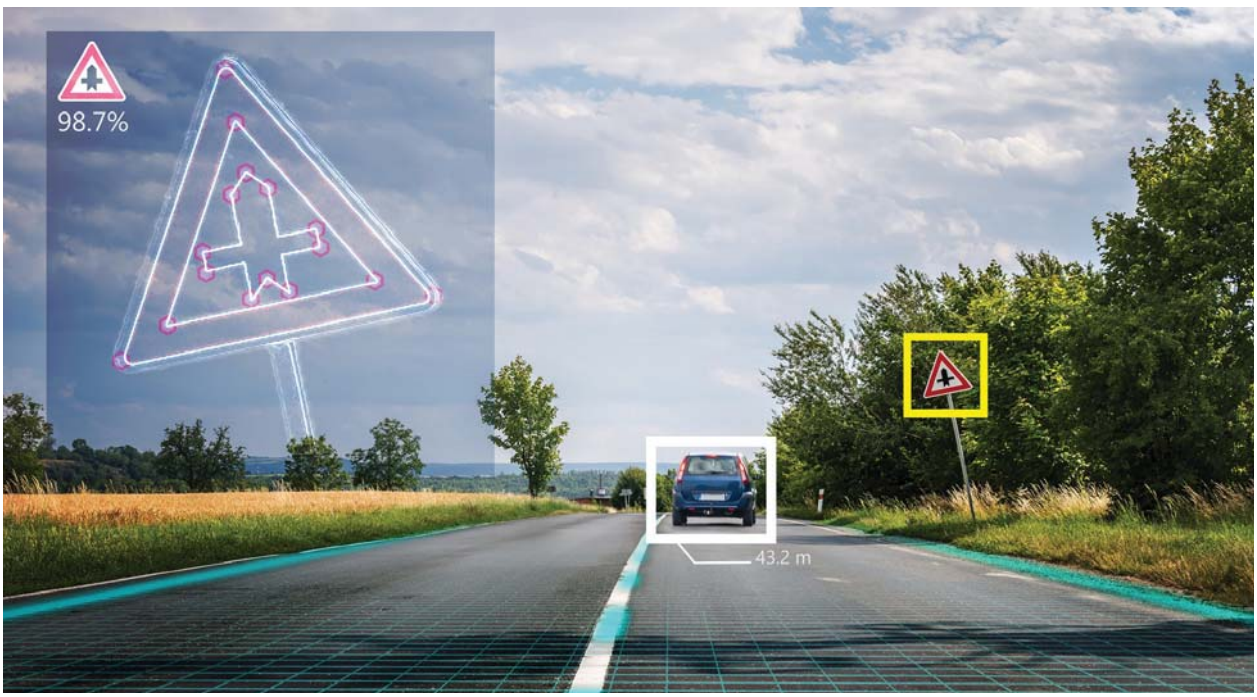
Other significant costs are involved as well, from startup, to training of developers, to training of models that come into play. These can be justified if they improve the quality or functionality of the development process or application. If not, they may be a gold ring that's not worth wearing.

Developers need to keep in mind not only the possibilities that tools like GPT can provide, but also the potential limitations. For example, what will be the false positive and negative rates? Will they be significant? Will a customer be faulted, hurt, etc. because of results that might be subpar? Is there sufficient training data? Will training be an ongoing process? How will using ML and GPT affect support and security? How will the system be tested and verified?

The latter brings into play details like explainability, the ability for an ML model/system to provide a description of the results, how they were arrived at, and how they're justified.

P.S. I still haven't figured out how to get a lion into the article so that I could use it in the title. Guess I should have asked a chatbot. ED

GIL ABRAHAM | Business Development Director and Product Marketing, CEVA Artificial Intelligence and Vision



Explainable AI for Anomaly Detection

Explainable AI (XAI) can improve safety, security, and the overall user experience in IoT applications.

Anomaly detection is the process of identifying when something deviates from the usual and expected. If an anomaly can be detected early enough, relevant corrective action can be taken to avoid serious consequences. As children, we have played the game of who can identify the oddities in a cleverly composed picture. This is anomaly detection at play.

Engineers, scientists, and technologists have historically counted on anomaly detection to prevent industrial accidents, stop financial fraud, intervene early to address health risks, etc. Traditionally, anomaly-detection systems have relied on statistical techniques, predefined rules, and/or human expertise. But these approaches have their limitations in terms of scalability, adaptability, and accuracy.

The number of real-life, high-value use cases for AI anomaly detection have grown a lot over the years and are expected to continue to rise. Advances in artificial intelligence (AI) are revolutionizing the field of anomaly detection. The result is improved accuracy, faster detection, reduced false positives, scalability, and cost-effectiveness. This article will identify what's needed to implement such solutions and will touch on some use cases for illustrative purposes.

These days, many of the anomalies we come across may not be just happenstance but rather human-created with malicious intent. For example, social media is rife with images and videos that are fake and deepfake. Advanced graphics and video production and manipulation technologies have made this possible. Let's take a simple example and play the game of spotting the oddities on a modern day picture that was found on social media.

Study the *figure* (p. 11) and carefully and note down things that are anomalous.

Will traditional techniques for AI anomaly detection work on this picture? Maybe. One's knowledge of the place referenced in the caption, common sense, knowledge of physics principles, practicality perspective, etc., could help identify the anomalies in the picture. Based on that, one could declare the picture to be genuine or fakery.

However, that's not enough for others to believe your conclusion. You need to be able to explain how you came to that conclusion. This is the explainability part and it's essential.

What is Explainable Artificial Intelligence (XAI)?

XAI is a subset of AI that emphasizes the transparency and interpretability of machine-learning models. With XAI, the output or decision of the AI model can be explained and understood by humans, making it easier to trust and utilize the results.

Anomaly detection using XAI can help identify and understand the cause of anomalies, leading to better countermeasure decision-making and improved system performance. The key benefits of XAI for anomaly detection are its ability to handle complex datasets, improve accuracy, and reduce false positives and false negatives.

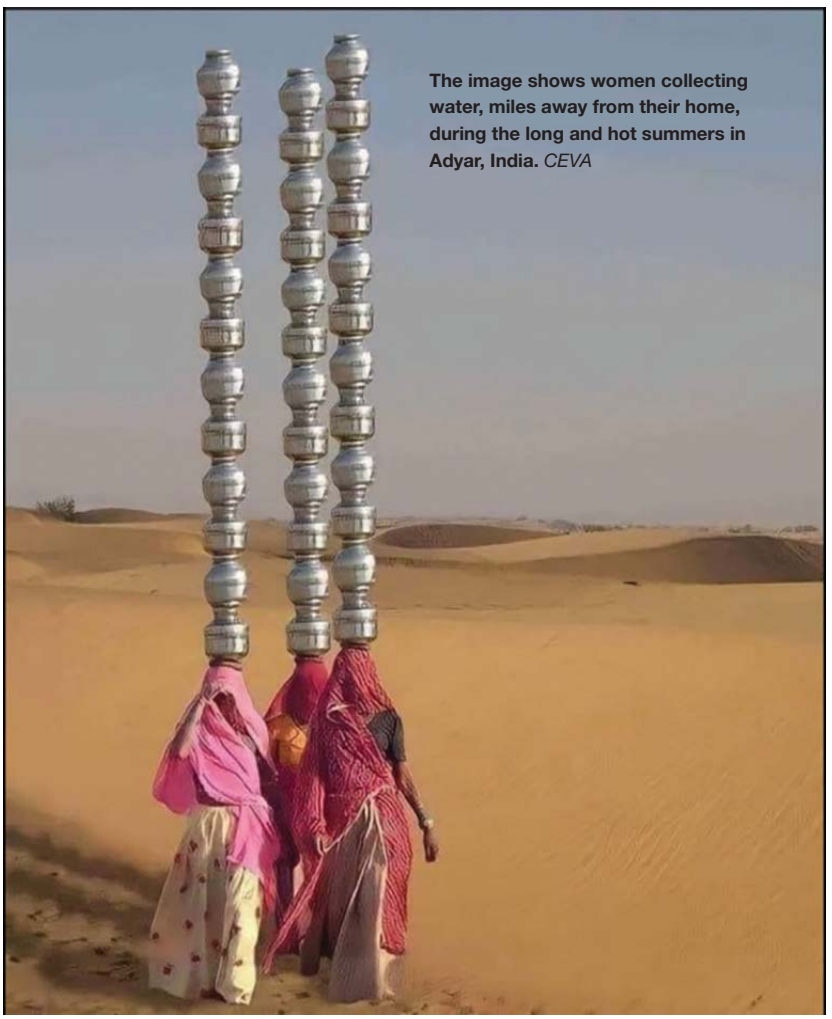
What are the Different Use Cases for XAI?

AI anomaly-detection systems may make decisions that have significant impacts on individuals and the social collective at large. Many use cases are on the edge AI applications that relate to security, safety, production-line longevity, and customer-friendly service.

Furthermore, bottom-line decisions without reasoning are somewhat useless for use cases that will penetrate the judicial system and medical prognosis services in the future. XAI provides a way for systems to illustrate the decision-making process, as well as learn and continually improve for the benefit of industry and society.

Use Case: Access Control (Facial Recognition)

Authentication by facial-recognition applications is widely used for access control purposes and relies on computer vision and AI. While a system may be very good at detecting faces, many unexpected factors may cause the system to fail to recognize a face.



The image shows women collecting water, miles away from their home, during the long and hot summers in Adyar, India. *CEVA*

Given the purpose of this application, it's tuned to prevent false-positives and alert if a malicious breaching attempt is taking place. But for a user who knows that his face should be recognized, it's very annoying to say the least. Perhaps the application was running into difficulty near the mouth area or around the eyes. XAI can communicate accordingly so the user can retry after removing the mask or the glasses.

AI systems are learning-oriented and count on feedback for continual improvements to their algorithms. The system may be able to improve itself and recognize this user the next time around, even with partial occlusion of the face. On the other hand, XAI is enabling the system to distinguish at all times between recognition failure and intentional breaching attempt and alert accordingly.

Use Case: Autonomous Driving TSR (Traffic Signs Recognition)

Autonomous driving uses computer vision and AI to recognize speed limits and act accordingly. What if a malicious actor or natural deterioration were to alter a sign to change it from say 60 mph to 600 mph or to 80 mph? This use case can be more challenging than the facial-recognition case.

The 600-mph sign could be easily ignored as a tampered sign as no road-based vehicle of current times can even come close to 600 mph. But the 80-mph sign is easily achievable by many vehicles and it's a legitimate speed limit in many places on many roads.

However, if the sign was fake, acting accordingly may not only be illegal, but also dangerous due to special road conditions. XAI could determine the validity of a sign, provide a probability level to the conclusion, and explain how that was arrived at. The autonomous-vehicle system could then take a safe action based on that input.

Use Case: Monitoring the Health of a Factory Machine

A factory machine that stops working unexpectedly and abruptly could be economically very expensive for a business. To avoid such a situation, sensors placed in the machine would continuously monitor the sounds emanating from the machine and run AI network models to analyze and detect abnormalities.

If out-of-order sounds or irregular frequencies are detected, which may lead to mechanical problems, the technician would be alerted to take preventative action before an abrupt breakdown of the machine.

Futuristic Use Case: Enabling Legal Hearings and Sentencing

There's talk about using AI to analyze legal cases and issue verdicts. By analyzing legal documents and historical data, AI can identify anomalies in the data that may be relevant to the case.

With human judges, the most important aspect is the reasoning found in the opinion piece written after the case has been heard. By using XAI, the system can explain the anomalies identified, which can lead to better decision-making and improved overall system performance. For example, the use of XAI can help to identify the reasons why a particular legal precedent wasn't used in a case.

What are the Tech Requirements for Implementing XAI?

Most XAI-driven anomaly-detection use cases require excellent computer vision, sound analysis, sensor-fusion capabilities, and multiple AI network models. For example, in the facial-recognition use case, parallel to the main AI network model that detects and authenticates specific individuals it's trained to recognize, a relatively lean network will run only over a minimal region of interest (ROI) that was detected and authenticated positive.

The purpose of the secondary network is to run anomaly detection and genuine check to prevent a system breach through DeepFake and others.

The purpose of the secondary network is to run anomaly detection and genuine check to prevent a system breach through deepfake and others. This process overhead must be optimized to minimize power consumption, and therefore will run mixed precision network on selective frames, ROI, and only over selective input/output layers from the main network.

The latter flow is somewhat different from traditional use cases, thus requiring a flexible memory architecture and adaptive data flow between the different AI processor blocks. When authentication negative or a genuine issue is detected, a larger XAI model will come forward to identify the issues that caused the fail and pass that information to the application layer for further action.

How is AXI Implemented?

Most of the AI anomaly-detection use cases are typically on edge AI applications. Anomalies need to be quickly detected, and then identify the cause and report it accordingly to take appropriate corrective actions in real-time.

An AI processor that can run multiple AI networks in parallel and perform computer-vision analysis, as well within the processor itself, is key. Depending on the use case and application, part of an AI network may have to be run, followed by statistical analysis on the subject image or sensing element. This may be followed by manipulation of the image. Then the rest of the first network or another AI network is run to explain the anomaly reason.

Thus, the implementation of XAI requires a powerful processor that offers the following:

- Highly flexible AI processor to implement diverse XAI/ML processing flows: memory architecture, multi-engine structure.
- High-performance computing capabilities: support for multiple data types including low-precision arithmetic operations; highly parallel processing capabilities; advanced quantization capabilities.
- Support the latest neural-network architectures.
- High utilization for efficient power consumption.
- Built-in computer-vision/DSP processing capabilities.
- Support mixed precision inferencing for data and weights.

CEVA Processor for Implementing XAI

One example of a platform designed to run XAI networks is CEVA's NeuPro-M AI processor. The NeuPro-M processor core can be chosen in configurations of up to eight engines, each with its own vision DSP processor. As a result, there's no need for the application to reach for an external DSP, GPU, or CPU for image processing.

Depending on the application need, the configuration with the appropriate number of engines can be selected to enable that many different AI networks to be run. The engines support various neural-network architectures and quantization capabilities.

An application can implement some network layers in 16-bit, some in 8-bit, etc. In certain situations, even 2-bit implementations are possible. This flexibility not only saves power and area, but also accelerates performance, all of which are critical for edge AI use cases. NeuPro-M supports mixed precision as well, e.g., data and weight.

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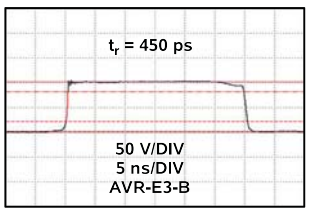

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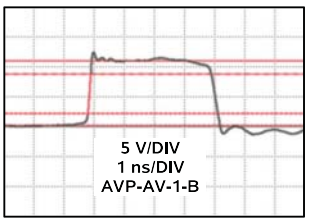

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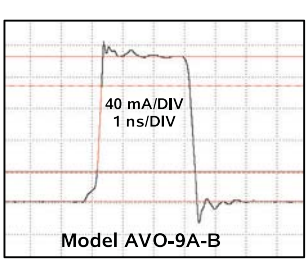

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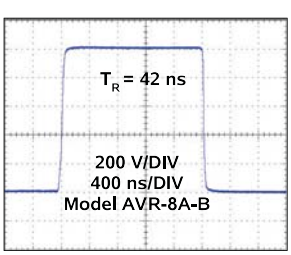

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HAL CONKLIN | Vice President of Business Development, Lightelligence

11 MYTHS About Silicon Photonics

By harnessing the basic properties of light and using photonics to speed computing, systems can be made that extend Moore's Law. However, myths have emerged about the technology. This article debunks them, setting the record straight.

Silicon photonics is a technology that uses silicon-based materials to manipulate and transmit light to create lower-latency compute and interconnect solutions. One of the main advantages is its ability to integrate optical components onto a single package with electronic components. This allows for the creation of highly integrated systems that can process both electronic and optical signals, potentially leading to more efficient and compact devices.

Many misconceptions abound about how to use photonics to enhance today's designs. Its potential is understood, but is it ready to be deployed? Overall, the value of silicon photonics lies in its potential to enable new technologies and applications that were previously not possible with traditional electronic circuitry, as well as to improve the efficiency and performance of existing technologies. So, what myths have emerged? We look at 11 of them, and present the evidence to debunk them.

1. Nice research project, not commercially viable today.

Silicon photonics has been gaining interest in recent years due to its potential to offer high-speed data transfer, increased bandwidth to memory, and low-power consumption. While some challenges are still associated with its implementation, silicon photonics has already shown promising commercial viability in various applications *(see figure)*.

One application is in data-center interconnects, where it can offer high bandwidth, low latency, low power consumption, and rack-to-rack connections. High-speed copper connections have length limitations without using repeaters. Silicon photonics can improve data-center interconnect by providing lower-latency Compute Express Link (CXL) connections between servers, GPUs, and memory pools.

The use of standard CMOS fabrication processes for silicon photonics may be able to reduce the cost and complexity of manufacturing, making it a more viable commercial solution.

2. CMOS will continue to scale according to Moore's Law.

Since the start of the semiconductor industry, computing power improvement can be described by Moore's Law: Transistor density doubles every 18 months, enabling CMOS chips to continuously improve computing power while maintaining constant energy and area consumption.

As the chip manufacturing process moves to 5 nm and 3 nm, transistor density is close to its physical limit. Moore's Law is slowing down and the traditional single-chip computing power improvement path is unsustainable.

Silicon photonics is a technology that will allow scaling to continue beyond the limits of Moore's Law. Digital chips are now limited by the physical limits of the underlying component—the CMOS transistor. Optical signals and devices follow different physical principles. The interactions of optical signals are typically linear and can be mapped as linear calculations. They should enable optical compute accelerators to outperform CPUs and GPUs over time.

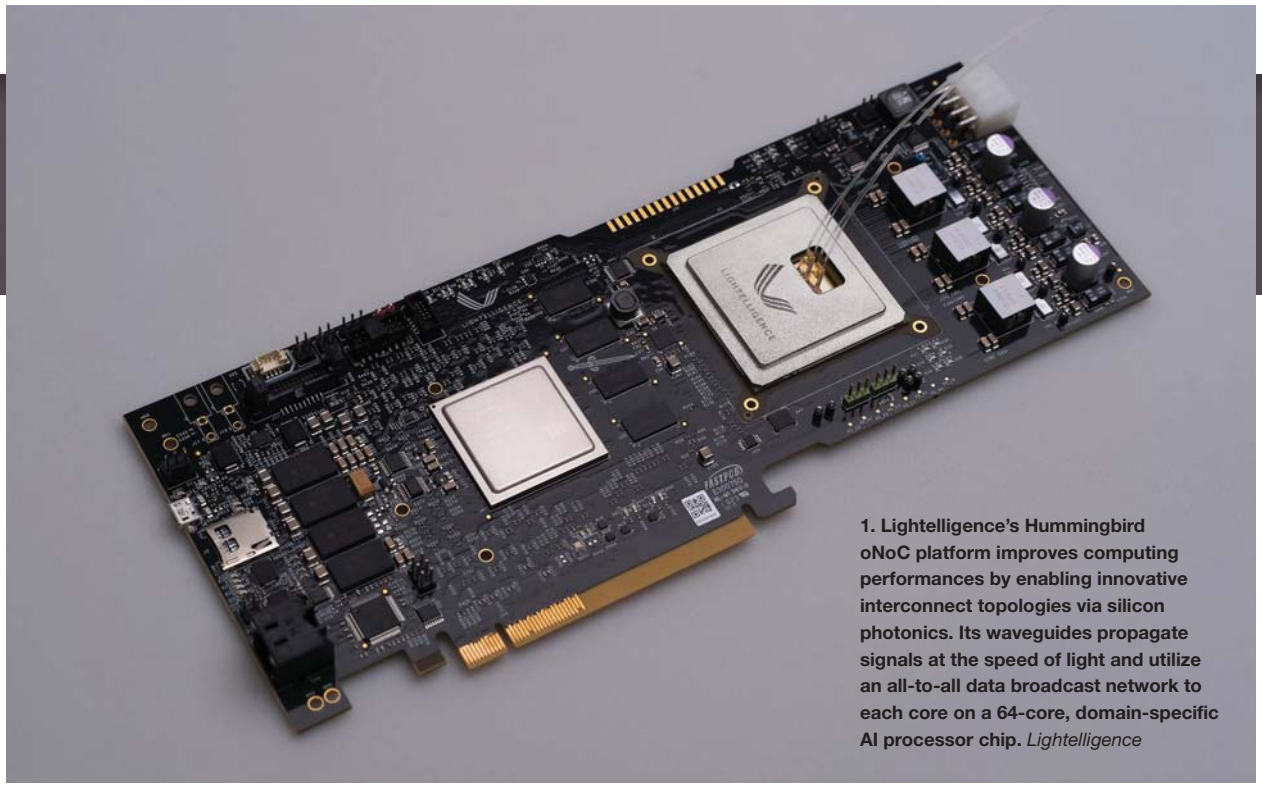
3. Silicon-photonics use cases are very narrow.

Silicon photonics is a technology that uses silicon as a platform for the generation, manipulation, and detection of light. It's a mature technology in telecom and data-center applications for transporting information over fiber connections.

It's now applied to other compute needs, where high bandwidth and low latency are required for scaling systems and has the potential to revolutionize a wide range of industries.

Some applications include:

- Data-center interconnects to transmit large amounts of data over long distances at high speeds.
- High-performance computing to connect multiple processors together, enabling faster data transfer and reduction of I/O bandwidth to large memory pools.



1. Lightelligence's Hummingbird oNoC platform improves computing performances by enabling innovative interconnect topologies via silicon photonics. Its waveguides propagate signals at the speed of light and utilize an all-to-all data broadcast network to each core on a 64-core, domain-specific AI processor chip. *Lightelligence*

- Telecommunications networks to increase capacity and speed of data transmission.
- LiDAR systems for self-driving cars and other autonomous vehicles, enabling precise and accurate distance measurements.
- Quantum computing to control and manipulate qubits, opening the door to faster and more efficient quantum computations.

4. Photonics requires a significant shift in methodology.

Leveraging silicon photonics requires extending the existing methodology from traditional electronics to photonics. In electronics, the information is transmitted and processed using electrons. In photonics, information is transmitted and processed using light. Fabricating photonic ICs will require a different set of design rules, fabrication processes, and testing methodologies.

Using photonic ICs in a system leverages existing methodologies and design rules. Many photonic ICs use electronic ICs in a co-packaged configuration to translate electrical signals to optical signals and back to electrical signals. The application is transparent to the system designer since the optical signals are internal to the device.

5. Implementing silicon photonics would require a steep learning curve for adoption.

The learning curve to fabricate silicon photonic devices is not as steep as other emerging technologies. Silicon photonics involves the integration of multiple disciplines, including electronics, optics, materials science, and fabrication techniques.

Adopting silicon-photonics ICs is similar to electronic ICs since the photonic ICs are generally co-packaged with electronic ICs. These ICs typically have electrical interfaces and behave similarly to other ICs in the design of a system.

6. Digital ICs and photonic ICs are hard to integrate.

Integrating digital and photonic ICs is possible, and it's been proven by several companies producing photonic ICs using a hybrid approach to ensure their reliability and performance.

A hybrid integration approach is often employed to integrate electronic and photonic ICs by fabricating digital and photonic circuits separately and then bonding them together. This can be done using various techniques, such as flip-chip bonding, wire bonding, or solder bonding.

The design and fabrication of hybrid ICs requires careful consideration of several factors, including thermal management, electrical and optical coupling, and packaging. Because digital circuits can generate a significant amount of heat that can affect the performance of photonic circuits, thermal management is critical to ensure the reliability and stability of the ICs.

7. Artificial-intelligence/machine-learning (AI/ML) workloads will continue to scale on GPUs.

AI/ML workloads scale on GPUs without the use of photonics and are the workhorse of AI/ML training due to

their ability to handle parallel-processing tasks, critical for training large models. Thanks to recent improvements in GPU performance, they can handle increasingly complex AI/ML workloads.

However, as AI/ML workloads continue to grow in complexity and size, faster and more efficient data transfer is needed between GPUs and other processing units. This is where photonics can play a role by enabling high-speed, low-latency interconnects between GPUs, CPUs, and other processing units to boost efficiency and data-transfer speed.

As AI/ML models become more complex, specialized hardware accelerators, such as tensor processing units (TPUs) and field-programmable gate arrays (FPGAs), will be required. These accelerators can use silicon photonics for efficient interconnects and data transfer via low-latency CXL connections.

In addition, new photonic accelerators use low-latency optical NoCs (optical network-on-chip or oNoC) to increase performance and throughput of AI workloads. For specific functions, these accelerators are up to 800X faster than the most advanced GPUs.

8. Digital chips at 3 nm have better performance.

It's difficult to directly compare the performance of digital chips at 3 nm and silicon-photonics chips because they're designed for different applications and use different metrics to measure performance. The choice depends on the specific application requirements and design considerations.

Digital chips at 3 nm are designed to process digital information, such as performing arithmetic operations, logic functions, and memory operations. They're optimized for high-speed computation and low-power consumption, which is critical for applications such as mobile devices, data centers, and high-performance computing.

Silicon-photonics chips are designed primarily for transmitting and processing optical signals. They're optimized for high-speed data transfer and low-power consumption, critical for applications such as data communication, sensing, and medical imaging.

It's difficult to directly compare the performance of digital chips at 3 nm and silicon-photonics chips because they're designed for different applications and use different metrics to measure performance.

While digital chips at 3 nm may have better performance than silicon-photonics chips for digital processing tasks, silicon-photonics chips have the potential to offer higher bandwidth and lower latency for data transfer over longer distances. For example, photonics can be used to improve a digital chip's access to memory and significantly reduce the memory I/O bottleneck. In addition, silicon-photonics chips can offer higher energy efficiency for certain applications in which reducing power consumption is critical.

9. Optical NoCs are too small to be practical.

Optical NoCs have the potential to offer high-bandwidth and low-latency communication between on-chip processing units. The practicality depends on various factors, such as cost, power consumption, reliability, and scalability.

The cost of implementing an optical NoC requires specialized components—e.g., lasers, modulators, and detectors—that can be expensive to manufacture and integrate. While optical communication may offer low-power consumption compared to electrical communication, the power consumption of optical components, such as lasers and modulators, still often runs high.

Optical NoCs hold several key advantages over their digital counterparts. Since connections between the digital chips use light, oNoCs are extremely low latency and can communicate with all nodes across the device at the same time. This solves the nearest-neighbor problem with digital ICs and enables new topologies to be considered.

Unlike digital NoCs, oNoCs aren't limited to a single reticle. With wafer stitching, oNoCs can provide wafer-scale density when using standards like the Universal Chiplet Interconnect Express (UCIe) for the digital interfaces between chiplets.

10. CXL is fine with copper interconnect, not optical interconnects.

CXL is a high-speed interconnect standard designed to enable communication between CPUs, GPUs, memory, and other processing units. While the initial versions of CXL use electrical interconnects, utilizing optical interconnects for CXL beyond a meter is growing in interest.

Optical interconnects can offer higher bandwidth, lower latency, and lower power consumption compared to electrical interconnects, especially over longer distances. Using optical interconnects for CXL beyond a meter can also enable more flexible system design and deployment. With optical interconnects, processing units may be placed further apart, allowing for more flexible system configurations and reducing the need for complex cabling.

11. Other technologies are more promising.

Silicon photonics is being used for high-speed interconnects in computing systems, including interconnects between processors, memory, and other components. Another application is in the development of co-packaged photonic ICs with electronic ICs. These packages offer a more compact and efficient solution for data transfer between components in computing systems, reducing the need for complex cabling and improving the overall performance and power consumption of the system. ED

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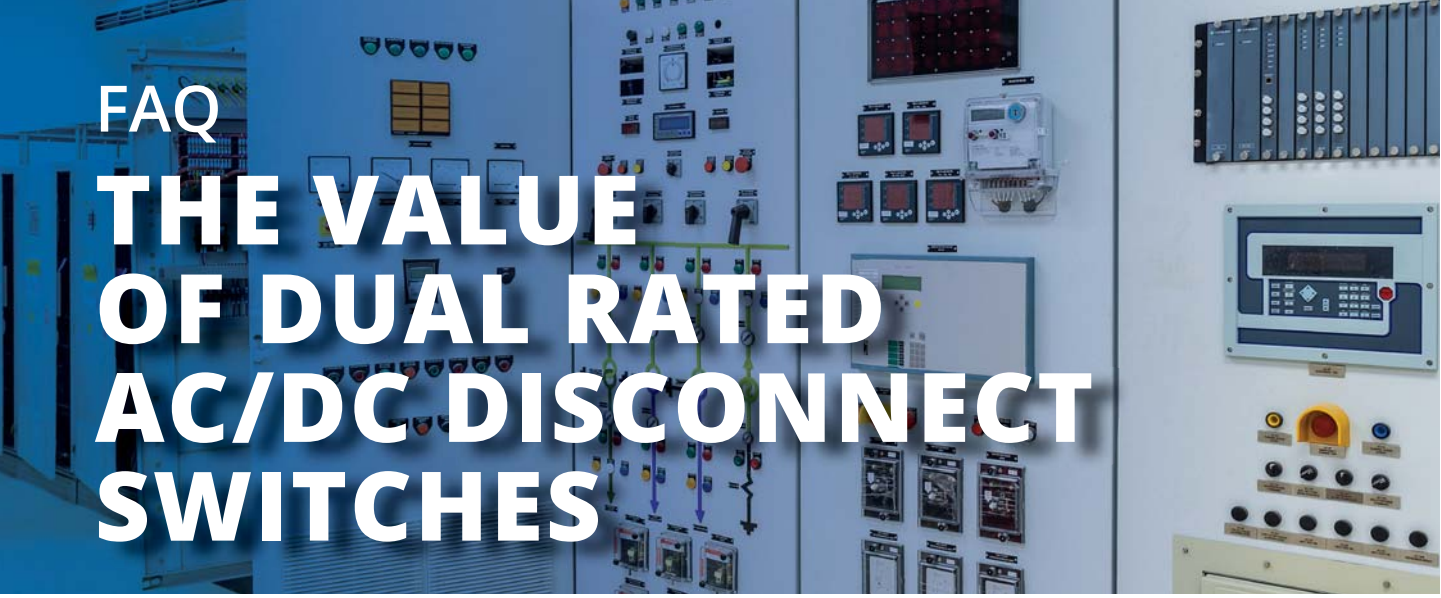

FAQ

THE VALUE OF DUAL RATED AC/DC DISCONNECT SWITCHES

Q: Why is it necessary for me to have a disconnect switch installed in my application?

A: The main function of a safety disconnect switch is to protect personnel from harm and equipment from damage. Disconnect switches are used to guarantee that a specific electrical circuit is de-energized in the case of an emergency failure, service requirement, or maintenance operation. Disconnect switches have become critical components for electrical distribution systems whether for plantwide use or isolated areas so that technicians can provide repair and maintenance of one machine while the rest of the facility operates normally. In addition, the National Electric Code mandates that disconnect switches are used in all industrial and manufacturing facilities.

Q: What does a DC motor disconnect switch do?

A: An AC disconnect switch is designed to separate the inverter from the electrical grid, while a DC disconnect switch is designed to separate the equipment from the DC source. Until recently, users had to purchase each of these separately, but companies have created innovative products, like the dual rated disconnect switch that combines both functions for ease of use. The switches must be installed in such a way that incoming power can be quickly shut off whenever an emergency occurs.

Q: How is it possible that these disconnect switches have evolved to this point?

A: A number of factors pull together whenever there is an advancement. Innovation, of course, is an ongoing thing, but other aspects can push technology forward more quickly. For example, as markets change, the availability of materials changes, and the needs of manufacturing change, design teams adjust to meet those situations. At that point, engineers are tasked with not only coming up with new devices to meet present challenges, but to project into the future as well. Only companies with a history in the market have the insights needed to provide this type of innovation.

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Q: Could you further discuss some of the technologies used inside these disconnect switches?

A: High-grade plastics are used to make the switch bodies, which are designed to handle most harsh environments on the factory floor. The tough bodies also operate within a wide temperature range and provide users with a shock resistant and chemical resistant product. Contact quality inside the device was also something the design team focused on. Silver plated contacts and rivets were used throughout the device in order to assure long life and better conductivity.

Q: With the dual rated disconnect switch, do I need additional panel or control room space?

A: Not at all. Technology advancements have added to an engineering team's ability to design products with greater capabilities while maintaining the same form factor. In fact, with smaller areas of real estate being available in such applications as robotics and lab equipment, disconnect switches are often mounted close to the device. This meant that size was a critical factor in the design.

Q: What specific products are on the market now that meet these challenges?

A: At this time, Altech has recently introduced the LSF series of disconnect switches that are the only DC switches available in a compact frame size that is dual rated for AC and DC. Due to the needs of the industry, these switches have been made available for mounting in multiple ways, including with an integrated base and DIN-rail mounting, and a separate RT version with integrated door mounting and side panel mounting.

Q: Could you supply some technical details concerning these disconnect switches?

A: Basically, the RT devices are provided with rear facing terminals to make them easy to install. For electrical box installations, there are two mounting versions that are dependent strictly on user requirements.

The first option is an extended handle application where the shaft sticks out beyond the electrical box for easy access and interlocks with an external handle so that the box cannot be opened until power is turned off (see Figure 1). Frame size it only 36mm (W) x 71mm (H) x 46mm (D), without integrated switching knob and panel mount tabs.

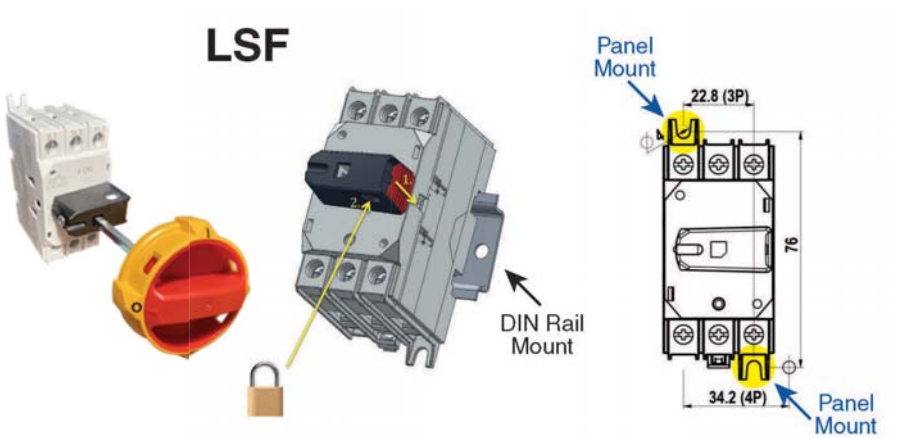


Figure 1: The extended handle application uses a long shaft that sticks out beyond the electrical box for easy access.

Q: Could you supply some technical details concerning these disconnect switches? ***(continued)***

The other option is a panel mount version. This disconnect switch is typically installed in a side panel and requires users to drill a small 22.5mm hole into their panel. The hole is used to accommodate the rear-mounted disconnect switch (see Figure 2). Once installed, a knob is attached to the front of the panel for easy access.

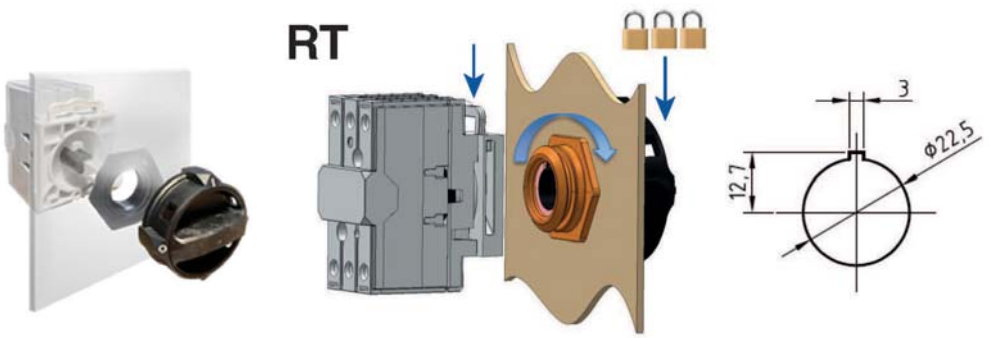


Figure 2: The panel mount option for the LSF series disconnect switch is easy to install.

Both mounting options have only three parts, unlike most other products on the market that have multiple parts and can be complex to install. The entire LSF series of disconnect switches are available for a wide variety of applications. They are available in 16A, 30A, and 40A versions and offer UL 60947-4-1 certification.

Q: Are there any other important design features I need to know about?

A: There is another feature that has to do with the switch's make/break operation, which is independent from the operator's turning speed. The actuator arm essentially has nothing to do with changing the switch's state. Internally, the switch is spring loaded so that the DC current cannot arc or burn up the contacts after multiple uses. The switch is turned to a certain point and then snaps into place and cannot be backed off.

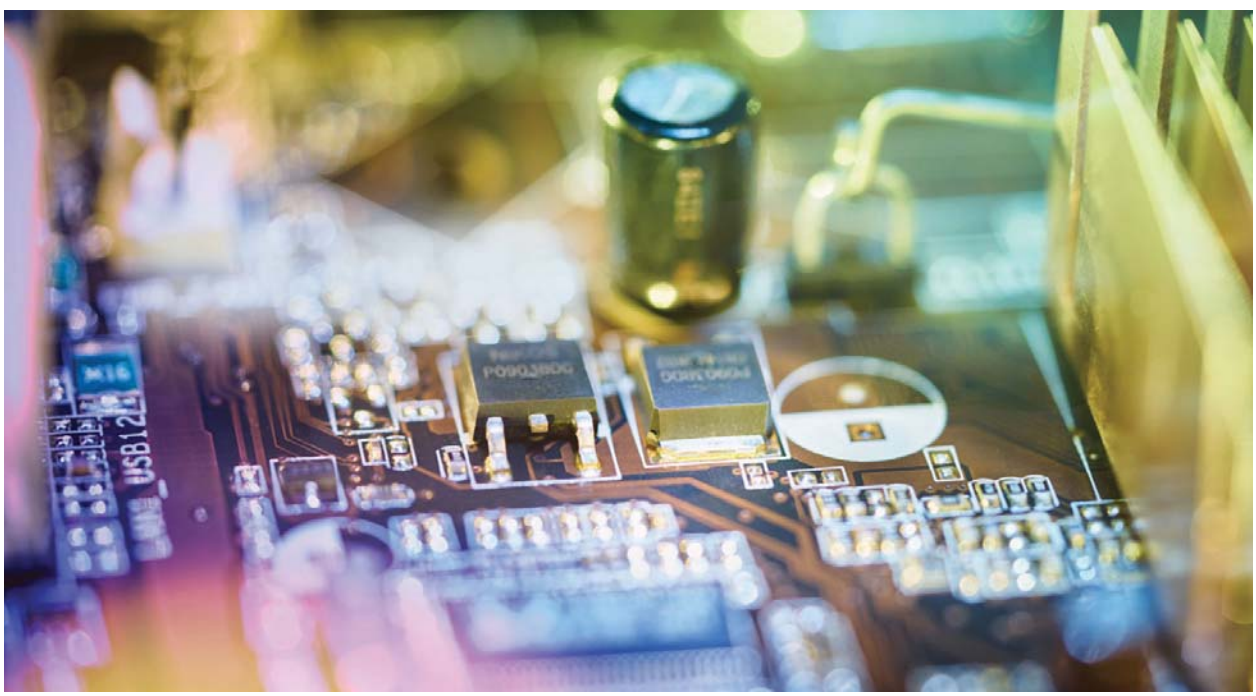
Q: While incorporating new designs and new technologies, does this affect supply chain deliveries?

A: Great question. When thought through properly, design and automation go hand-in-hand with supply chain considerations. New designs, such as the LSF series, go through rigorous analysis to assure that quality is maintained through the entire line of products being manufactured and that an equal amount of attention is paid to the availability of materials and the reduction of the number of component parts—all aimed at maximizing supply chain capabilities while minimizing the challenges.

FREDERIK DOSTAL | Power-Management Technical Expert, Analog Devices

How to Easily Design **Power Supplies (Part 1)**

This article looks at the LDO and the switch-mode power supply, as well as the most common non-isolated topologies used for SMPS.



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This article series gives an overview of the possibilities for power-supply design. It addresses the basic and commonly used isolated and non-isolated power-supply topologies along with their advantages and disadvantages. Also covered will be electromagnetic interference (EMI) and filtering considerations. This mini tutorial aims to provide a simplified understanding and renewed appreciation for the art of power-supply design.

Most electronic systems require some sort of voltage conversion between the voltage of the energy supply and the voltage of the circuitry that needs to be powered. As batteries lose charge, the voltage will drop. Some dc-dc conversion can ensure that much more of the stored energy in the battery is used to power the circuitry. Furthermore, for example, with a 110-V ac line, we can't power a semiconductor such as a microcontroller directly.

Since voltage converters, also named power supplies, are used in almost every electronic system, they have been optimized for different purposes over the years. Certainly, some of the usual targets for optimization are solution size, conversion efficiency, EMI, and cost.

The Simplest Power Supply: The LDO

One of the simplest forms of a power supply is the low-dropout (LDO) regulator. LDOs are linear regulators as opposed to switching regulators. Linear regulators put a tunable resistor between the input voltage and the output voltage, which means the output voltage is fixed independent of how the input voltage changes and which load current is running through the device. *Figure 1* shows the basic principle of this simple voltage converter.

For many years, a typical power converter consisted of a 50- or 60-Hz transformer, connected to the power grid, with a certain windings ratio to generate a non-regulated output voltage—a few volts higher than the needed supply voltage in a system. Then, a linear regulator was used to convert this voltage to a well-regulated one as needed by the electronics. *Figure 2* shows the block diagram of this concept.

The problem with the basic setup in *Figure 2* is that the 50-/60-Hz transformer is relatively bulky and expensive. Moreover, the linear regulator dissipates quite a lot of heat, so the total system efficiency is low and getting rid of the generated heat is difficult with high system power.

Switch-Mode Power Supplies to the Rescue

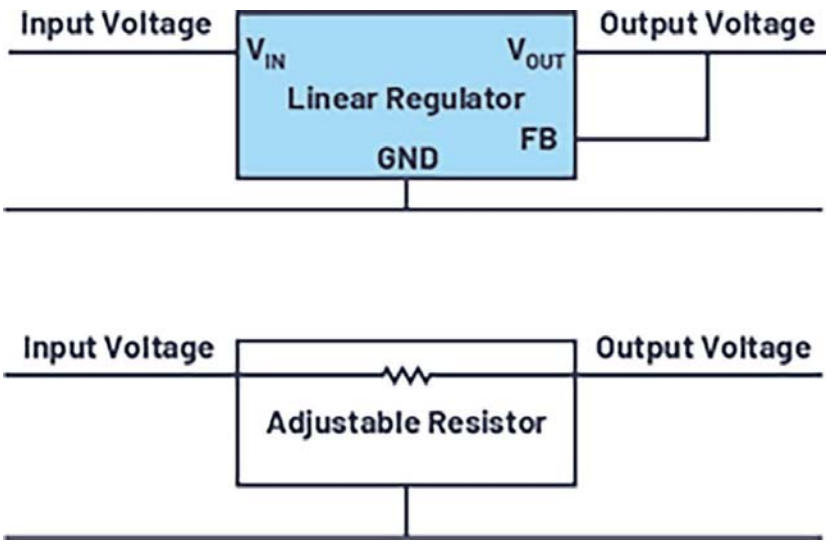
To avoid the disadvantages of a power supply as shown in *Figure 2*, switch-mode power supplies (SMPS) were invented. They don't rely on 50- or 60-Hz ac voltage. SMPS take a dc voltage, sometimes rectified ac voltage, and generate a much higher-frequency ac voltage to use a much smaller transformer. In non-isolated systems, they can rectify the voltage with an LC filter to generate a dc output voltage.

The advantages of SMPS are small solution size and relatively low cost. The ac voltage being generated doesn't need to be a sine voltage waveform. A simple PWM signal shape will work just fine and is easy to generate with a PWM generator and a switch.

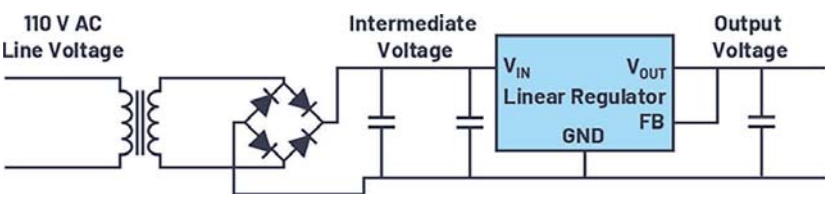
Up until the year 2000, bipolar transistors were the most commonly used switches. They would work well but had relatively slow switching transition speed. They weren't very power-efficient, limiting the switching frequency to 50 kHz or maybe 100 kHz.

Today, we use switching MOSFETs instead of bipolar transistors, allowing for much faster switching transitions. This, in turn, gives us lower switching losses, which enables switching frequencies of up to 5 MHz. Such high switching frequencies make it possible to use very small inductors and capacitors in the power stage.

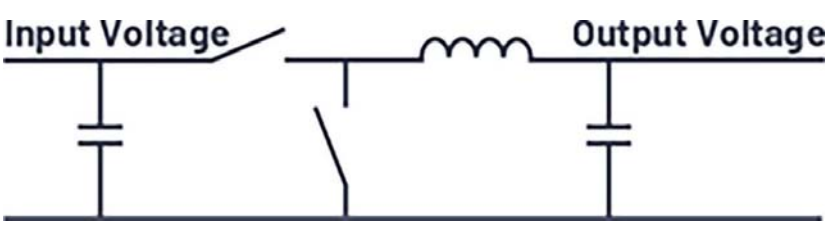
Switching regulators bring many benefits. They generally deliver power-efficient voltage conversion, enable voltage step-up and step-down, and offer relatively compact and low-cost designs. The disadvantages are that they're not so simple to design and optimize, and they generate EMI from the switching transitions and the switching frequency. The availability of SMPS regulators, along with power-supply design tools such as LTpowerCAD and LTspice, have greatly simplified this difficult design process. With such tools, the circuit design process of a SMPS can be semi-automated.



1. A linear regulator converts one voltage into another.



2. Shown is a line transformer followed by a linear regulator.



3. Concept of a simple buck step-down converter.

Isolation in Power Supplies

When designing a power supply, the first question should be whether or not galvanic isolation is required. Galvanic isolation is used for multiple reasons. It can make circuits safer; allows for floating system operation; and prevents noisy ground currents from spreading through different electronic devices in one circuitry. The two most common isolated topologies are the flyback and forward converters. However, for higher power, other isolated topologies are employed, such as push-pull, half-bridge, and full-bridge.

If galvanic isolation isn't required, then in most cases a non-isolated topology is used. Isolated topologies always require a

transformer, which tends to be expensive, bulky, and often difficult to get off-the-shelf with the exact requirements of a custom power supply.

Most Common Topologies When Isolation Isn't Required

Buck

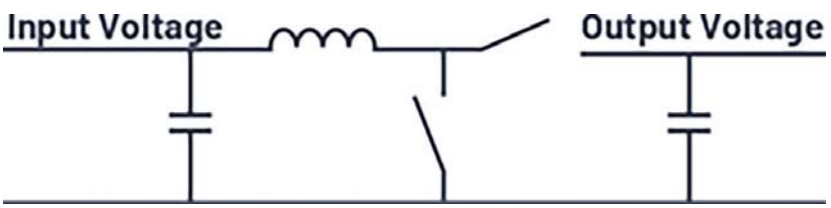
The most common non-isolated SMPS topology is the buck converter. It's also known as the step-down converter. It accepts a positive input voltage and generates an output voltage lower than the input voltage. The buck converter is one of the three most basic SMPS topologies that only require two switches, an inductor, and two capacitors.

Figure 3 shows the basic principle of the buck-converter topology. The high-side switch pulses a current from the input and generates a switch-node voltage alternating between the input voltage and ground voltage. The LC filter takes that pulsed voltage on the switch node and generates a dc output voltage. Depending on the duty cycle of the PWM signal controlling the high-side switch, a different level of dc output voltage is generated. This dc-dc buck converter is very power efficient, relatively easy to build, and requires few components.

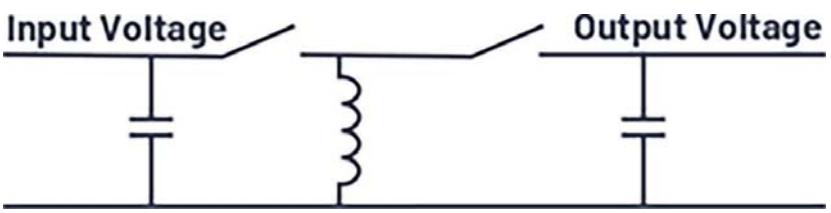
The buck converter pulses current on the input side, while the output side has continuous current coming from the inductor. This is the reason why a buck regulator becomes very noisy on the input side and not so noisy on the output side. Understanding this is important when low-noise systems must be designed.

Boost

Besides the buck topology, the second basic topology is the boost, or step-up, topology *(Fig. 4)*. It uses the same five basic power components as the buck converter, but rearranged, so that the inductor is placed on the input side and the high-side switch is placed on the output side. The boost topology is used to step up a certain input voltage to an output voltage that's higher than the input voltage.



4. Concept of a simple boost step-up converter.



5. Concept of a simple inverting buck-boost converter.

When selecting a boost converter, it's important to note that boost converters always specify the maximum rated switch current and not the maximum output current in their datasheets. In a buck converter, the maximum switch current is directly related to the maximum achievable output current, independent of voltage ratio between the input and output voltage. In a boost regulator, the voltage ratio directly affects the possible maximum output current based on a fixed maximum switch current. When selecting a suitable boost regulator IC, you need to not only know the desired output current, but also the input and output voltage of the design in development.

A boost converter is very low noise on the input side because the inductor in line with the input connection prevents rapid changes in current flow. However, on the output side, this topology is quite noisy. We only see pulsed current flow through the outside switch, and thus output ripple is more of a concern compared to the buck topology.

Buck-Boost

The third basic topology, only consisting of the five basic components, is the inverting buck-boost converter *(Fig. 5)*. The name is derived from the fact that this converter takes a positive input voltage and converts it into a negative output voltage. Besides this, the input voltage may be higher or lower than the absolute of the inverted output voltage. For example, –12 V output voltage may be generated out of 5 V or 24 V on the input. This is possible without making any special circuit modifications.

In the inverting buck-boost topology, the inductor is connected from the switch node to ground. The input side as well as the output side of the converter see pulsed current flow, making the topology relatively noisy on both sides. In low-noise applications, this nature is compensated by adding additional input and output filtering.

One quite positive aspect of the inverting buck-boost topology is the fact that any buck switching-regulator IC may be used for such a converter. It's as simple as attaching the output voltage of the buck circuit to system ground. The buck IC circuit ground will become the adjusted negative voltage. This trait leads to a very large selection of switching-regulator ICs on the market. ED

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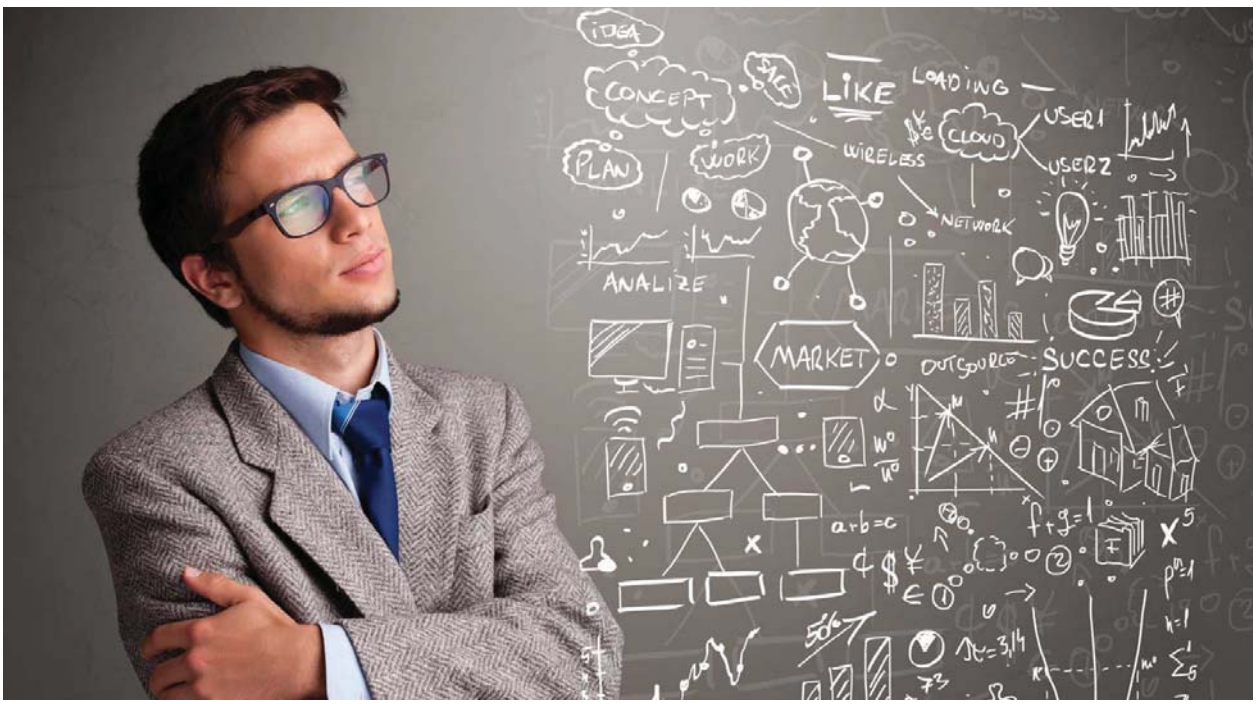

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Why are Specifications and Characterizations for Op Amps and FDAs Different and Confusing?

From input offset voltage to slew rate to gain bandwidth product, specifications for operational amplifiers can vary widely amongst different vendors.

It can be a maddening (and time-consuming) task to compare data across vendors to get a real comparison between possible solutions. Between "marketesse" and just plain deception and/or errors, how can you see through these and normalize critical specs across vendors to get real comparisons.

Having contributed to the development and product launch of over 150 high-speed amplifiers from 1985 forward, the level of detail and tradeoffs going into product datasheets and simulation models probably exceeds the wildest imaginings of the end-system designers. Here you will learn some of the hidden background for (and often confusing) specifications along with what to look out for in characterization curves and vendor simulation models.

First, who does this work and what do they bring to the task?

IC design engineer

The designer, working with the latest process design kit (PDK) takes the marketers end-product targets and iterates over many months to get close. Usually, these targets take the form of more and more performance at lower and lower supply current.

Occasionally, a new topology will come along that fills an important niche, such as the fully differential amplifier (FDA) and current feedback amplifier (CFA). Once the nominal transistor-level topology is set, he/she will start running statistical process case and over-temp simulations to extract out corner cases for the proposed end limits on key specs. PDKs have evolved to be remarkably good; only some of that gets into the datasheet and customer simulation models.

Marketing engineer

Looking at the extant solution universe, the marketing engineer tries to carve out unique and valuable new product targets. Through the course of

design and introduction, he/she trades off "don't care" versus "must care" specs with the designer to hopefully emerge with a meaningful new solution for the analog design community.

ATE engineer

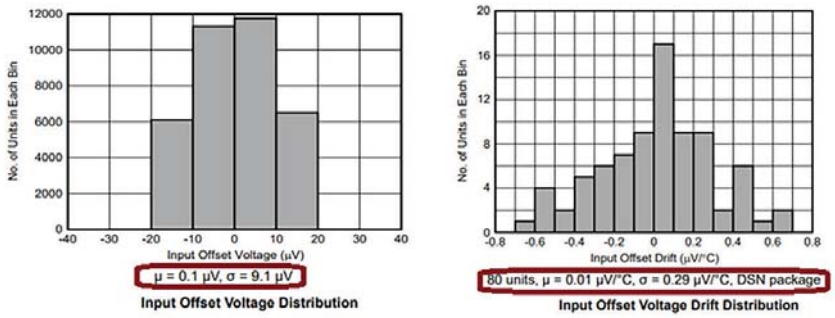
This key team member is tasked with layering over a set of probe and/or finished product tests to ensure nothing ships that's defective. In the early days of high-speed amplifiers, 100% ac testing was done at Comlinear Corp on the industry's first current feedback op amps using an HP3577 network analyzer. Over time, it became clear that a full suite of stressful dc tests shipped good ac parts and that production expense was eliminated.

With a few exceptions, all current precision and higher-speed amplifiers receive only a dc test at probe and/or final test at some nominal temperature (with some span on that), imputing ac performance within the designer worst-case simulation results.

The ATE engineer is incentivized to deliver tests and limits with 100% yield. The marketing engineer must resist this—say, on input offset voltage, a ±3.5-sigma test limit is probably adequate (implying no more than 0.04% yield loss). Expanding single-lot ATE data to final datasheet limits is largely internal culture, designer simulation tools, and judgement calls among the development team members and any QA mandates that might be imposed.

Applications engineer

Directed by the marketing engineer, and with an assist from design, the application engineer is tasked with taking the characterization curves and working with the modeling team to develop and test the public simulation model. This is where the rubber meets the road in what the customer sees as a product support package. He/she will also add suitable application text and examples to the final datasheet to illustrate the fabulous new capability for a device that probably cost well over $1M to develop.



1. Recent OPA2863A offset and offset drift histogram examples show widely different plus/minus sigma limits.

Personnel and Datasheet "Churn"

One of the difficulties with consistent and accurate material is the relative turnover in these positions. Often, the designer and ATE engineer are 20-plus-year folks. There's quite a bit of churn in the marketing and applications roles where the latter might be just out of school. Hence, a very tenuous thread links today's datasheets to those done even 10 years ago (and nearly none to those done 20 years ago).

At a more basic level, no NIST reference document exists on how the different specs and characterization curves "must" be done. In fact, on some of the critical specs, there's been an ongoing evolution of better methods.

For instance, when I first started doing distortion plots (circa 1987), about −90 dBc was the measurement limit imposed by spectrum analyzers. Today, bench techniques reach down near −150 dBc (if you want to spend enough effort on it, very non-trivial—operating above audio precision measurement frequency range).

Clarifications on Occasionally Murky DC Specs

Most of the op-amp and FDA dc specifications are pretty clear. Some, but not all, of the dc specifications become the final test lines. A few can cause confusion at times, particularly those with a zero mean as well as the output current specification.

Input offset voltage

The input offset voltage (and current for bipolar inputs) will usually have a distribution centered on zero. Modern devices trim this to a zero mean at either wafer probe or packaged eTrim. So what do you specify for a typical, because "0" doesn't really give you much information?

The informal practice across the industry is to report the ±1-sigma number as the typical specification to avoid customer surprises when devices with a zero mean don't test at zero for typical devices. Specifications for a maximum input offset voltage (and current where needed) are extremely inconsistent. Essentially those are a combination of a plus/minus shift of the mean off of zero plus/minus some number of standard deviations.

My practice was to impose a ±3.5-sigma range (THS4551) to accept approximately 0.04% yield loss. Other devices and product groups allow for much wider limits (OPA837, THP210, ADA4805, etc). Some of this is related to test repeatability, where there's also an error band in test over different physical testers. While this might pass more units, you do wonder if devices way out on the distribution tails (some allow for >8 sigma) might be shipping "defective" units.

These same issues apply to the specified input-offset-voltage temperature drift, where it's extremely rare to see this as a 100% tested specification (the JFET input OPA656 is one of the very few). Maximum offset drift numbers are sometimes provided without ATE screens (OPA2683A, ADA4895), while many more devices have no maximum drift spec(s).

The guaranteed maximum drift numbers are from extensive bench characterization of packaged units that are

(hopefully?) at the extreme allowed limits of the tested room-temp input offset voltage (and current where appropriate). Drift magnitude is often linearly related to initial offset, so testing units at the allowed limit should expose the worst-case drift specs.

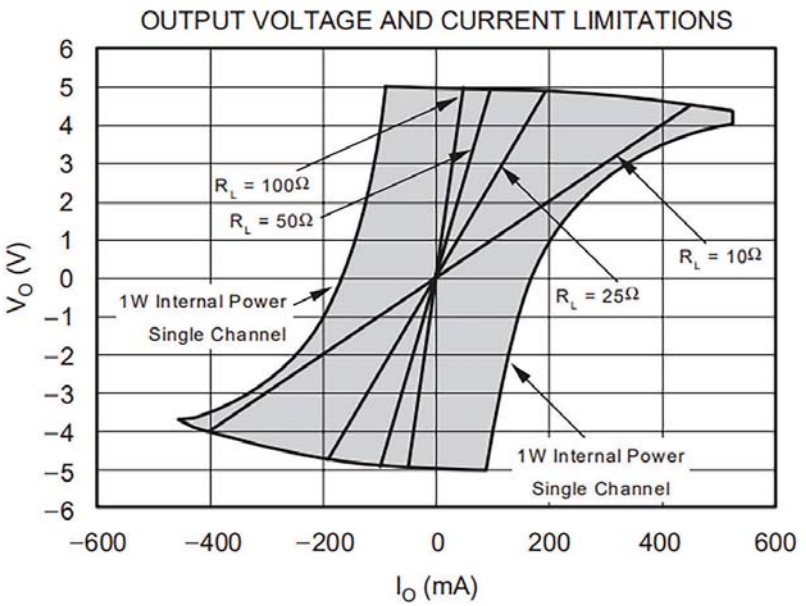
Figure 1 shows a recent example where the tested V_{os} limits are ±95 µV (or ±10 sigma), imputing a drift limit of ±1.2 µV/°C or ±4 sigma. The actual V_{os} histogram data in *Figure 1* is much tighter than the ATE limit in the specification table. Apparently, the ATE engineer got this through while the marketer was out traveling.

Output current

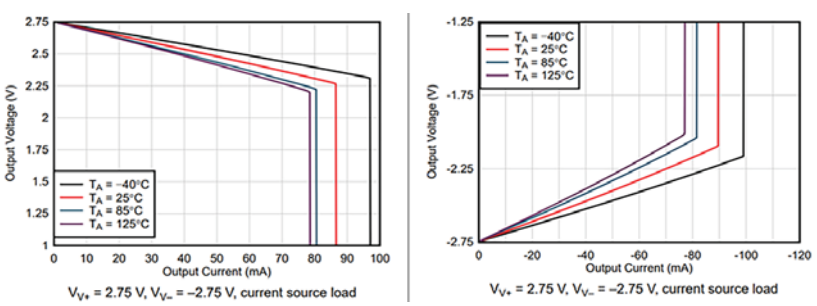
Probably the most slippery dc specification on any op-amp or FDA datasheet is the output current. Marketers want the biggest number possible. Designers struggle with that as large output devices bring an increased capacitance, which adds open-loop phase shift that impairs achievable bandwidth on ever-declining supply current budgets. ATE engineers are all over the map in how this might be tested.

Physically, the output-current demand will get involved with the available "linear" output-voltage swing available. Every device (even rail-to-rail outputs) will see an increase in required headroom to the supplies for linear operation due to rising load-current demand. Keep in mind that not only the actual load, but also the feedback network, is part of that load. In non-inverting configurations, that's the sum of the feedback and gain resistors, while in inverting configurations (and for FDAs), it's just the feedback resistor appearing in parallel with the actual load.

First, it's important to recognize that any "short circuit" current specification



2. Shown is an example four-quadrant output VI limit for a dual CFA high-power PLC line driver.



3. Compared are the output swing vs. current for the RRIO precision OPA328.

is usually a self-limited (base or gate drive) typical specification. Traditionally, it needs to be there, but it doesn't really give you much information. Only when there is a min. or max. specification is there an "active" current limit in the output stage design (THS3491), with some exceptions (OPA2683A).

Over time, several different efforts at a "linear" output-current specification have been attempted. During the PLC line-driver developments (where the line can push current back into an amplifier output), a four-quadrant envelope of limits was shown—like that in *Figure 2* taken from the OPA2674 datasheet (on ±6-V supplies). Only the quadrants with the load lines describe normal operation here.

More typically, a bipolar "claw" curve has evolved to describe the loss of output headroom, as more sourcing or sinking current is required. Here, the two polarities are separated into two plots, but the increase in required headroom with out-

Maximum current into a resistive load	T_A ≈ 25°C, ±1.6 V into 27 Ω, V_{IO} < 2 mV	±58	±70	mA	A
Linear current into a resistive load	T_A ≈ 25°C, ±1.7 V into 37.4 Ω, A_{OL} > 80 dB	±45	±50	mA	A

4. This is an example linearity test for output current and voltage into a resistive load for the OPA837.

put source/sink current is clearly shown in *Figure 3*.

These output limits are hard limits (usually from simulation). However, in final ATE, a more common test is a minimum Aol test at some conservatively guardbanded (25°C) test point. It exercises most of the available output current (from worst-case designer simulations at 25°C) at the maximum swing to rail available at that current draw, as shown in *Figure 4* for the OPA837.

Here, the final ATE test lines are clearly designated by the "A" test level, and the test conditions to produce these stated output currents are shown (using ±2.5-V supplies in this case). This type of ATE screen is intended to ensure that no "weak" output stage devices are getting into inventory.

These issues apply to all op amps and FDAs. It is, however, often not clearly shown in the customer support material and almost never accurately modeled in the vendor simulation models.

Common Hazards in Interpreting Op-Amp and FDA AC Specs

If the dc specifications have some typical traps, the ac specifications are often much worse. Again, none of these are tested on an outgoing basis and the typical—and much more rarely guaranteed—ac specifications (e.g., OPA2677) come completely from simulation. Usually, a single (hopefully typical) lot of early material is characterized one time at product release.

Vendor models are normally bounced against typical designer simulation with some first-lot material validation. A few very typical performance parameters are prone to error and/or confusion.

Input spot noise

The input spot noise voltage must be in every datasheet. Physically, these always have a 1/f corner that varies considerably more than the higher-frequency "flatband" number (except for chopper-input VFAs, which have a flat noise spectrum down to dc but then add noise spurs at the higher chopper frequency).

A very old convention for relatively slow (often precision) amplifiers is to report an input spot noise at 1 kHz. This apparently came out of the audio world and the 1-kHz number may be above, or below, the 1/f corner. It's much more descriptive to specify a typical flatband number (most higher-speed amplifiers do this) above the 1/f frequency and then a typical 1/f corner.

However, many VFAs quote a single noise number and only after some digging can you discern if that's the 1-kHz number. You must then consult the swept-frequency input spot noise plot to decide what that means.

Gain bandwidth product

The second most confusing ac specification has become the typical gain bandwidth product (GBP) for VFA op amps and FDAs. Classic theory describes this as the 1-pole projection to 0-dB crossover for the devices' Aol curve. Modern devices have higher-frequency open-loop poles (and sometimes pole/zero pairs, LT6363) in the Aol response that convolutes this quite a bit.

Since the new product characterization folks are a revolving door of new grads, many datasheets erroneously report the GBP as the Aol = 0 dB frequency.[1] That's never very close for decompensated devices and often even a bit off for unity-gain stable devices. This confuses new grads quite a bit since the closed-loop small-signal BW (SSBW) never really was accurately described by the GBP idea even for unity-gain stable VFAs.[1] Lower phase margins at loop-gain (LG) crossover always extend the closed-loop SSBW far beyond the GBP model (below 65-deg. phase margin, which is approximately a 1.6X extension).

Sometimes, those new grads try to force a fit to the simple GBP model by modifying what they report. It's always best to confirm the single-pole GBP in simulation for design work *(go to the 40-dB Aol gain frequency and multiply that by 100X to get the single-pole GBP; Figure 6 shows a simulation setup, see page 32).* Oftentimes, that's far different than what shows up in the datasheet, and hopefully the modeling effort worked closely with the designer to emulate the new devices' typical Aol gain and phase-match the designer PDK simulations.

Slew rate

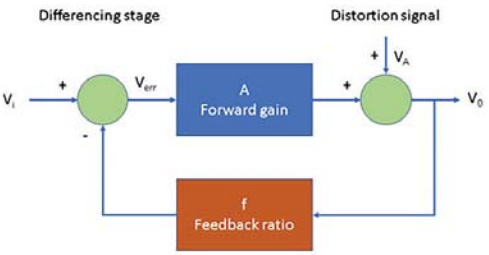
Slew rate has long been a difficult specification and fraught with error. Early ±15-V op amps showed a very distinctive, limited dv/dt on a large output transition. Sometimes those are different for rising and falling, where reporting the faster rate in the specification table is not uncommon. With few exceptions, a signal that rises with a certain maximum rate must also fall at a similar rate. Check the plots to see if this bit of chicanery is at play (Figure 39 in the OPA192 datasheet).

$$\begin{cases} V_0 = A * V_{err} + V_d \\ V_{err} = V_i - f * V_0 \end{cases}$$

$$V_0 = A * V_i - A * f * V_0 + V_d$$

$$(1 + A * f) * V_0 = A * V_i + V_d$$

$$V_0 = A * \frac{V_i}{(1 + A * f)} + \frac{V_d}{(1 + A * f)}$$



5. Fundamental harmonic distortion correction in negative feedback op amps or FDAs.

In most applications, the available slew rate is like a hard output transition rate that should be avoided, if possible, in application. By definition, the feedback loop has opened up if the output is slew limiting where that recovery time to a closed-loop final condition is rarely specified—and if so, only for limited number of external operating conditions.

The best way to explore edge transition rates is to plot the measured or simulated point-by-point dv/dt on the edges.[2] This will clearly show when an edge has hit a slew limit (flat dv/dt) and more detail is going into and out of slew limiting.

Harmonic distortion

One of the more difficult characterization requirements in any new op-amp or FDA development is a range of typical harmonic-distortion plots. These have evolved over the years to show performance to ≤145 dBc on occasion. The main reporting difficulty is all of the different conditions that influence the measured values, including:

- Supply voltages
- Gain (more precisely, the loop gain over the testing frequency span)
- Output loading (and this includes the required feedback network)
- Output voltage swing
- Frequency of the test fundamental (or two of these for two-tone intermodulation testing)

This myriad of test conditions does make it relatively difficult to compare data across different possible solutions. It's important to always keep in mind some fundamental harmonic-distortion facts. Essentially, the output closed-loop distortion terms are the open-loop distortion terms in the output stage corrected by the LG at the fundamental frequency of testing. The LG is A*f* in *Figure 5*.

The easiest way to show a better HD number in characterization is to test with a lighter resistive load. Be careful comparing devices on their stated loading under test.

Hidden Traps in Vendor-Supplied Simulation Models

As a new op amp and/or FDA approaches public release, the modeling effort gets underway. Over time, several approaches have dominated:

- **Simplified full transistor-level models:** These can be very good if the embedded transistor models capture enough of the available parameters (Comlinear models and full netlists are in the TINA libraries showing detailed transistor models).[3] Some transistor-based models use such a simplified core transistor model that they're nearly useless.
- **Boyle model:** This is more of a behavioral model that does okay on basic things, but often isn't very accurate.[4]
- **Custom block diagram types of models that can capture quite a lot of the device characteristics:**[5] In this case, the internals are often company confidential and sometimes those models are encrypted.

How this is organized inside a company makes a huge difference in the effective-

ness of these models. Some groups have each project's individual application engineer and/or designer do these (which leads to lots of modeling variations). Some have a dedicated modeling group that usually leads to throughput bottlenecks. Others have a designated applications specialist in each development group that becomes the resident expert. This will yield better and better models with some consistency, until they move on to another job.

One theme here is that the op-amp and FDA models have been getting regular updates from some of the vendors. Designers should certainly try to verify that they're using the most recent update, as earlier (more error-prone) models are still available from some legacy sources.

Importantly, the vendor models must assign some typical dc value specifications where their "range" is never captured. Therefore, dc parameters are just enough—they don't span the full range of the datasheet specification limits. Far more effort is put into the ac performance characteristics, but again, only typical. To get a good prediction of small-signal ac performance over a wide range of external application circuits, the model must have very good:

- Open-loop gain and phase modeling.
- Open-loop output impedance modeling (this has become relatively involved with RRout devices).
- Accurate input impedance modeling. This is usually mainly input capacitance, but for CFA devices, a good inverting-input impedance model is necessary (usually just a low R value; however, for instance, the THS3217 OPS model includes a series RL into the inverting input and parasitic C to ground on that device pin).

An op amp's open-loop gain or phase is really the core value proposition for the ac aspect of the device. There are numerous approaches to extracting this from the vendor model. *Figure 6* shows one simple approach.

Typically, these are done with split bipolar supplies with the V+ input grounded and the test signal injected into the inverting input. It's critical to load the amplifier with the stated resistive (and/or capacitive) loads noted in the datasheet.

This approach applies a simulation trick to close the loop at dc at unity gain using a ludicrously high feedback L value, and then injects the small-signal ac test input through an equally high input capacitor. These elements set up a midscale dc operating point and then disappear on the first ac frequency step. Since the input is into the inverting input, the output meter here is rotated 180 deg. to report Aol, where its phase starts out at 0 deg. and proceeds toward −180 deg.

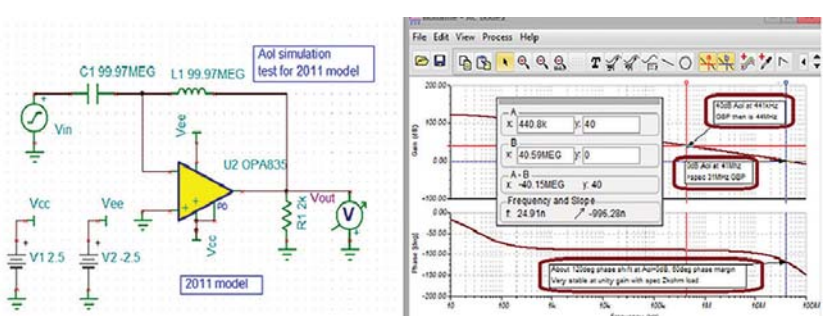
This model shows quite a bit more GBP than the specified typical of 31 MHz. The 0-dB crossover is less than the predicted

single-pole GBP due to the higher-frequency Aol poles indicated by the phase shift moving down −90 deg. from the single pole. This OPA835 model is now updated to a 2017 revision, where this simulation shows a correct 31-MHz GBP projecting from a 40-dB Aol point.

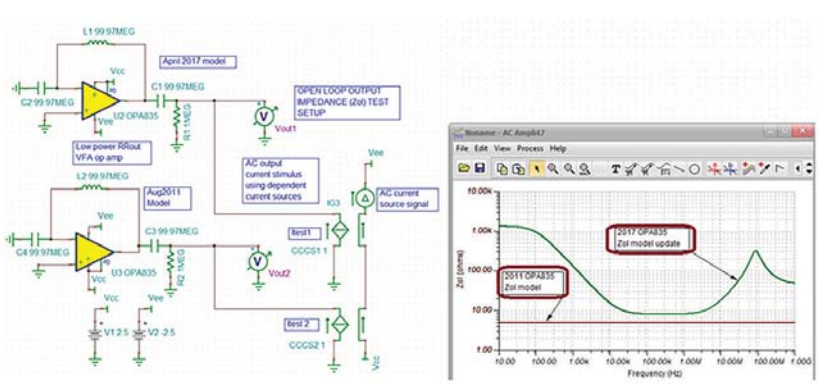
One of the modeling oversights receiving much attention in recent years is the open-loop output impedance. Early bipolar op amps and FDAs offered a very power-efficient Class AB output stage that delivered lots of current with a low dc open-loop output resistance going inductive at higher frequencies.

Those required considerable headroom for the supplies, where more recent devices have gone to RRout structures. The output stages show a considerably more involved open-loop output impedance[6] that was completely missed in much of the original modeling. They're getting updated over time as shown in the OPA835 Zol simulation of *Figure 7*, going from the 2011 to 2017 model updates. The high-frequency resonance in the RRout Zol can sometimes lead to closed-loop peaking or oscillations with relatively simple external conditions.[7]

Once again, some of the legacy models have these in the model incorrectly, where that's being repaired over time. At minimum, when using a higher-speed device in simulation, confirm that the model values match the datasheet values (from designer sims) using the approaches detailed in Reference 8.



6. This is an example of Aol gain and phase simulation using the OPA835 2011 model.



7. Open-loop output impedance simulations were performed for the OPA835 RRout low-power op amp.

The last key issue for accurate ac modeling involves the input impedances. For VFA op amps, these are usually just the common-mode and differential-mode input capacitances. Usually, these relatively low-value elements will not interact with lower-speed (<10 MHz) device applications, but they become critically important for higher-speed op amps and FDAs.

Once again, some of the legacy models have these in the model incorrectly, where that's being repaired over time. At minimum, when using a higher-speed device in simulation, confirm that the model values match the datasheet values (from designer sims) using the approaches detailed in Reference 8.

As you endeavor to select and apply modern op-amp and FDA devices, keep in mind some of these inconsistencies across vendors and modeling pitfalls that pervade the industry. Working through these can be difficult, but when armed with what to look out for, supplier application teams can be a great help. ed

THIS ARTICLE IS PART OF THE eBOOK

"What You Need to Know About Signal Path Development." To download the eBook, go to *https://electronicdesign.com/21267405.*

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AKBER ROY | CEO, RUSH PCB Inc.

Designing Noise-Free, High-Speed PCBs

It's getting more difficult to design noise-immune circuits for several reasons: An increase in integration of components due to surface-mount technology; new package designs for these integrated circuits that bump up the number of pins per package; and miniaturization of components.

Such features lead to less distance between the conductors, which raises the values of capacitance and inductance per unit length of interaction. Consequently, it increases the induced interference in adjacent conductors.

One remedy is to boost the speed of signal circuits of modern PFs as well as have a large spread in speed, from 1 MHz to hundreds of MHz, and even 1,000 MHz. For example, there are circuits that transmit a signal at a frequency of 48 MHz and at 576 MHz.

The increase in speed decreases the duration of the signal front, which, in turn, leads to problems in ensuring the integrity of the signal during its transmission. With a large spread in the speed of signal circuits, one needs to classify communication lines and evaluate their noise immunity.

Routing and Modeling in High-Speed Circuit Boards

From these features, it follows that in the early stages of design, both for routing and modeling, it's necessary to allocate transmission lines with common routing rules. To do this, you need to create a pre-topological analysis procedure.

Moreover, a post-layout analysis procedure is required, i.e., a topology-checking mechanism to identify and correct PCB layout errors.

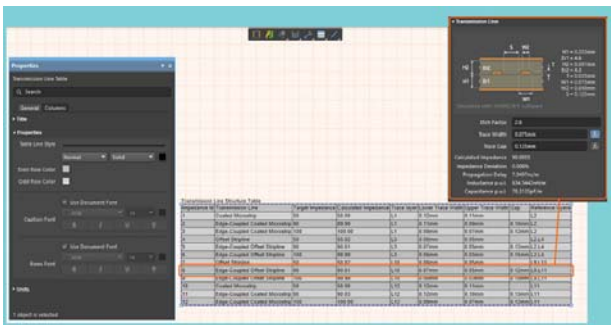
The concept of noise immunity is complex. It includes protection from external and internal pickups. This article discusses internal noise immunity.

Noise immunity of electrically short communication lines was considered according to the active-passive line model, or active-passive-active, involving minimization of interference reflections for differential transmission lines and for electrically long transmission lines. The elimination of interference in power circuits was taken into account, too.

Fixing Noise Issues in High-Speed PCBs with Altium Designer

The solution to these problems can be combined into a single technique, which includes algorithms for pre-topological and post-topological analysis.

The technique is geared to the Altium Designer package—i.e., the forced limitation of the length of conductors and the area of interaction of two or more conductors—and the HyperLynx package for checking the resulting topology. The TXline package calculates differential transmission lines *(see figure)*. The need to use various software products is due to their advantages in different areas of design.



Altium Designer's TXline package can calculate differential transmission-line configurations. *Rush PCB*

Based on the developed methodology, the circuit board of the CF subunit was designed and tested. The digital filter subunit and its circuit board can be classified as high-speed equipment, since its circuits include circuits that transmit a signal with a frequency above 300 MHz.

Design Methodology

The task of the pre-topological analysis of the noise immunity and the choice of the layout of elements forms the criteria and rules for interactive routing of a PCB, which is resistant to external and internal interference (electromagnetic and electric fields).

The initial data for pre-topological analysis are the electrical circuit diagram, element parameters (for example, number of pins, pin pitch), characteristics of the entire device (for example, supply voltage), and noise-immunity values of microcircuits.

Based on the expected area of the board and the expected volume of the product and other design features, the size of the PCB is determined. Then, based on the expected number of connections on the PCB and the parameters of the microcircuit packages, the pitch between the conductors and the accuracy class of the board is determined.

Factors to Consider in High-Speed Circuit-Board Fabrication

From the parameters of the device, namely, the supply voltage, we determine the number of layers of the developed multilayer printed circuit board (MPC).

After analyzing the electrical circuit diagram, we sort all of the circuits so that the frequency of the transmitted signal between groups differs by about 10X. Subsequently, the average length of the connection l is determined, on the basis of which we will classify the transmission line as electrically long or electrically short.

For an electrically short transmission line, additional matching of the line with the load and signal source isn't required. The voltage at all points along the length of the line at a certain point in time has the corresponding identical values.

Short lines are modeled by lumped ideal elements; their typical models are electrical capacitance or inductance. For electrically short transmission lines, the level of crosstalk must be determined.

Evaluate the Level of Crosstalk

For electrically long communication lines, it's also necessary to evaluate the level of crosstalk at the beginning and end of the line. Based on the level of interference and the values of the crosstalk coefficients at the beginning and end of the line—the pulse front—select the required distance between the conductors and the length of the allowable interaction section.

For these transmission lines, typically one must find not only the values of the linear capacitance and inductance of the communication line of two conductors, but also the intrinsic capacitance and inductance of each conductor. Eventually, it will be required to choose whether or not to match the transmission line with the signal source and with the load.

Interference in the power supply and grounding system (consumption current surges) can be eliminated by reducing the resistance, namely the inductance of the power bus. Particular attention should be paid to the installation of decoupling capacitors on the board to power the IC. The capacitors protect microcircuits from power surges.

Follow these rules when laying out decoupling capacitors on the MPC:

- Place decoupling capacitors as close as possible to the power and ground pins of the microcircuits.
- Wide, short conductors should be used between the plated hole and the pad of the capacitor.
- The plated hole should be next to the pad, or directly in the pad (microvia).
- If the metallized vias of decoupling capacitors carry currents opposite in direction, then these holes should be located at the minimum possible distance from each other (preferably no more than l mm).

It's possible to reduce the inductance of the power supply and grounding system by properly forming the MPC structure. The power layers and return layers (ground layers) must be placed as close as possible to each other so that the capacitance of the resulting planar capacitor is larger (which, in turn, leads to a decrease in the inductance of the power supply and ground).

The formation of the MPC structure will further simplify the task of assessing its noise immunity.

The power and ground conductors should be as wide and short as possible. We will determine the width of the conductors based on the values of the current flowing through the conductor and the allowable voltage drop on the power bus.

Now let's go to the analysis of transmission lines of information signals. By selecting any of the formed groups, we determine the critical length of the communication line *(l_{KP})*. If the ratio $l/l_{KP} \leq 0.5$, then this transmission line can be classified as electrically short. If $l/l_{KP} > 0.5$ and < 0.9, the given transmission line is neither electrically short nor electrically long.

With this technique, for such transmission lines, it's possible to increase the signal's minimum edge by introducing additional elements (resistors or capacitors) into the circuit in case the crosstalk value doesn't satisfy the condition.

It's important to remember that an increase in the front must be agreed upon with the developer since this degrades circuit speed. If $l/l_{KP} > 0.9$, the transmission line is electrically long. For electrically long transmission lines, designers must set the characteristic impedance and determine the margin of the transmission line's internal noise immunity. By choosing the parameters of the transmission line, the specified and calculated wave impedances must be equal.

Level of Crosstalk from Neighboring Conductors

If the wave impedances are equal, we analyze the crosstalk level from neighboring conductors to match the transmission line with the signal source and load.

Differential transmission lines transmit high-frequency signals so that they can be attributed to electrically long communication lines. Next, set the differential wave impedance and determine the margin of the transmission line's internal noise immunity.

Before designing, it's necessary to determine the type of the differential transmission line. For example, is it a stripline or microstrip line? The advantage of striplines is that mode velocities are the same and there's no interference at the far end of a passive line (unlike a microstrip line). However, using surface mounting for the stripline requires vias.

This effect on transmitting differential signals must be evaluated with special software tools. And it's necessary to evaluate all advantages and disadvantages of one or another option and choose the most suitable for the design being developed.

Differential Transmission Line

Set the differential transmission line's parameters (distance between conductors, conductors' width, and distance between the conductors and the screen layer). For the given parameters, calculate the differential wave impedance.

If the value of the calculated impedance and given impedance are the same, calculate the level of internal noise and transmission-line length. To eliminate skew when transmitting a differential signal, calculate the allowable difference between the conductors' lengths in the communication line.

Method for Matching the Designed Transmission Line

The final step is to choose a method for matching the designed transmission line with the load and signal source. In some cases, if there's a difference in the design of one line of the differential pair, an alternating component may appear in the general signal.

In this case, it's necessary to coordinate the differential signals and general signal, which can be done with a with a U- or T-shaped switching circuit.

Pre-topological analysis of the FY CF yields a set of parameters of various

communication lines, which at this stage provide noise immunity for the product, the minimum crosstalk values, and good traceability of the entire circuit. These parameters let engineers correctly arrange elements on the PCB.

If some communication line's parameters lines aren't available during routing (e.g., the length of the interaction section of adjacent conductors), the PCB's parameters must be adjusted. For example, increase the number of signal layers. Then, in accordance with the selected parameters, recalculate the wave impedances of the line's gears.

Post-Topological Analysis

Post-topological analysis checks the fulfillment of specified rules for the design of PCBs and parameters of printed conductors.

Initial data for this analysis is the finished topology and parameters of the transmission lines calculated earlier. Since Altium Designer doesn't allow for interactive control of the transmission lines' lengths, report the lengths of all conductors and compare them with previously calculated ones.

For differential-signal transmission lines, it's necessary to monitor the lengths and control the difference between the lengths of conductors in a pair to eliminate skew. If any conductor exceeds the allowable length, the circuit's topology must be corrected.

Troubleshooting methods:

- Partially rearrange the circuit elements. It's possible to shorten the interaction section and the conductor.
- Reroute the conductor. It should be placed further from the offending conductor.
- If there's not enough space to reroute the conductor, it can be moved to another signal layer.

After tracing and manually checking the topology, export it to HyperLynx. To evaluate crosstalk and the critical link length, designers must do an automatic quick analysis, a fast analysis technique based on an expert algorithm.

An expert algorithm that identifies crosstalk nets makes worst-case assumptions to catch all crosstalk nets. This means the Standard IC Model is used if no transmitter model is in the circuit. The algorithm assumes all chains are inconsistent.

The sum of the intensity of the two strongest aggressors also is displayed in the report file, as this is the most typical. To generate the Crosstalk Strengths Report, an expert algorithm uses the transmitter edge speed and the transmission-line interference information.

It's necessary to set those values that were determined earlier, at the stage of pre-topological analysis, and which represent the worst case. ed

STEVE TARANOVICH | Contributing Editor

What's the Difference Between **EMI and EMC in Electronic Designs?**

Electromagnetic interference and electromagnetic compatibility are both important considerations when designing and working with electronic components and systems.

It's incumbent on electrical/electronic designers and troubleshooters to understand the difference between electromagnetic interference (EMI) and electromagnetic compatibility (EMC).

EMI is caused by electromagnetic emissions that may disturb the function of electronic devices and radio-frequency (RF) systems. Such devices and systems must be properly shielded from electromagnetic radiation for them to perform optimally. EMC measures how well these devices and systems can perform in the presence of any disruptive EMI.

Defining EMI and EMC

EMI definition[1]

EMI is typically present as undesirable noise in any electrical/electronic system. EMI occurs due to electromagnetic emissions that disturb functionality in radio-frequency (RF) or electronic devices. One way to protect the optimum functionality of systems and devices is the use of proper shielding from electromagnetic radiation. EMC will measure how these devices/systems will function properly in a disrupting EMI environment.

Essentially, EMI is undesirable noise in a system that disrupts electronic, electrical, and RF systems.

There are four kinds of EMI:

- *Conducted EMI:* This type of EMI, which flows through wires, occurs via physical contact with the source of that EMI.
- *Differential-mode EMI:* This low-frequency EMI will flow in an opposite direction through adjacent wiring.
- *Common-mode EMI:* This high-frequency form of EMI flows in the same direction through one or more electrical conductors.
- *Radiated EMI:* This is the most common type of EMI. It's caused by radiating electromagnetic fields. Common signs of radiated EMI include "snow" on TV monitors and static noise on AM/FM radio receivers.

EMC definition[1]

EMC of an electrical, electronic, or RF device has two features:

- The capability of working properly while in the presence of electromagnetic radiation.
- The capability to not generate any additional EMI that may affect the proper operation of any other devices nearby.

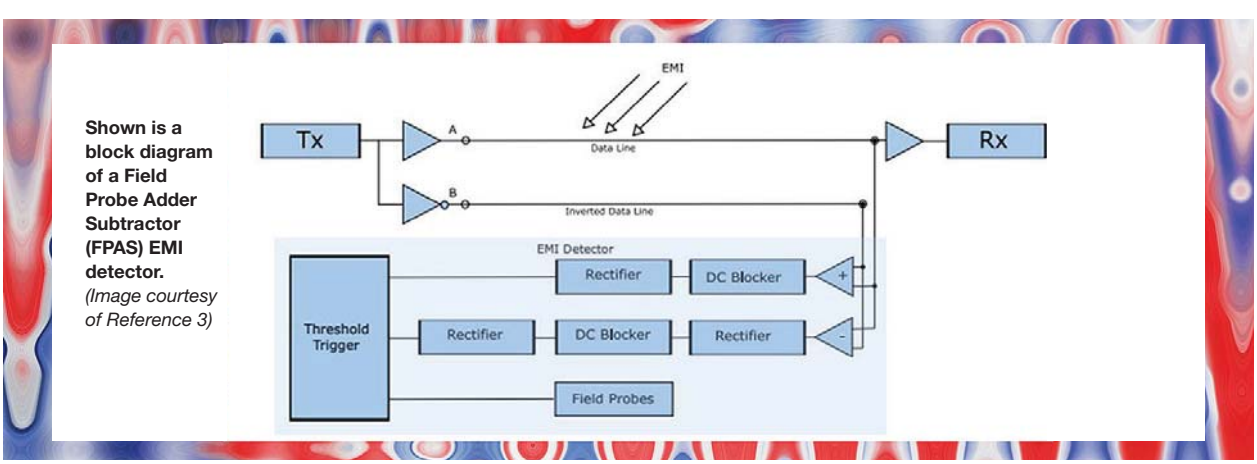
The EMC of any device may be improved by using a clever design and shielding, along with EMI filtering. A device's EMC can be measured via compliance testing by using a dedicated test system that's composed of antennas, near-field probes, and spectrum analyzers.

EMC testing may prove to be expensive. However, it's essential to ensure that an electrical/electronic design will function as expected and will not generate disruptive EMI.

EMI and EMC Compliance

EMI and EMC compliance standards are not uniform worldwide. Myriad different regulatory bodies globally will each have their own specific standards.

An example is the compliance standards in the European Union (EU) that differ from those in the United States. To further complicate matters, the U.S. military employs far more strict standards



Shown is a block diagram of a Field Probe Adder Subtractor (FPAS) EMI detector. *(Image courtesy of Reference 3)*

than do commercial industries. Commercial compliance standards will often vary depending on the specific industry and the end use of any device.

EMI Detector Design

All electrical/electronic/programmable electronic (E/E/PE) devices can generate, and may also be vulnerable to, electromagnetic disturbances (EMD). EMD may create critical errors in an electronic system.

A correct and safe operation can be achieved via increasing demand for safety- and mission-critical systems. A combined expertise in the engineering disciplines of EMC, risk management, and functional safety have become quite important.

The IEEE Standard 1848-2020 focuses on measurements and techniques that could be used to make a system quite resilient to EMI via design.

Wired communication channels still play a critical role in modern-day communication systems. It's key for designers to focus on their dependability. Many hardware- and software-based methods are designed to render a wired communication channel to be EMI-resilient through proper design.

Some hardware-based techniques involve detection of EMI and frequency, spatial and time diversity. There are also software-based approaches that include error detection codes (EDCs) and error correction codes (ECCs). The key goal of these techniques and measures is to be able to detect and correct EMI-related bit errors in the communication channel.[2]

A Field Probe Adder Subtractor (FPAS) EMI detector was proposed in Reference 3 *(see figure)*. This method can detect the EMD induced in a wired communication channel.

This kind of detector is used at the receiver end and will generate a warning when an EMD disrupts the data transmitted. This type of warning may be used by the system to request a retransmission of data or shift the system into a safe state. The Adder & Subtractor (A&S) EMI detector can't detect EMI at those EMI frequencies, which are an integer multiple of the detector sampling rate.

Field probes are able to characterize the electromagnetic (EM) environment and detect the EMD. One problem with these types of probes is that conventional field probes are slow and costly. A possible remedy for this is the received signal strength indication (RSSI)-based fast probes that can operate as an EMI detector.

Such probes will produce dc output voltages that are able to be used to measure the field envelope. They have a flat frequency response along with an improved sensitivity at low frequencies, enabling them to readily detect EMI in a harsh EM environment.

The FP EMI detector will generate a large number of data false positives (DFPs), which in some cases compromises the detector availability. However, the FPAS EMI detector can overcome this limitation with the A&S EMI detector that implements the Field Probe (FP) EMI detector. However, the FPAS EMI detector will continue to produce a limited number of DFPs. Studies are ongoing to reduce DFPs.

EMC Quasi-Peak Detector

Quasi-peak detectors (QPDs) are a weighted form of peak detection.[4] The measured value of the QPD falls as the repetition rate of the measured signal increases. QPD is a method of measuring the "annoyance factor" of a signal. This is just like listening to a radio, where every couple of seconds you hear a "pop" related to noise.

A majority of conducted and radiated limits in EMC testing are based on the quasi-peak detection mode. A quasi-peak detector will weigh signals according to their repetition rate. This is a method of measuring their "annoyance factor." It's achieved by having a charge rate that's much faster than the discharge rate. So, as the repetition rate ramps up, the QPD will not have enough time to discharge as often, leading to a higher voltage output (i.e., response to a spectrum analyzer).

For continuous-wave (CW) signals, the quasi-peak and peak responses will be the same. In addition, a quasi-peak detector will also respond, in a linear manner, to different amplitudes. Low-repetition-rate, high-amplitude signals can produce the same output as low-amplitude, high-repetition-rate signals.

During measurement, QPD readings will always be less than or equal to peak detection. Quasi-peak readings are far slower (by two or three orders of magnitude as compared with peak). It's quite common to initially scan using peak detection, and then, if that is only marginal or fails, switch and run the quasi-peak measurement against the limits.

Summary

EMI isn't a desirable phenomenon, and EMC is a set of practices and rules that will control it. Without EMI, EMC isn't necessary; without EMC, EMI will ultimately cause design problems.

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Ad Index

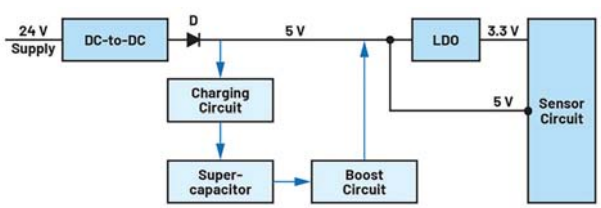
FREDERIK DOSTAL | Power-Management Technical Expert

Compact UPS with Supercap

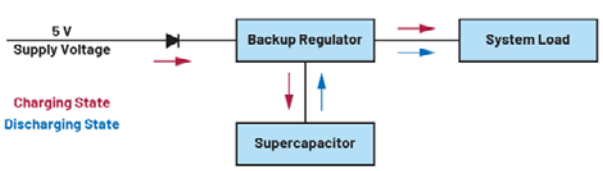
Continuous supply voltage via an uninterruptible power supply is crucial for a number of applications, but it can be tough to ensure at all times. This Idea for Design offers a reliable, compact solution that's easy to integrate.

In many applications, it's important for the supply voltage to be continuously available no matter what the circumstances. This isn't always easy to ensure, though. A new concept can provide an optimal solution for an uninterruptible power supply with an extremely compact design.

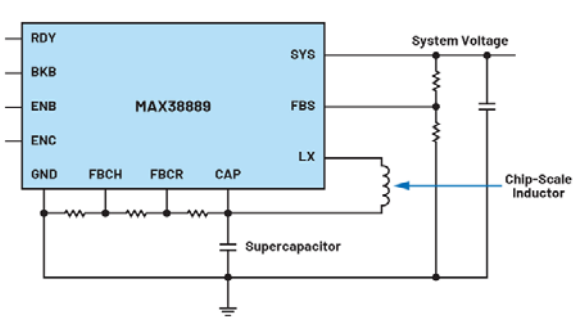
Several applications require an uninterruptible power supply. One example is the RAID system for redundant data storage, which must be protected so that no data is lost in the event of a power failure at an inconvenient time, such as during data backup activity. Systems with real-time clocks also must be supplied continuously with power. This can come from a battery or another backup solution. Other applications include telemetry apps in the automotive sector and systems for administering medications—for example, controlled insulin pumps used in the healthcare sector.



1. Shown is a typical application for an uninterruptible power supply.
Images courtesy Analog Devices



2. The Continua backup concept has numerous integrated system functions.



3. This implementation features a tiny Continua backup solution with the MAX38889.

Figure 1 shows a typical industrial application for an uninterruptible power supply. Here, an industrial sensor is supplied with power. The reliability of the system mainly depends on this sensor's power supply.

A linear charge regulator IC is used to charge a supercapacitor when there's available system voltage. If the system voltage drops, the energy from the energy-storage system is raised to the required supply voltage level with a boost regulator.

This system works well, but it's difficult to implement because many different energy converters are needed. Moreover, in many applications, it's important that no energy flows from the energy-storage system back to the power supply *(depicted in Fig. 1)*.

As shown in the left side of *Figure 1*, the supercapacitor should only power the sensor circuit and not any other electronics that may be attached to the 24-V line. The energy-storage system is normally designed to supply the local load and not the complete system attached to the 24-V supply voltage. This makes diode D in *Figure 1* necessary.

Figure 2 shows a new concept supported by the MAX38889 from Analog Devices (ADI). It's a highly integrated backup solution called Continua for power rails up to 5 V. A single IC with a few passive external components is all that's required. The MAX38889 has an integrated half-bridge, operated alternately in highly efficient buck and boost modes.

A complete, operable circuit is illustrated in *Figure 3*. The logic and the power switches are all integrated, so just a small external chip-scale inductor and a few backup capacitors are required, apart from the supercapacitor.

The integrated high-side power switch is executed with the True Shutdown technology developed by ADI. As a result, the system voltage can be separated from the CAP voltage so that no current flows from the CAP to the system if the CAP voltage is ever higher.

While plenty of backup solutions for various voltage and current ranges exist on the market, the compact MAX38889 Continua backup solution can easily be added to the 5- or 3.3-V supply line with minimal development and implementation effort. It also offers high conversion efficiency of up to 94% in charging and discharging modes to minimize the size and cost of the energy storage.

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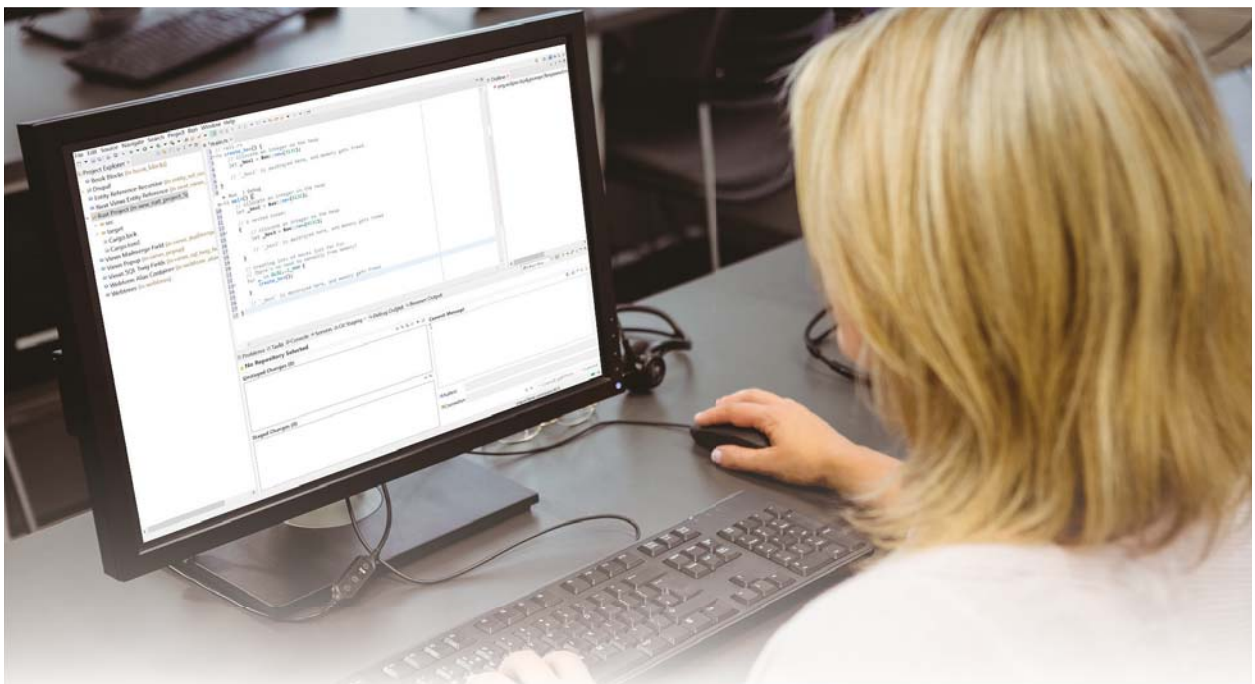
BILL WONG | Senior Content Director



Delivering Reliable, Rugged **Rust**

Though it's a relatively new programming language, Rust is now ready for prime time.

Rust is a somewhat new programming language that's designed to reduce the number of common errors by providing a more restrictive and descriptive programming environment. It's built to compete with C in performance while significantly minimizing the number of errors a programmer might accidentally include in an application.

Several aspects of Rust make it more robust than C, such as tracking memory utilization, including pointers. The Rust borrow checker forces the programmer to explicitly control the use of memory references, thereby preventing many of the most common errors found in C programs.

Though Rust is a general programming language, it can also be used for bare-metal and operating system implementations where C is dominant. The challenge in using Rust these days is that the open-source project continues to evolve the language. While that's great for improving the language, it can wreak havoc on programmers who need to support applications on a long-term basis.

Rust implements much of its error checking at compile time using static analysis. MISRA C also uses static analysis, but C doesn't provide the ability to describe how things like memory are controlled with respect to pointer usage. MISRA C is used in markets such as automotive, although Rust is much more robust in allowing programmers to define how memory references are manipulated. Rust still lacks features like contracts found in Ada/SPARK, but Rust's memory reference tracking is superior.

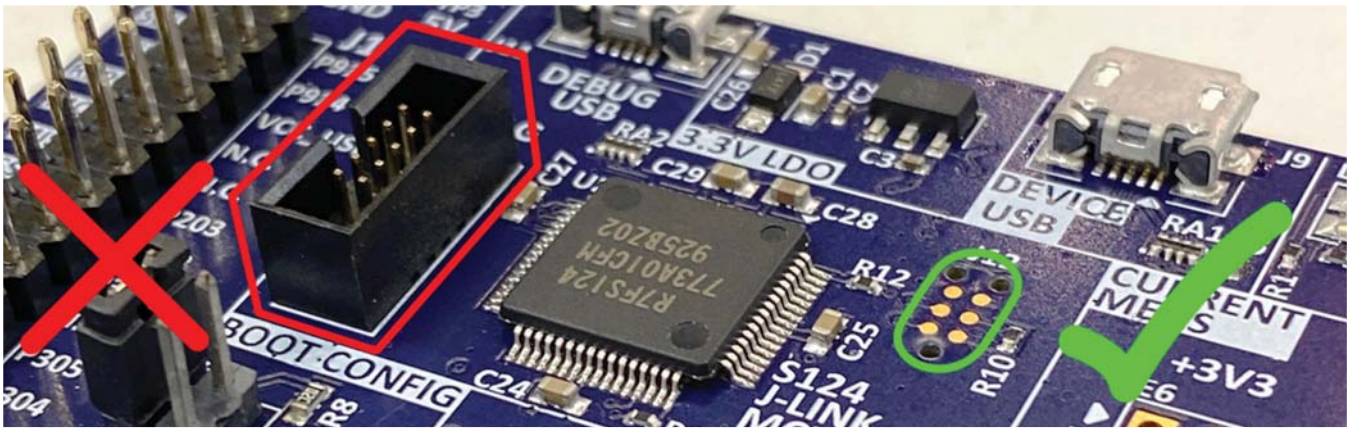
Two companies, Ferrous Systems and AdaCore, are at the forefront of Rust support for applications that need qualified versions of the compiler and tools to meet standards requirements. Standards include ISO 26262 and IEC 61508 as well as the more demanding DO-178C, ISO 21434, and IEC 62278.

Ferrous Systems' solution is called Ferrocene, and AdaCore has the GNAT Pro for Rust, which is based on its GNAT Pro tool series that supports C, C++, Ada, and SPARK development. These tools target high-quality, high-reliability software applications but are equally suitable for developing any embedded application. AdaCore provides Ada-Rust bidirectional bindings that allow for mixed language application implementations. AdaCore is an ISO 9001-compliant and NIST SP 800-171 organization targeting SLSA Build Level 3 compliance.

The main difference between the open-source version of Rust and the commercial versions are the level of support, including bug fixes and long-term support. Both companies have a track record of supporting safety and security environments from automotive to avionics.

Using Rust can be a challenge given C's dominance, but there are Rust drivers in Linux now. Rust is ideal for implementing drivers, operating systems, and bare-metal applications where high-quality software is paramount to safety and security.

Tag-Connect



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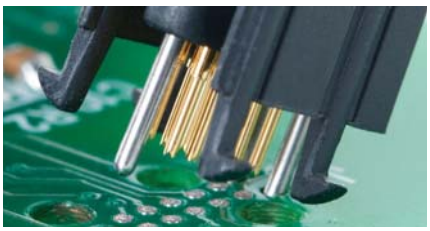

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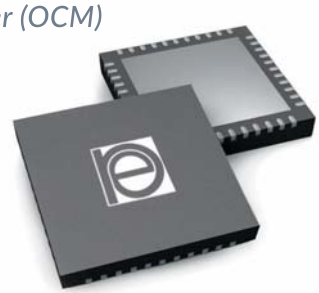

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