

What Signal-Path Developments are Still Missing from Textbooks?

Here's what you didn't learn in school, such as how to really combine the distortion terms in cascaded amplifiers.

Industry amplifier development groups continue to improve on devices and analysis techniques, publishing those in datasheets, application notes, industry articles, etc. But these rarely find their way into textbook updates. Read on for a representative sample of what you might have missed in your EE education.

The classic gain bandwidth product (GBP) idea was always an oversimplification. One simple plot yields much closer SSBW versus gain prediction for any voltage feedback amplifier (VFA) or fully differential amplifier (FDA).

The well-known GBP model predicts that the closed-loop small-signal bandwidth (SSBW) will simply be the GBP divided by the noise gain (NG). The NG is the inverse of the voltage divider from the output pin back to the feedback input pin(s). In a non-inverting VFA design, the NG will be the same as the desired signal gain.

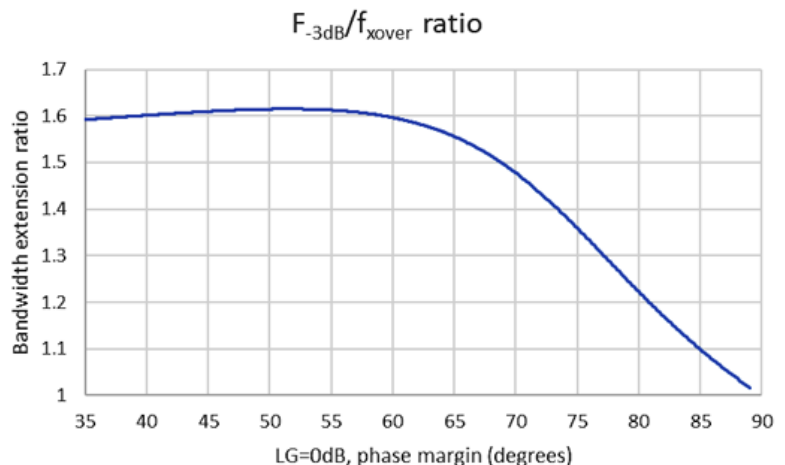
It doesn't take very long in characterizing SSBW over gain for VFA amplifiers to find out that this model is not very close at lower gains. The model is assuming a single-pole loop gain (LG) condition, where that's hardly ever the physical case. A second-order model gets much closer, but it too is still an approximation for most modern VFA op amps and/or FDAs.

Almost any modern (but accurate) VFA model can be used to illustrate these effects—even allegedly unity-gain stable devices. All IC designers (and most marketers) know that designing a unity-gain VFA op amp for about 65-deg. phase margin will give far higher closed-loop SSBW than the GBP might predict ($\approx 1.55X$). A nominal unity-gain, 65-deg. phase-margin design is very common, yielding an approximate closed-loop Butterworth design (at least second order by definition).

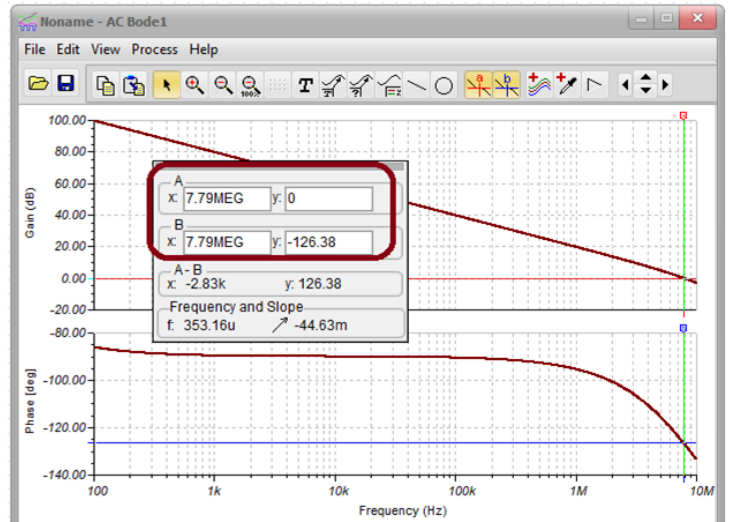
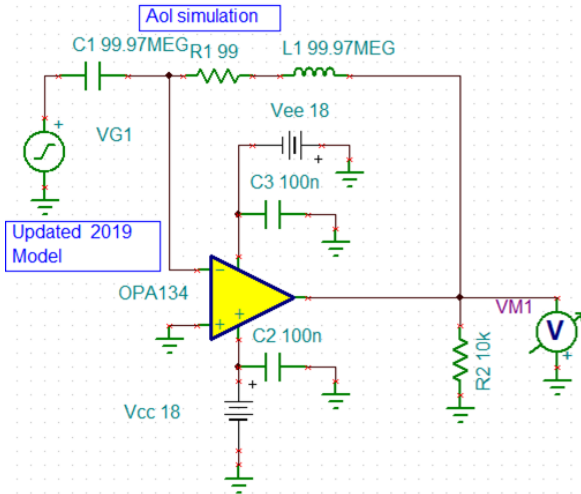
The approach to generate *Figure 1* was to introduce a NG zero to a single pole Aol analysis by adding a tuning capacitor at the inverting node to ground for an inverting op-amp configuration. Solving for the loop gain (LG) = 0-dB point, as that zero is reduced in frequency (ramping that capacitor up), will yield one quadratic.

Then, at that same capacitor value, the LG phase margin is used to solve for the closed-loop second-order Q, and subsequently the resulting F-3dB. The ratio of that F-3dB to the LG = 0-dB frequency is formed to get *Figure 1*. Note that for phase margin < 65 deg., the closed-loop response will also be peaking.¹

A good example can be shown using the [OPA134](#) simulation model. *Figure 2* shows the Aol gain and phase simulation,¹



1. The SSBW extension over the LG = 0 dB (fxover) phase margin.



2. Open-loop gain and phase simulation for the OPA134 VFA op-amp model.

which would be the same thing as the LG plot for a unity-gain configuration.

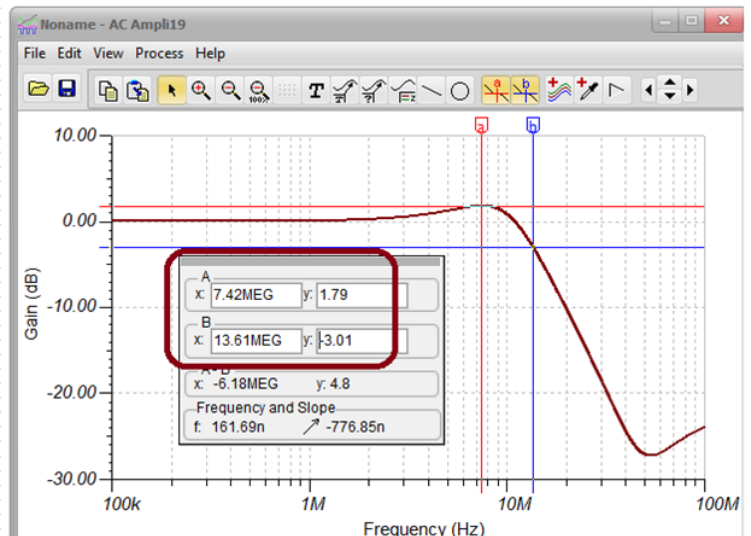
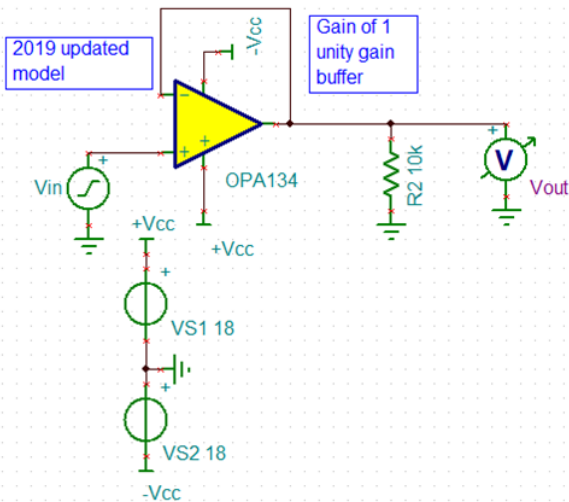
This simulation shows 54-deg. phase margin, which, from *Figure 1*, should give a close-loop gain of 1 SSBW extension to $7.79 \text{ MHz} \cdot 1.61 = 12.54 \text{ MHz}$. The gain of 1 simulation in *Figure 3* shows a 13.6-MHz F-3dB with 1.8 dB peaking. Ideally, a 54-deg. phase margin should be giving about 1.2 dB peaking (*Fig. 2*)¹, so these results are close, but not exact, to the expected response shape due to higher-order poles in the model not captured by this second-order analysis.

The curve of *Figure 1* adds a lot to our understanding of the closed-loop SSBW over gain versus the simple GBP model that would have predicted only 7.8-MHz F-3dB unity-gain bandwidth.

How do you really combine the distortion terms in cascaded amplifiers or amplifier + ADC systems? Legacy power summing calculations are quite incorrect.

One of the fundamental questions in an analog-to-digital converter (ADC) driver application is how low do the harmonic-distortion (HD) terms need to be coming into the ADC to only slightly impair its performance. Numerous early efforts at this simply added powers as if the individual distortion terms were in a 45-deg. (quadrature) relationship.

In fact, the individual input distortion terms must be added linearly to those same terms for the ADC itself. Extensive testing with individual FDAs ([THS4509](#)) and high-speed ADCs ([ADS5500](#)), where each device was separately character-



3. Gain of 1 OPA134 simulation showing 13.6-MHz F-3dB and 1.8 dB peaking.

ized then combined, proved that the individual distortion terms add in phase as voltage vectors.² The math combining two cascaded stages for each distortion term is shown as Eq. 1:

$$SFDR_{system} = -20 \cdot \log \left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}} \right) \quad (1)$$

This is written as spurious-free dynamic range (SFDR), but actually the HD2 and HD3 (etc.) terms would be combined individually. Legacy literature would often report the combination as a total harmonic distortion (THD) power combination as in Eq. 2, which is totally incorrect, (page 43, ref. 3):

$$THD_{system} = \sqrt{THD_{Amplifier}^2 + THD_{ADC}^2} \quad (2)$$

Much more recent bench testing of a two-stage amplifier ([THS3217](#)), where the input and output stages were measured separately, then combined in cascaded stages, showed these same results (*Fig. 4*). Here, the input D2S stage was tested over frequency with a 2 V p-p into 200-Ω load, while the OPS stage in that same unit was tested separately producing 5 V p-p into 100-Ω load.

These separate measurements were combined using Eq. 1 to predict the cascaded distortion. Then the same part was measured in a cascaded configuration producing the same swings and loading at each stage. Clearly, Eq. 1 appears to correctly combine the cascaded distortion performance.

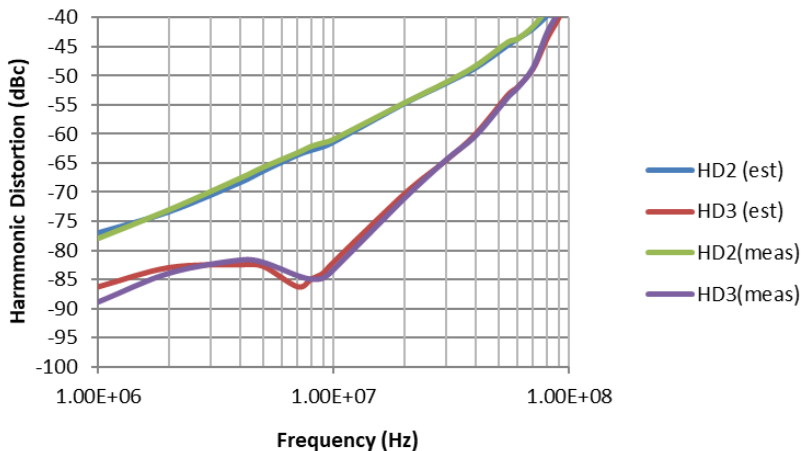
Imagine coming into an ADC (or second amplifier stage) with a large fundamental carrier that has its own HD2, HD3, etc., harmonic distortion terms. The ADC (or second amplifier stage) will generate its own harmonic terms from the large fundamental and combine those “in phase” with the terms coming into its input. This makes the problem of minimal ADC degradation much more difficult than predicted by the legacy (and incorrect) power addition assumption of Eq. 2.

Sweeping Eq. 1 for a fixed ADC SFDR term and an improving input-signal SFDR term shows a slowly closing gap in *Figure 5*. For any ADC spurious term reported, degrading it by less than 1 dBc requires an input term at least 20 dB lower than the ADC reported number. This example was for a -75-dBc ADC spur, but it generally holds for any starting level.

The fully differential amplifier (FDA) combines a differential + common-mode (CM) control loop. Hiding inside some FDAs is a very low noise active balun capability.

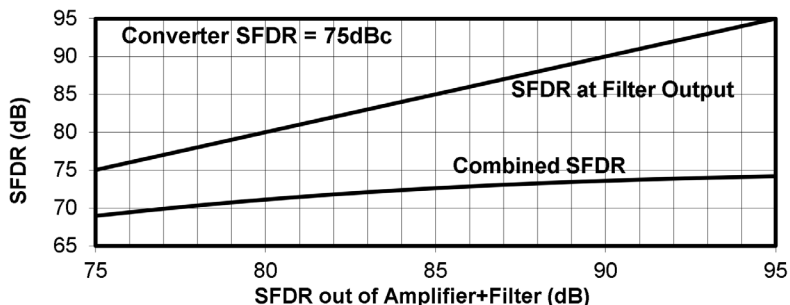
The first FDA—the [AD8138](#)—emerged in 1999. It was an ideal solution for converting single-ended signal paths to the differential drive required by the high-speed pipeline ADCs that had started to emerge in the mid-90s. As FDA bandwidths increased (far beyond 4 GHz today), the need for a matched input im-

THS3217 HD total device

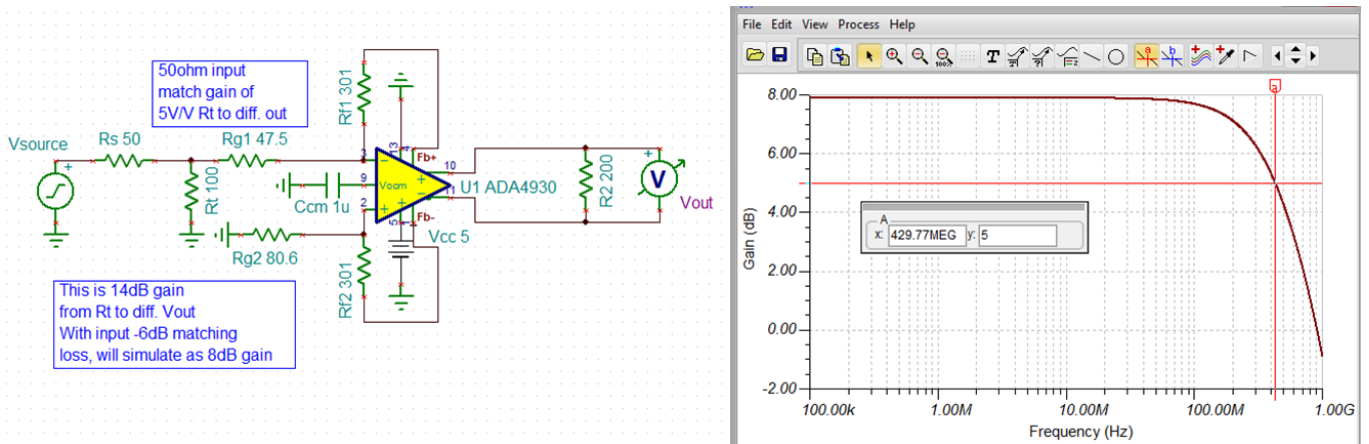


4. Calculated and measured two-stage amplifier distortion comparison.

Combined SFDR



5. Combining spurious at the ADC input and the ADC spurious into a final result.



6. Single-to-differential dc-coupled gain of 5 V/V with a 50-Ω input match using the ADA4930 FDA.

pedance was obvious.

However, the FDA's two-loop nature rendered the solution for the required resistors to provide that single-ended impedance match, as well as the desired differential gain, very elusive. In fact, both National Semiconductor and Analog Devices capitulated on that analysis⁴ and developed solutions that were in fact iterative to simultaneously match to some source impedance and deliver the desired gain.

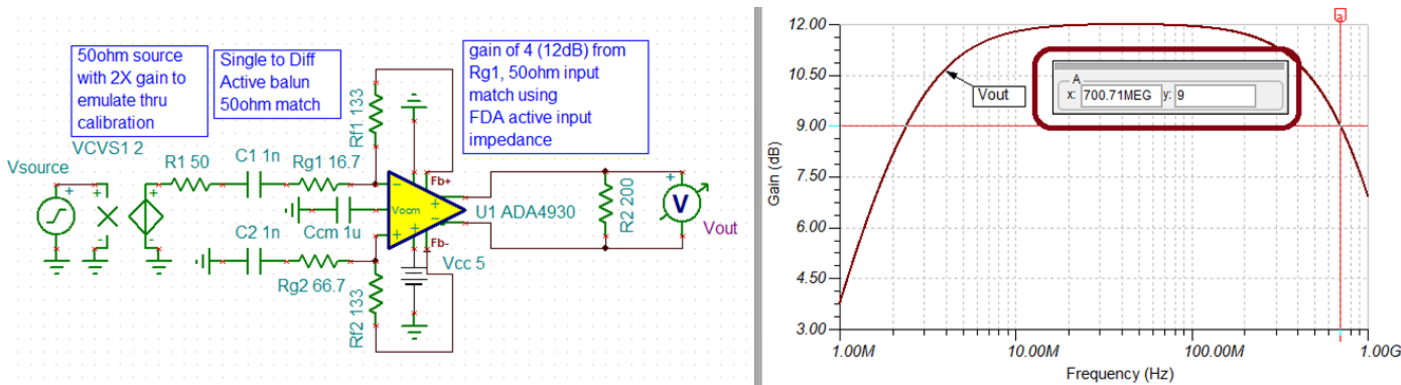
Sinking deep into an algebraic morass in the 2012 timeframe, I extracted a closed form solution for the input resistor to ground (R_t) as Eq. 3:

$$R_t^2 - R_t \frac{2R_s \left(2R_f + \frac{R_s}{2} A_v^2 \right)}{2R_f(2 + A_v) - R_s A_v(4 + A_v)} - \frac{2R_f R_s^2 A_v}{2R_f(2 + A_v) - R_s A_v(4 + A_v)} = 0 \quad (3)$$

Figure 6 shows an example gain of 5-V/V design, first picking $R_f = 301 \Omega$, then solving for R_t and subsequently the two R_g values to give a 50-Ω input match. The FDA CM loop will move the CM input voltages with the input signal to generate the output voltage on the non-signal input side. This has the effect of making the apparent impedance looking into R_{g1} higher than the physical value (100-Ω active impedance in Figure 6).

With R_t solved, the series input gain resistor is then resolved for a selected R_f value.⁴ While Eq. 3 looks too complicated to be either correct or useful, it's in fact both. In the original work, I tested these results against both the ADI and NSM tools, delivering identical results for the required R values. Starting with a selected feedback R_f value is required to apply current-feedback-based FDAs.

So, what does this equation offer over the equally effective iterative approaches? Recalling that this equation is for the (kind of extra) resistor to ground (R_t) at the input to attain an impedance match, what if we solved the denominator expression for a zero value? That will eliminate this extra R_t resistor to ground, leading to the lowest noise ac- or dc-coupled matched input impedance single-to-differential FDA interface.



7. Active balun single-resistor match to 50 Ω and a gain of 4V/V to the differential V_{out} .

Unlike typical magnetic baluns, commonly used in higher-frequency RF channels, this solution can be truly dc-coupled. This “active balun” solution offers a new signal-path processing option for single-to-differential requirements up to an ADC.⁵

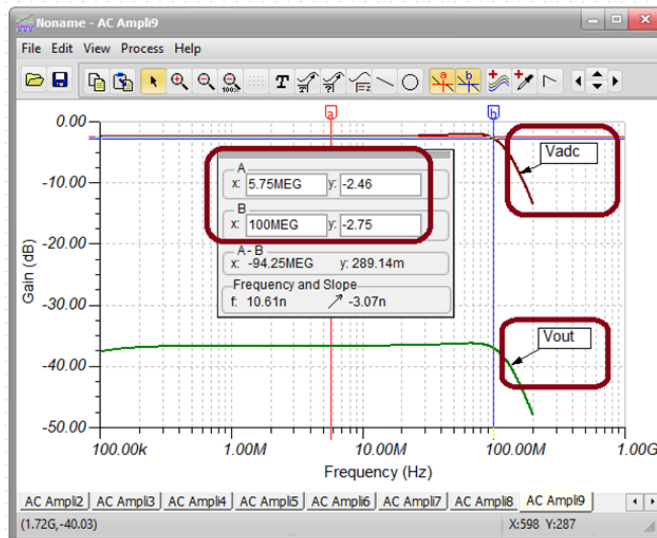
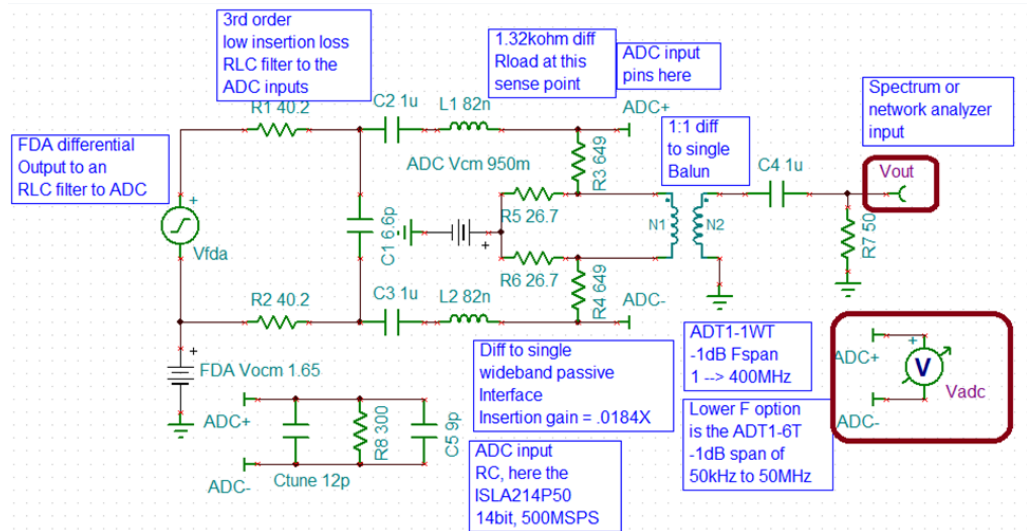
While the [ISL55210](#) would be the lowest-noise ($0.85\text{nV}/\sqrt{\text{Hz}}$) device to apply here, *Figure 7* shows an example design using the $1.4\text{-nV}/\sqrt{\text{Hz}}$ noise [ADA4930](#). Here, the 2.4-MHz , lower F-3dB is set by the 1-nF blocking caps and could be lowered using higher capacitor values.

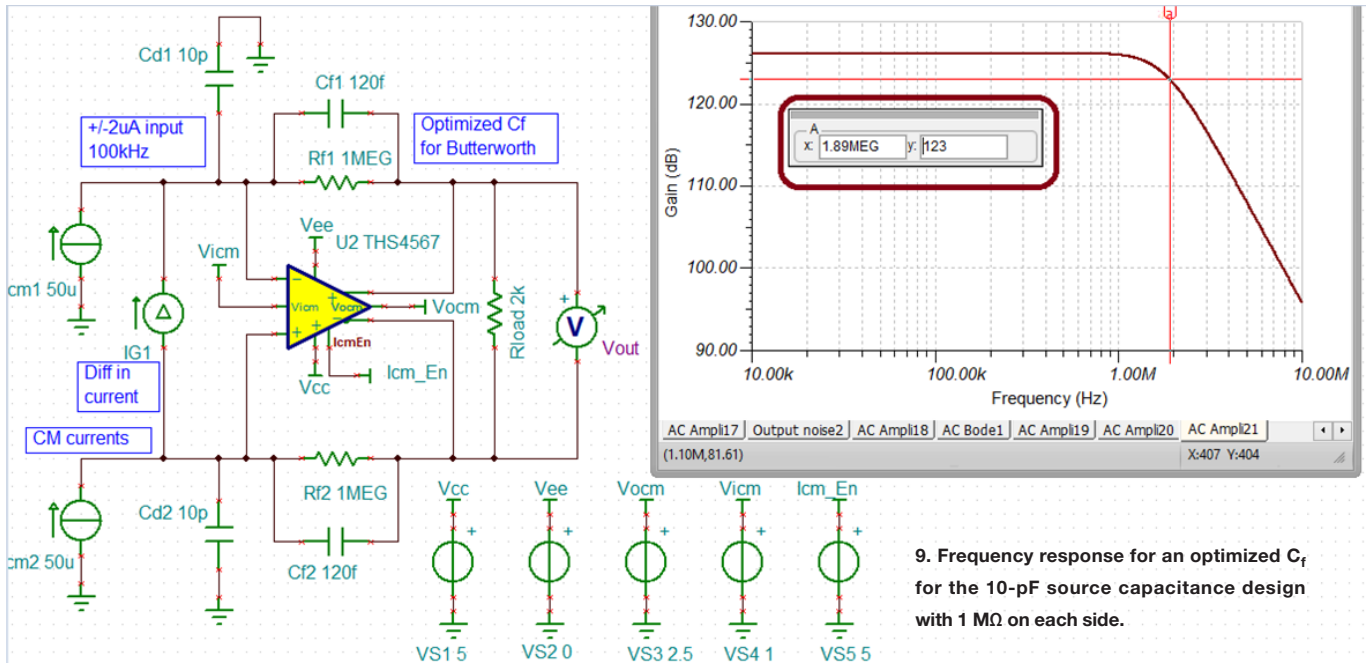
This 12-dB gain stage (from Rg1) gives about 200-MHz flat span with 700-MHz F-3dB. That $Rg1 = 16.7\ \Omega$ is in fact providing a $50\text{-}\Omega$ input match using the active impedance feature of a single-to-differential FDA stage.⁵ For this to work broadband, the internal CM loop bandwidth must be on the order of the differential loop—they are for these higher-speed FDAs. That CM loop bandwidth is much higher than the reported bandwidth from the control pin to the output CM voltages.

Running an output differential spot-noise simulation shows only $4.2\text{nV}/\sqrt{\text{Hz}}$; the input refers to about 1 nV for this gain of the 4-V/V stage. The input referred noise here is actually less than the specified 1.4-nV FDA input voltage noise, since the signal gain of 4V/V is slightly more than the noise gain of 3 V/V . This 1-nV input spot noise translates into 7.8-dB noise figure for a $50\text{-}\Omega$ source and $T_a = 17^\circ\text{C}$.

How would you really interface from an FDA to an ADC while also implementing a direct response shape or har-

8. Example RLC filter interface with wideband passive output sense path.





9. Frequency response for an optimized C_f for the 10-pF source capacitance design with 1 M Ω on each side.

monic distortion measurement with the ADC input pins down to -110 -dBc levels?

The significant effort devoted to delivering a very-low-distortion input signal to an ADC, with some desired frequency-response shape, then combines with the ADC distortion and frequency response terms. Differential probes can be used at the ADC inputs to verify the response shape or step response, but they don't have the dynamic range to extract out the distortion performance for the best interfaces.

Starting from a simple RLC interstage filter⁷ design (adapted to differential for an FDA-to-ADC design), that last parallel resistor across the ADC inputs can be split into a very high-dynamic-range differential to single-ended test port to measure the response shape and harmonic distortion right at the ADC inputs.

These ideas show up in a fully developed and tested evaluation (EVM) boards using a 4-GHz low-noise FDA ([ISL55210](#)) with a 14-bit, 500-MSPS ADC.⁸ The aim was to provide a flat 100-kHz to 100-MHz gain of 15-dB interface with minimal signal-to-noise ratio (SNR) and SFDR degradation over the ADC-only specs. That was achieved indicating the SFDR at the ADC inputs was ≤ 110 dBc through 100 MHz driving 1.8 V p-p differentially at those ADC input pins.

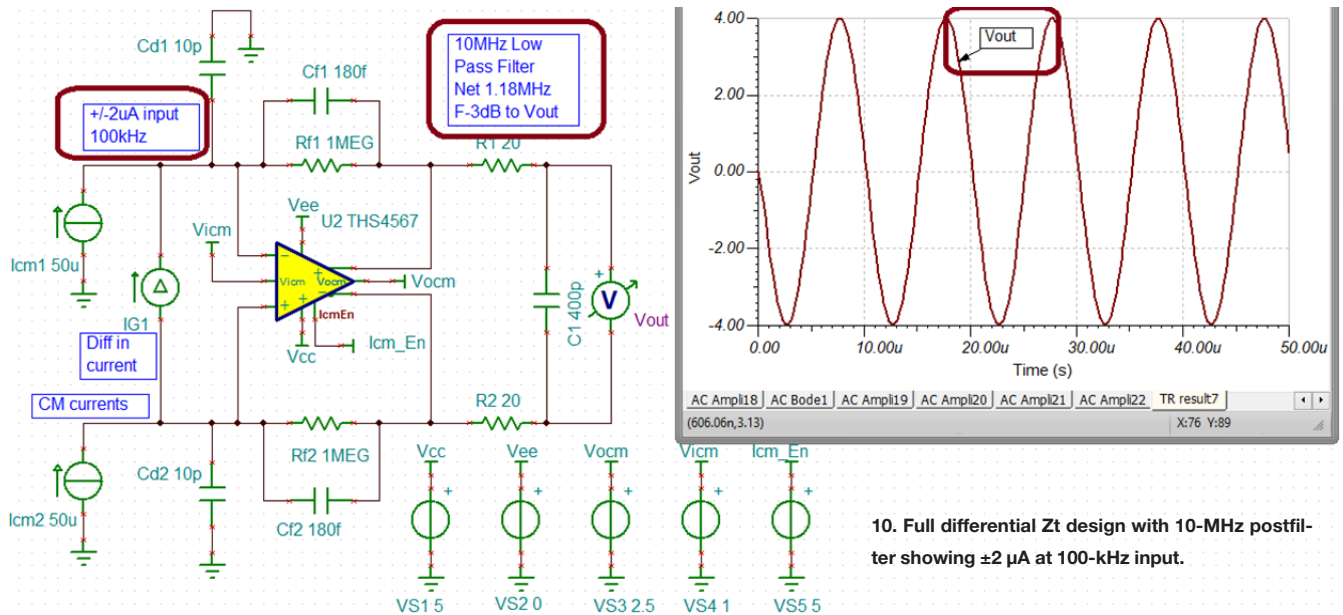
The RLC filter design was necessarily a bit iterative as both the board parasitics and ADC input C were somewhat uncertain. The RLC filter design intentionally targeted a final differential C at about 2X the ADC reported internal value to enable some range for tuning the final external C value down.

That proved trivial as the exact response shape to the ADC inputs (while sampling) was available through the interface described here. Board-level tuning on that last C reduced it to only 1 pF. This signal sense technique can be applied right at the input of any ADC interstage filter design with good results. It's necessarily ac-coupled but suitable for the intended network- or spectrum-analyzer measurements.

While the starting point for this RLC filter design is second order,⁷ the design went third order with that added differential C right after those first resistors (*Fig. 8*).

Going left to right in *Figure 8*:

- The FDA differential outputs drive the filter with an output common-mode dc voltage that optimizes the SFDR out of the chosen FDA (1.65 V here, for example)
- Those first small 40.2- Ω resistors isolate the FDA outputs from the reactive loading of the LC elements. They will also introduce a small insertion loss in the filter to the final differential Rload (-2.45 dB here).
- To isolate common-mode voltage setups from the FDA to the ADC, series 1- μ F blocking caps are inserted in the signal path. This is okay for the measurements here, but the interface could also be dc-coupled to the ADC input pins with a bit more effort.
- The differential C, series L's and total final differential C form the third-order filter. This ADC specified a 300 Ω ||9 pF differential input Z where an external tuning Ctune is added to fine-tune the filter flatness in this simulation (it also is used to fine-tune the measured response flatness in the final EVM⁸).



10. Full differential Zt design with 10-MHz postfilter showing $\pm 2\ \mu\text{A}$ at 100-kHz input.

- The filter design called for a final single-ended R of 122 Ω . With half of the ADC's internal 300 Ω forming part of that, the external single-sided R's needed to be 662 Ω . The sense path interface passes through a differential-to-single-ended balun conversion (here using the Mini-Circuits ADT1-1WT) to a final 50- Ω measurement instrument termination. That reflects back to the input side of the balun as 25 Ω on each side in parallel with the physical 26.7 Ω . Those combine to 12.9 Ω to form a total of 12.9 Ω + 649 Ω = 662 Ω as required for the filter design.
- The actual design flow for those two resistors targets a total input resistance, including the reflected 25 Ω from the test instrument, and sets a source impedance (26.7 Ω || 649 Ω) looking back from the balun primary matching that's 25 Ω for each side on the balun inputs (50 Ω total).
- Since blocking caps are in the signal path, the required ADC input Vcm can be brought in at the junction of the two 26.7- Ω resistors (0.95 Vcm here).

The frequency response to the ADC inputs shows about ± 0.3 -dB flatness through 100 MHz (tuning this with the external Ctune), while the sense path at the balun output is a very near replica in shape with considerable attenuation. That measurement path loss is fine for response or harmonic distortion measurements. For lower-frequency spans, use the ADT1-6T.

This approach can be adapted to other design requirements, with the only requirement being a relatively large differential resistor at the ADC inputs broken into this differential-to-single-ended sense path structure. Reference 8 shows measured results using this circuit, revealing that fast Fourier transform (FFT) distortion performance is slightly better than the ADC-only specifications.

Once we have the single-ended version of the ADC input voltage available at the balun output, several harmonic-distortion measurement methods may be applied. Simple spectrum-analyzer measurement will get down to about -90-dBc levels, whereas source cancellation approaches will drop down to better than -110 dBc.⁹

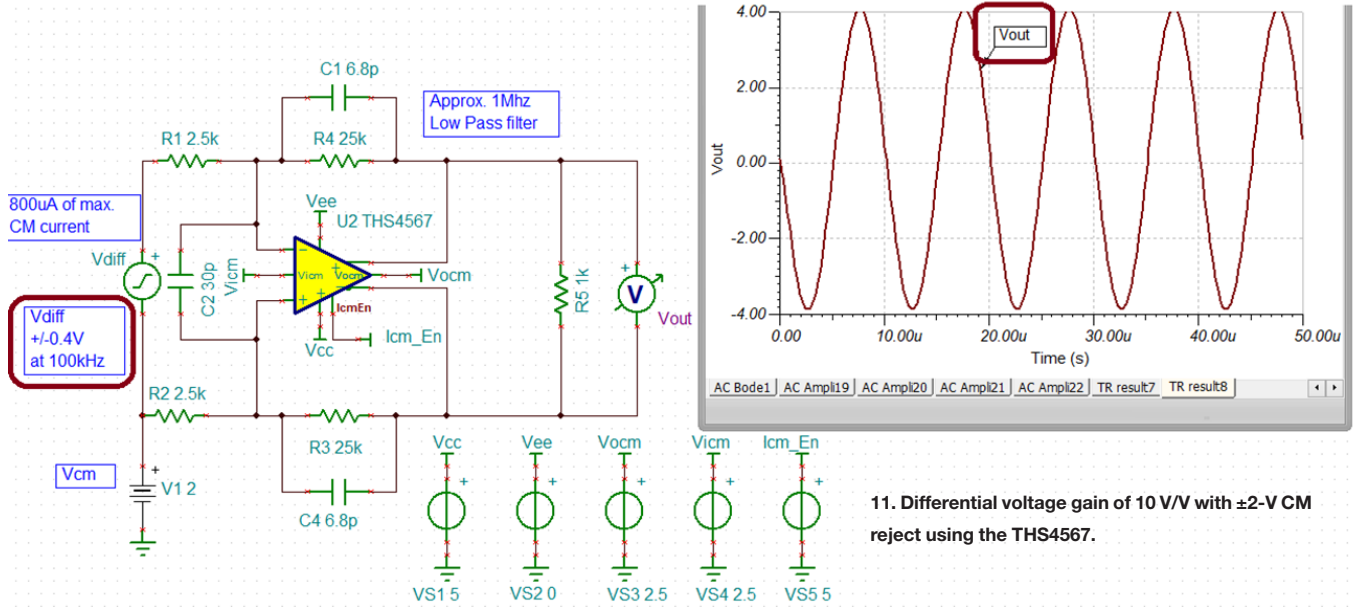
Legacy FDAs struggle with background CM signals on both inputs. A newer solution adds an input CM control loop along with the classic FDA design.

One of the more interesting problems that crops up occasionally is to implement a differential transimpedance stage instead of an FDA when the latter would seem to be applicable. Often, what's made this more problematic is if the two source currents have a large and varying CM current on top of the differential signal.

If that CM current is constant, sometimes we bleed that off at the input summing junctions with fixed resistors to some supply. That, of course, increases the dc noise gain and injects whatever noise is on the reference supply. And it won't work if that CM current varies with time.

The obvious, but previously unavailable, solution is to add an input servo loop that sums equal CM currents into the input nodes to hold an externally set "input" CM voltage. The new (released Dec. 2020) [THS4567](#) starts out with a relatively fast 220-MHz, GBP decompensated core FDA structure and then adds this input servo loop to absorb the source CM current terms.

Since it's intended for differential transimpedance applications from detector diodes, the decompensated FDA is more suited to that application, where the first job in any design is to get the feedback Cf set for the desired frequency response, usually Butterworth. A simple solution for compensating a transimpedance design for the required feedback Cf to achieve



a closed-loop Butterworth is as follows:¹⁰

First, get the approximate noise gain zero dropping out the feedback C_f from this equation for Z_1 , where C_s is the total capacitance on each input pin:

$$Z_1 = \frac{1}{2\pi R_f (C_s + C_f)} \text{ Hz}$$

The characteristic frequency for the second-order closed-loop response will be given by:

$$F_0 = \sqrt{Z_1 GBP}$$

Where we need to be using the true single-pole GBP in this equation.¹⁰

Then, to set the feedback pole location (P_1), use this relationship, where F_c is the intersection of the higher frequency noise gain ($1+C_s/C_f$) with the GBP curve, but use the P_1/F_0 part of this here:

$$Q = \frac{F_o}{F_c} = \frac{P_1}{F_0}$$

Setting P_1 (the feedback pole) to get a $Q = 0.707$ (Butterworth) will then yield an $F_{-3dB} = F_0$.

Stepping through this with a desired $1 \text{ M}\Omega$ on each side gain for the TMS4567 with 10-pF detector diode capacitance will give:

$$Z_1 = 1/(2\pi * 1 \text{ M}\Omega * 11 \text{ pF}) = 14.47 \text{ kHz (where I've added 1 pF for the TMS4567 input C on each side)}$$

$$F_0 = \sqrt{(14.47 \text{ kHz} * 220 \text{ MHz})} = 1.78 \text{ MHz} = F_{-3dB} \text{ (if Q set to 0.707)}$$

$$P_1 = 0.707 * 1.78 \text{ MHz} = 1.26 \text{ MHz}, C_f = 0.12 \text{ pF}$$

The response certainly looks Butterworth, with almost exactly the expected $1.8 \text{ MHz } F_{-3dB}$ for this $2 \text{ M}\Omega$ ($126 \text{ dB}\Omega$) design (Fig. 9).

Resetting the feedback C_f to a typical thick-film resistor 0.18-pF parasitic, and adding a 10-MHz post RC filter, shows the $\pm 4\text{-V}$ differential output of Figure 10 for a $\pm 2\text{-}\mu\text{A}$, 100-kHz sine-wave input sitting on top of $50\text{-}\mu\text{A}$ CM input current. Without the input cancelling currents, that $50\text{-}\mu\text{A}$ CM current would be taking the outputs to negative 50 V .

Here, I had set the target input CM voltage to 1.0 V with the output V_{ocm} midsupply at 2.5 V . Each output is swinging $\pm 2 \text{ V}$ around that to give the $\pm 4\text{-V}$ differential output for the $\pm 2 \mu\text{A}$ shown in Figure 10.

This device might also be used to gain up a small differential voltage signal on top of a larger CM source voltage that varies with time. In this case, the maximum input I_{cm} current for the CM voltage range must be less than the maximum

available internal I_{cm} cancelling current. The specification doesn't appear in the datasheet, but up to 1 mA is supported in the simulation model.

Backing that maximum off to a safe $\pm 800 \mu A$ maximum, use that to design a gain of 10 stage with ± 2 -V input CM range. That will then require a $2\text{-V}/0.8\text{-mA} = 2.5\text{-k}\Omega$ input resistor with a $25\text{-k}\Omega$ feedback R_f .

These higher R 's will require some compensation. Here, I've added a feedback C_f to give a 1-MHz pole, then added a differential input C that will shape the noise gain to 10 V/V at higher frequency (*Fig. 11*).¹² The input I_{cm} servo loop cancels the input $800 \mu A$ of CM current to hold the input pins at 1 V. Those two I_{cm} currents do have some offset introducing an output offset voltage in this simulation.

This brief survey of some of the newer results coming out of the various amplifier development groups just touch on the vast range of newer (and hopefully better) analysis approaches and devices that have emerged over the last 10 years. Many more exist, but they require a close reading of the vendor material to expand your horizons. Someday, most of these might appear in an updated textbook.

References

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2. [TI Training Seminar – Selecting the Right High-Speed Amplifier to Drive High Speed ADC's](#)
3. [Legacy literature showing a combined THD as a power addition](#)
4. [Analog Devices Diff Amp Calculator](#)
5. [Wideband matched input single to differential active balun using an FDA](#)
6. [Active balun EVM using the ISL55210 videos](#)
7. [Low insertion loss RLC filter for ADC driving](#)
8. [14bit, 500MSPS ADC with FDA and filter EVM](#)
9. [Source cancellation harmonic distortion measurement](#)
10. [Transimpedance Design for High Speed Amplifier Application Note](#)
11. [Why is Gain Bandwidth Product so confusing?](#)
12. [Unique compensation technique tames high bandwidth voltage feedback op amps](#)