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# Essential Timing Factors for Low-Power Precision Signal-Chain Apps (Part 2)

Part 1 of this series discussed timing considerations for sigma-delta ADCs. Part 2 gets into the timing factors and solutions for reducing power while maintaining precision in low-power systems when using a SAR ADC.

The three blocks in *Figure 1* can be viewed independently, starting with the analog front end (AFE) for a successive-approximation-register (SAR) ADC. The type of signal chain will change the AFE, but some common aspects will apply to most circuits.

Figure 2 shows the AD4696 SAR ADC, the external amplifier, and a low-pass filter that make up the AFE. The AD4696 is a 16-bit, 1-Msample/s multiplexed SAR ADC with Easy Drive features. While external amplifiers and circuitry are required to interface with external sensors, Easy Drive features such as analog-input high-Z mode and reference-input high-Z mode reduce the analog input and reference drive requirements.

In higher-power applications, the SAR ADC's antialiasing filter design needs to be aggressive, but for sampling lower-bandwidth signals that are typical of low-power applications, the filter design is less demanding. The benefit to a sigma-delta architecture is that we can rely on the digital filter to determine frequency response and use the external anti-aliasing filter to filter at the modulator frequency.

In the absence of oversampling and the inherent filtering qualities, an external analog low-pass filter is required to prevent any higher-frequency signals present above the sample rate aliasing into the passband. The low-pass filter also acts to reduce wideband noise from the analog front-end circuitry, reduce the nonlinear voltage kickbacks that occur at the analog inputs, and protect the analog inputs from overvoltage events. The same principle applies to the
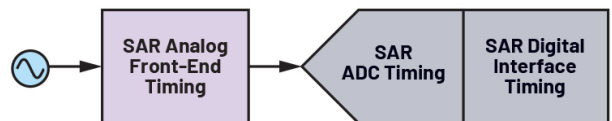

1. AFE timing considerations with a multiplexed SAR ADC.

timing considerations. For more, see the antialiasing filter section in Part 1.

The SAR ADCs, while sampling, incorporate a sample-and-hold mechanism, which is a switch and a capacitor that captures the input signal until a conversion is gathered.

The design of the amplifier stage is a two-step process. The first step is to select the signal-conditioning amplifier and external antialiasing stage similar to what's discussed in Part 1. The next step is to choose an external driver amplifier (which has a bandwidth dictated by the gain; remember there's a power vs. bandwidth tradeoff) that will buffer
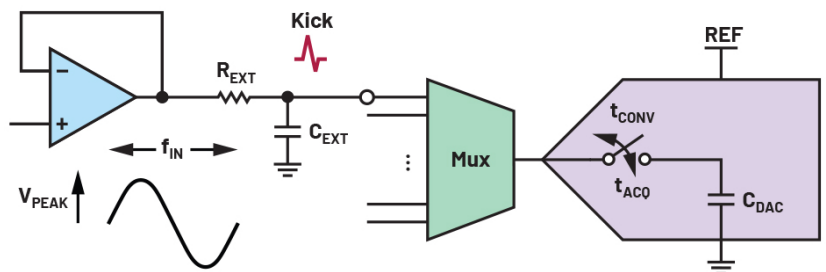
2. Shown is the AD4696 SAR ADC with an external kickback RC filter and a driver amplifier.

the signal-conditioning antialiasing filters output and drive the ADC input. The next step is to design the kickback filter, taking the total capacitance $C_{EXT} + C_{DAC}$ as the total capacitance of our filter.

Dealing with Kickback

Multiplexed SAR ADCs suffer from kickback when switching between analog input channels. Each time the switch is closed, the internal capacitor voltage (C_{DAC}) may be different from the voltage previously stored on the sampling capacitor (C_{EXT}). A voltage glitch occurs when these switches close due to the difference. The energy will be shared between them, and the voltage measured between the capacitor terminals will be halved.
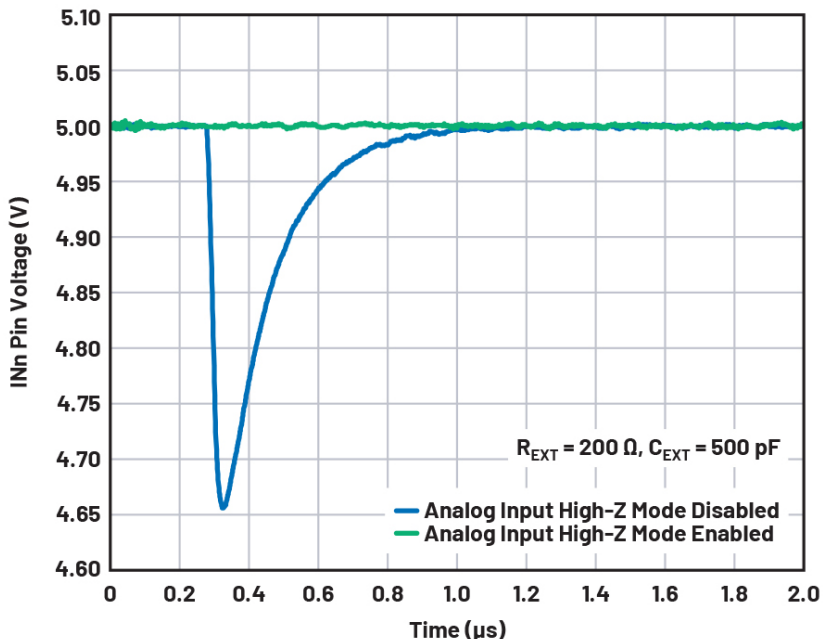
The C_{EXT} and C_{DAC} values will impact filter designs and need to be considered when designing a circuit. The kickback and the choice of the ADC driver are described in detail in the AD4696 datasheet. ADC driver tools in conjunction with training videos also are available.

The AD4696 contains an analog-input high-Z mode. This significantly reduces the magnitude of the voltage kickback as seen in *Figure 3*. The analog-input high-Z mode also reduces performance degradation caused by series resistance between the front-end amplifiers and the AD4696 analog inputs. This allows the resistor in the external RC filter to be larger compared to traditional multiplexed SAR ADCs.
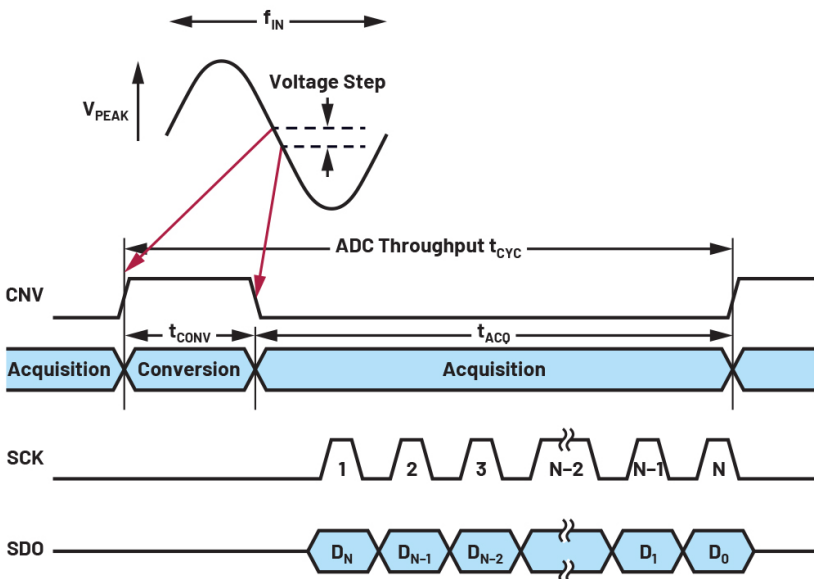
Using larger R_{EXT} with smaller C_{EXT} alleviates amplifier stability concerns without significantly impacting distortion performance. However, $C_{EXT} = 500$ pF minimum is recommended if an internal overvoltage-protection clamp is enabled to avoid stability issues. *Figure 3* shows us that we can sample the required signal quicker, speeding up our system timing.

ADC Timing Considerations

The ADC that's chosen will depend on what's important in your system. Numerous articles address what's a better fit in terms of performance and compare SAR and sigma-delta technology. In the low-power space, there's plenty of

3. The high-Z mode's impact on kickback.

$R_{EXT} = 200\ \Omega$, $C_{EXT} = 500$ pF

— Analog Input High-Z Mode Disabled
— Analog Input High-Z Mode Enabled

4. The AFE SAR timing considerations.

5. Typical SAR ADC timing.

overlap between SAR and sigma-delta ADCs measuring similar signals. One thing is clear, though: SAR timing is more straightforward to understand *(Fig. 4)*.

SAR ADCs, which sample the input at a point in time, consist of an acquisition phase and a conversion phase *(Fig. 5)*. In the acquisition phase, the sample-and-hold network or the internal capacitive network is being charged. In the conversion phase, the capacitor array is switched to a com-

parator network and a weighting on the DAC is modified until a code corresponding to the analog input is reached.

The maximum conversion time is specified in the datasheet—415 ns for the AD4696. The minimum conversion time to acquire the signal is 1715 ns, which is the acquisition time for the AD4696 while operating at 500 ksamples/s. The time between conversions is the throughput rate.

In terms of timing, the main tradeoff in relation to the SAR ADCs is the power consumption vs. the ADC sample rate. SAR ADCs have the advantage of maintaining a direct linear relationship between the sample rate and supply current, which means that it can scale depending on the bandwidth of the signal of interest. The internal ADC core powers down between conversions. Therefore, when operating at lower sample rates, e.g., 10 ksamples/s the AD4696 typically consumes 0.17 mW vs. 8 mW at 1 Msamples/s, making the devices suitable for battery-powered applications at lower sample rates.

6. V_{DD} current vs. sample rate.

Figure 6 shows the V_{DD} current. If we reduce the sample rate of the AD4696 to work in the sub-100-ksample/s range vs. at 500 ksamples/s, our I_{DD} current drops from almost 2.5 mA to 0.5 mA. If we reduce the current further to 10 ksamples/s, our typical I_{DD} current reduces to 42 µA. The rate of increase in current is linear. All digital and analog supply currents scale in a similar linear fashion, making the SAR ADC an attractive proposition for measurement of dc-ac signals using the same part.

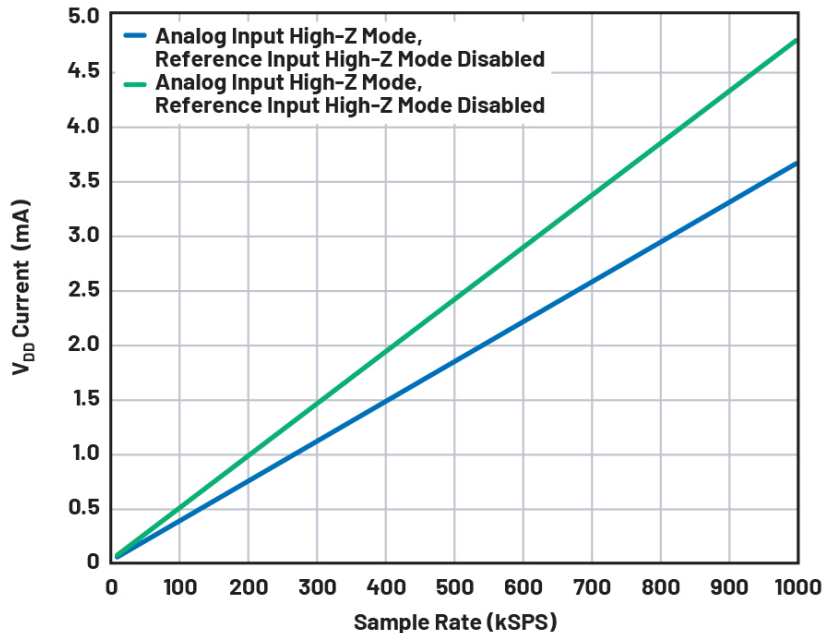**Digital Interface Timing Considerations**

Several features associated with the AD4696 would not be traditionally associated with SAR ADCs—features that could help low-power signal-chain designers achieve additional power savings but with timing implications *(Fig. 7)*.

A SAR ADC's throughput rate in comparison to the sigma-delta architecture is easier to calculate because filter latency needn't be considered:

$$Throughput\ Rate\ (SPS) = \frac{1}{t_{CYC}} \div CHs \qquad (1)$$

where CHs = the number of channels enabled.

The cycle time is the time between CNV rising edge transitions and consists of a combination of the acquisition and conversion phases, but there may be overlap. The ADC can begin acquiring a signal while the conversion phase is still taking place. The time between samples on a SAR ADC can be described as cycle time (t_{CYC}) or sample-rate time (t_{SR}).
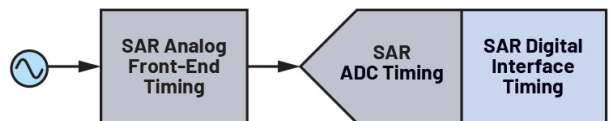

7. SAR digital interface timing considerations.

$t_{CONVERT}$ = conversion time t_{ACQ} = acquisition time
$t_{CYC} = t_{SR}$ = inverse of the sample frequency, the time between samples

The sample instant of when the conversion occurs is controlled by the CNV signal rising edge. In most modes, it's provided by an external signal. The AD4696 also has an on-chip autocycle mode that can generate the convert start signal internally. This signal kick starts the conversion. A number of sequencer modes are available on the AD4696, allowing the user to choose the order and configuration of conversions in a predefined fashion or control the next channel in the sequence on-the-fly without interrupting conversions.

The digital host must read back the data before the start of the next conversion. With higher-speed signals, the SCK frequency must therefore be fast enough to read back the data from the AD4696 SPI before the next CNV rising edge (or internal convert start signal when in autocycle mode). Faster sample rates require faster SCK frequencies due to the shorter time between conversions.

The minimum required SCK frequency is a function of the sample rate, the length of the SPI frame (in bits), and the serial data output mode in use. Conversion results for a given sample are available until the start of the next conversion phase. The SCK frequency must therefore be fast enough
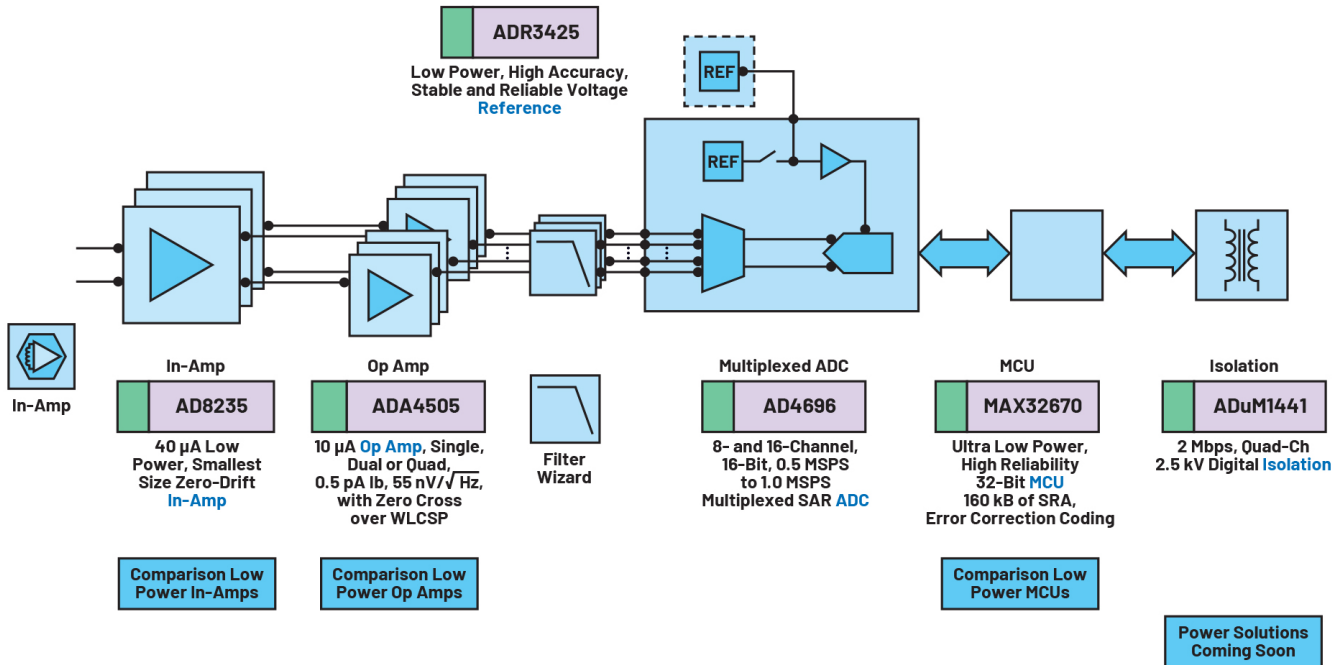
8. This is an example of a signal chain.

to read the data from the AD4696 SPI before the following CNV rising edge (or internal convert start signal when autocycle mode is enabled).

Multiple SDO Digital Outputs

The AD4696 family also includes dual-SDO and quad-SDO modes. In these modes, ADC results are shifted out on SDO and additional GPIO pins in parallel. These modes significantly lower the required SCK frequency for a given sample rate by doubling or quadrupling the number of bits output on the SPI per SCK period. This reduces the requirement on the microcontroller, which lowers the required clock from a 32-MHz SPI clock to a 16-MHz SPI clock when converting at 1 Msample/s.

The number of SCK periods required per conversion-mode frame (N_{SCK}) is a function of the number of bits per frame (N_{BITS}) and the number of serial data outputs (N_{SDO}):

$$N_{SCK} = \frac{N_{BITS}}{N_{SDO}} \qquad (2)$$

where N_{SDO} is 1 for single-SDO mode, 2 for dual-SDO mode, and 4 for quad-SDO mode.

The start of the conversion-mode SPI frame must not occur before the $t_{CONVERT}$ time has elapsed and must complete early enough to adhere to the minimum t_{SCKCNV} specification. The amount of time given to complete an SPI frame in conversion mode (t_{FRAME}) is calculated as follows:

$$t_{FRAME} = t_{CYC} - t_{CONVERT\_max} - t_{SCKCNV}$$

where t_{CYC} is the sample period, $t_{CONVERT\_max}$ is the maximum, $t_{CONVERT}$ is the specification, and t_{SCKCNV} is the SCK to CNV rising edge delay specification.

The f_{SCK} is a function of t_{FRAME} and N_{SCK}:

$$f_{SCK} > \frac{N_{SCK}}{t_{FRAME}} \qquad (3)$$

The AD4696 datasheet includes a table that gives examples of minimum SCLK frequencies vs. several sample rates.

Autocycle Mode

Traditionally, for voltage- or current-level monitoring applications, SAR ADCs require a host controller to issue a convert signal continually for conversions to take place. The system needs to examine the data for thresholds and make decisions based on these levels. This isn't power-efficient because it means the host needs to continually convert. The AD4696 can be configured to convert autonomously on a user-programmed channel sequence.

Autocycle mode is a great mode to use for monitoring analog inputs. There are several options for the conversion period, ranging from 10 μs (100-ksample/s rate) to 800 μs (1.25-ksample/s rate). This mode can be used with threshold and hysteresis detection alerts, which are configurable on a per channel basis to reduce overhead for the digital host system. In this scenario, the host controller can enter a low power state and only power up when it receives an interrupt from the AD4696 when a level is triggered.

Oversampling

Oversampling and decimation are inherent to sigma-delta architecture as seen in Part 1 of the series. The AD4696 SAR ADC includes an oversampling and decimation engine to allow for further noise reduction. It effectively averages consecutive ADC samples to generate an oversampled result with higher effective resolution and lower noise. The effective number of bits increases by 1 bit every time the oversampling ratio (OSR) is increased by a factor of 4 on the AD4696.

This is especially useful in measuring a slower-moving signal found in a low-power signal-chain application, such as temperature, which requires higher precision:

$$t_{SAMPLE} = t_{CYC} \times OSR \qquad (4)$$

where t_{SAMPLE} = the sample period, t_{CYC} = cycle time (1/sample rate), and OSR = oversampling ratio (a programmable value of between 4 and 64).

The tradeoff, similar to sigma-delta ADCs, is between performance and speed. See the *table* for a summary of the

SAR Summary

Topic	Timing considerations	Low-power signal-chain impact
Antialiasing filter	Delays can exist that impact the first conversion result(s)	Less aggressive filtering needed compared to higher-speed signal chains
High-Z mode	The kickback time is reduced when switching channels	Power scales with sample rate; less external circuitry
Current vs. sample rate	Reducing power reduces your sample rate	Reducing your sample rate reduces power
Autocycle mode	Software-configurable internal convert start	Host controller can enter a low-power state
Dual-SDO and Quad-SDO	At higher sample rates, read back of all data not possible with single SDO	Tradeoff between extra circuitry and data speeds
Oversampling	The interval between samples increases as the oversampling increases	Increasing OSR improves noise and resolution performance

SAR architecture.

Low-Power SAR Signal-Chain Example

Many applications require the measurement of a small signal on top of a large dc offset or common-mode voltage. If the aim of a system is to monitor flow in an industrial environment or make a biopotential measurement, there's overlap in the approach. These signals typically need ac coupling to remove the large offset as well as biasing and gain to maximize the dynamic range of the ADC.

Analog Devices has developed low-power precision signal chains that include suggestions on which devices to choose for this type of application *(Fig. 8)*. In addition, know-how with integrated knowledge (KWIK) circuits provide a more in-depth analysis of circuits as well as the latest suggestions on up-to-date components to choose.

Flow Signal-Chain Example

Take an example where we want to design a large multi-measurement system that includes flow measurement using the KWIK circuit shown in *Figure 9*.

Question: I want to run 10 flow sensors at 1 ksample/s. Is the SAR or sigma-delta the better option?

Answer: The SAR (AD4696) in conjunction with the AD8235 and ADA4505-2 amplifiers needed for signal conditioning are the best options. We can run 10 channels at 10 ksamples/s using an external convert signal or autocycle mode.

Question: What are the AFE timing considerations?

Answer: In this case, the response vs. gain of the AD4505-2 amplifier will dictate the BW of the signal under measurement rather than the antialiasing filter response. The high-Z mode will take the pressure off the performance of the input amplifier, enabling designers to choose lower power amplifiers. The components in *Figure 9* are chosen for their ultra-low-power performance.

Conclusion

When designing high-resolution, low-power data-acquisition systems, it can be difficult to find the lowest-power components available. On that front, ADI's precision low-power signal chains can act as a starting point for low-power designs. Care must be taken in understanding the tradeoffs and differences in timing when forming signal chains that incorporate sigma-delta and SAR architectures as their core ADC.

When interfacing with sensors or signals of interest, the analog front-end timing needs to account for
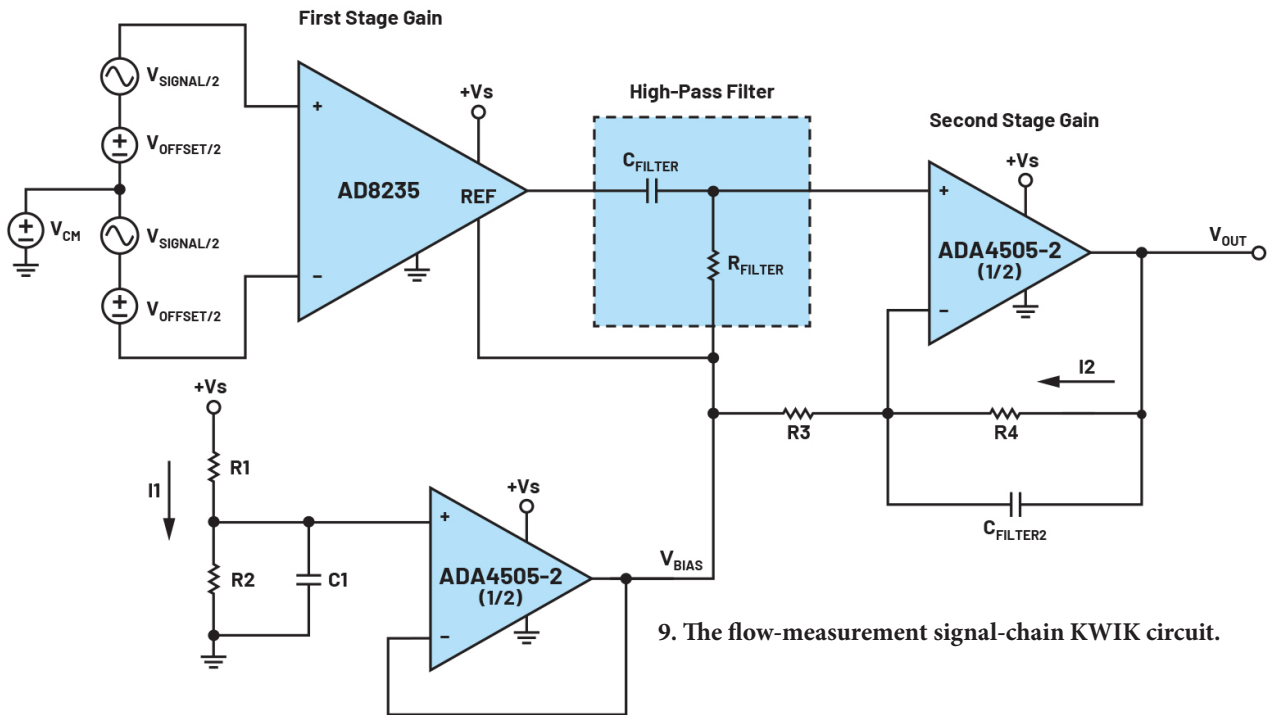
9. The flow-measurement signal-chain KWIK circuit.

chip-level startup, sensor biasing, external filtering, and component choice. Antialiasing filters are needed with stricter requirements on SAR ADCs because sigma-delta ADCs have inherent sampling associated with their design. On the AFE, sigma-delta ADCs incorporate PGAs while SAR technology like high-Z mode eases the drive requirements on external amplifier circuitry.

When we consider sigma-delta ADC architecture, oversampling and decimation as well as filter latency have an impact on the throughput rate, especially while converting on more than one channel. SAR throughput, on the other hand, is more straightforward to calculate because of the successive-approximation approach, with the added benefit that the slower you sample, the lower the current drawn while converting.

The complexity of the sigma-delta AD4130-8 digital timing has led to the development of ACE software timing tools. These help to simplify the understanding and aid in calculating the channel throughput rate. The same device has timing features like duty cycling, FIFO, and a standby mode to help conserve battery life, but care must be taken when looking at the achievable effective resolution when targeting a particular throughput rate.

When we examine a SAR ADC like the AD4696, we can sample at higher sample frequencies. This has its advantages, but it means the digital timeframe (t_{FRAME}), which you need to read back, is smaller. Thus, faster SPI clock speeds are needed.

Padraic O'Reilly is an electronic test and measurement applications engineer focused on low-power precision converter signal chains. Padraic enjoys architecting signal chains that combine technologies from multiple product lines. In the past, Padraic has held various measurement and applications roles. He has expertise in both RF microwave (PLLs, radar, radio transceivers) and precision mixed-signal converter systems (DACs, ADCs, ASICs). Padraic holds a bachelor's degree in electronic engineering from the University of Limerick.

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