Electronic Design

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How to Leverage the Inverting Buck-Boost in High-Voltage Apps

When the need arises for the generation of a negative voltage rail, the inverting buck-boost topology offers the best compromise between high efficiency and small form factor. But one must become familiar with the topology under high-voltage conditions.

A variety of topologies can be considered for applications that require the generation of a negative voltage rail, as illustrated in the article "The Art of Generating Negative Voltages."[1] However, if the absolute voltage at the input and/or output can exceed 24 V and the required output current may reach a few amperes, the charge pump and the negative LDO regulator are to be discarded due to their low current capability. Also, the size of their magnetic components causes the flyback and the Ćuk converter solutions to become quite cumbersome. As a result, under such conditions, the inverting buck-boost provides the best compromise between high efficiency and small form factor.

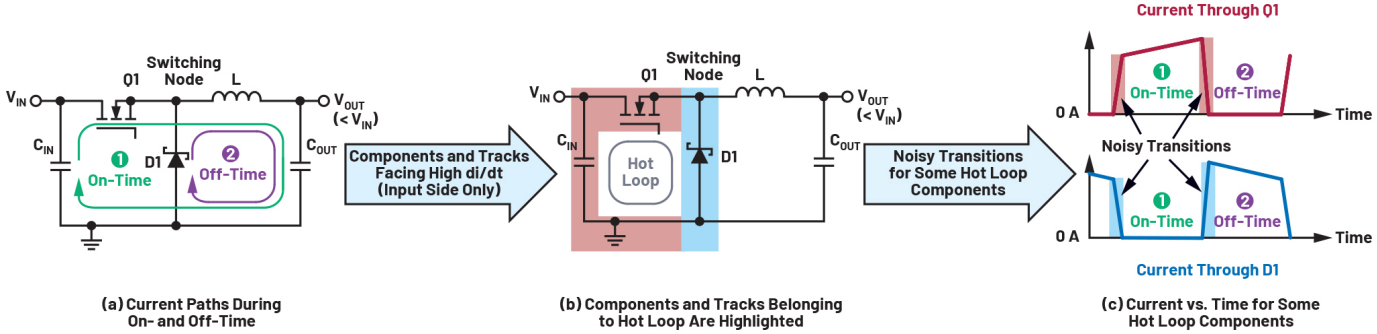
To reap these benefits, though, the operation of the inverting buck-boost topology under high-voltage conditions must be fully understood. Before diving into such details, we will begin with a brief review of the inverting buck-boost topology. Then, we will compare the critical current paths of the inverting buck-boost, buck, and boost topologies.

The Three Basic Non-Isolated Topologies

The inverting buck-boost belongs to the grouping of three basic non-isolated switching topologies. These topologies all consist of a control transistor (usually a MOSFET), a diode (either a Schottky diode or an active diode—the synchronous MOSFET), and a power inductor as the energy-storage element. The common connection between those three elements is referred to as the switching node. The positioning of the power inductor with regard to the switching node determines the topology.

If the coil is located between the switching node and the output, we obtain the dc-dc buck converter, which we simply call buck in the rest of this article. Alternatively, positioning the coil between the input and switching node creates the dc-dc boost converter, referred to as boost here. Finally, the dc-dc inverting buck-boost consists of placing the coil between the switching node and ground (GND).

During each switching period and even in continuous conduction mode (CCM), all three topologies include com-



1. Components and tracks belonging to the hot loop—buck converter operating in CCM.

ponents and PCB traces that are facing fast changes in current, leading to the noisy transitions highlighted in *Figures 1c, 2c, and 3c*. By keeping the hot-loop small, the electromagnetic interference (EMI) radiated by the circuit can be reduced.

At this stage, it's worth mentioning that the hot loop isn't necessarily a physical loop through which the current circulates. Indeed, for the respective loops highlighted in *Figures 1-3*, the sharp current transitions don't occur in the same direction for the components and tracks highlighted in red and blue that form the hot loop.

For the inverting buck-boost operating in CCM *(Fig. 3)*, the hot loop consists of C_{INC}, Q1, and D1. Compared with the hot loop of the buck and boost topologies, the hot loop of the inverting buck-boost contains components located both on the input and output sides. Among these components, the reverse recovery of the diode (or body diode if using a synchronous MOSFET) when the control MOSFET turns on generates the highest di/dt and EMI.

Since a thorough layout concept is needed to contain the radiated EMI from these two sides, the last thing you want is to create additional radiated EMI through excessive coil current ripple by underestimating the required inductance of the inverting buck-boost under high input and/or output voltage conditions. This risk exists for engineers who rely on their familiarity with the boost topology to size the inductance of their inverting buck-boost circuit, as we now see by comparing both topologies.

Design Considerations of Inverting Buck-Boost with High Voltages

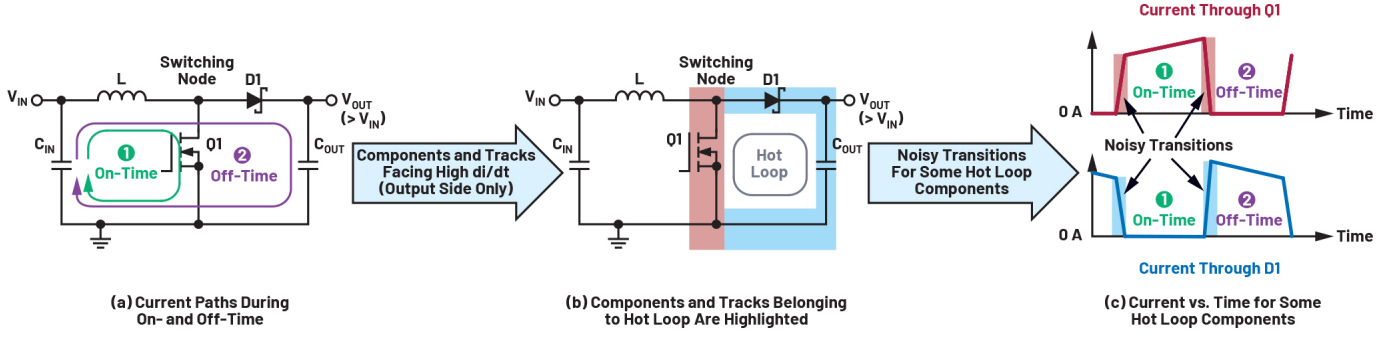
Both the boost and the inverting buck-boost can generate an absolute output voltage whose amplitude is higher than the input voltage. There are, however, relevant differences between both topologies that can be highlighted with the help of their respective duty cycles in CCM, provided in Equation 1 and Equation 2. Please note that these are first-order approximations that do not consider effects such as the voltage drops through Schottky diodes and power MOSFETs.

$$D_{INVERTING\ BUCK\text{-}BOOST} = \frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|} \quad (1)$$

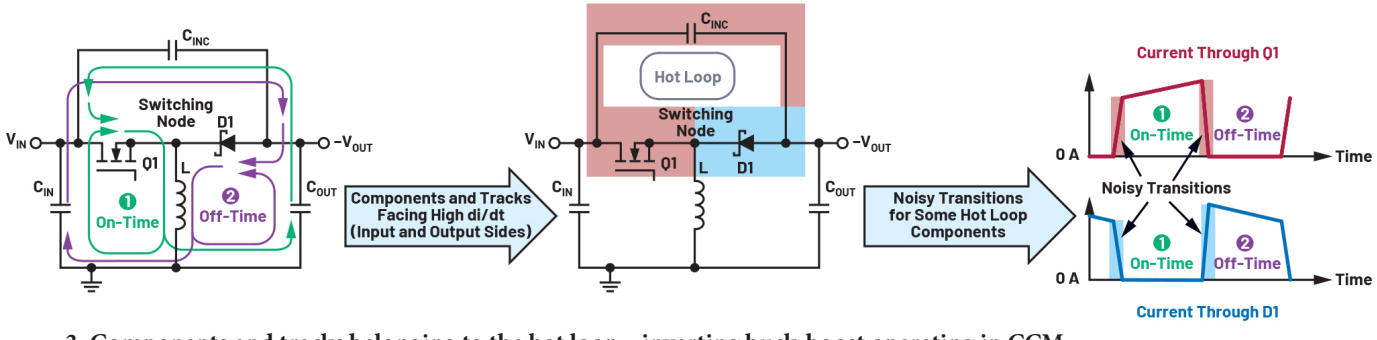
$$D_{BOOST} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

The first-order approximation for the variation of these duty cycles vs. $|V_{OUT}|$, and with V_{IN} = 12 V, is plotted on the left side of *Figure 4*. Moreover, assuming in both cases a switching frequency (f_{SW}) of 1 MHz and an inductance of 1 µH for the power coil, the variation of the coil current ripple vs. V_{OUT} was obtained on the right side of *Figure 4*.

We observe in *Figure 4* that the duty cycle of an inverting buck-boost will exceed 50% from a much lower $|V_{OUT}|$ than the boost: 12 V and 24 V, respectively. It can be understood



2. Components and tracks belonging to the hot loop—boost converter operating in CCM.



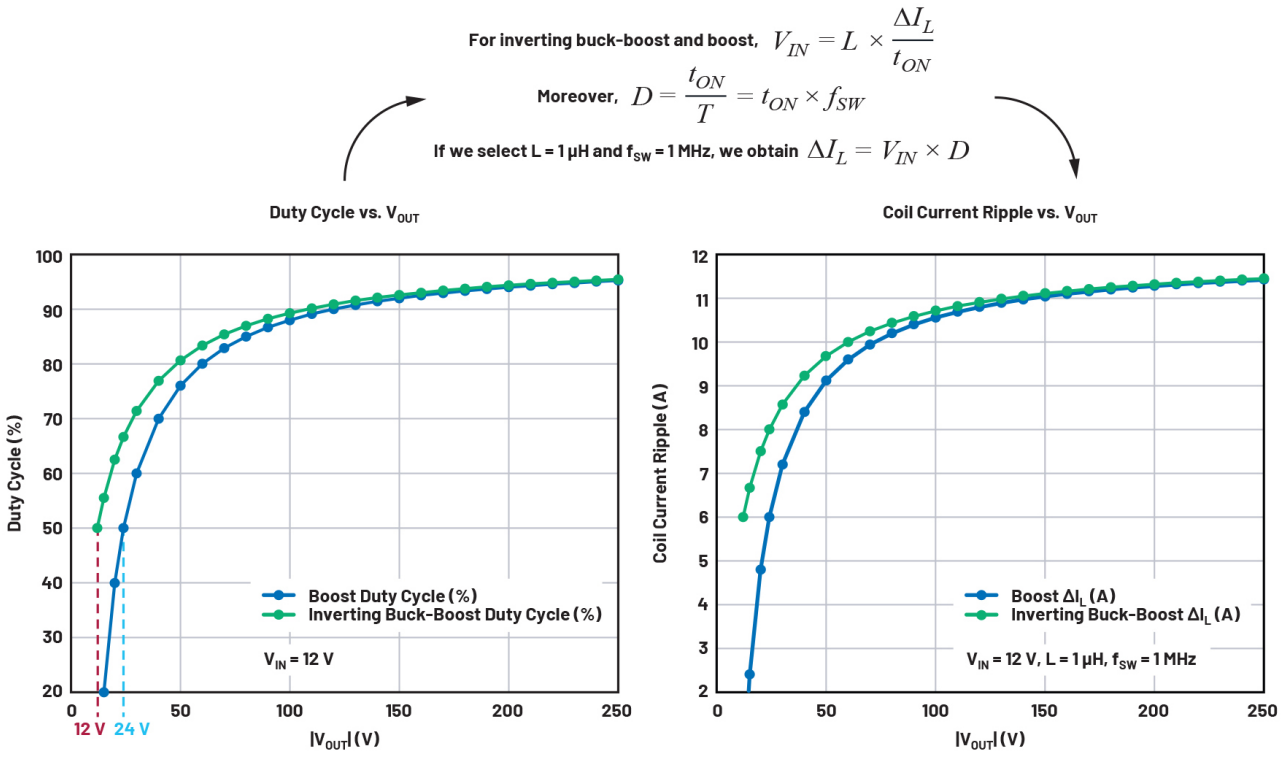
3. Components and tracks belonging to the hot loop—inverting buck-boost operating in CCM.

by referring to *Figure 5*.

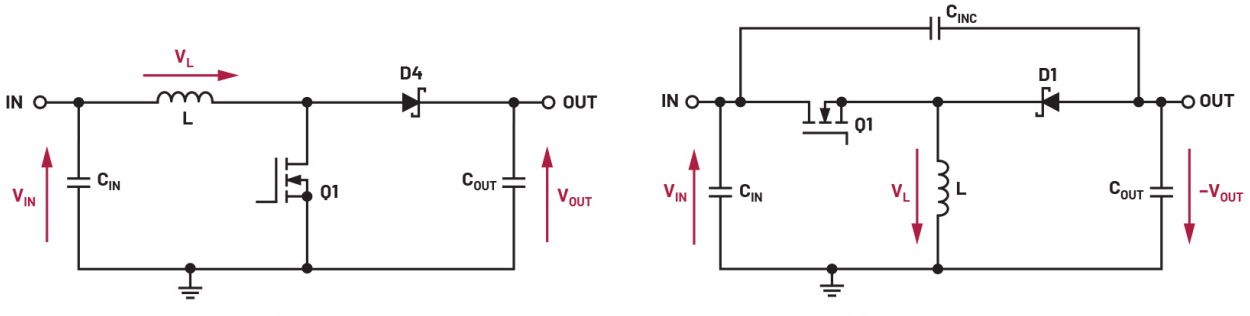
In the case of the boost, the inductor is in the path between input and output. Therefore, the voltage through the power inductor (V_L) adds up to V_{IN} to provide the required V_{OUT}. However, for the inverting buck-boost, V_L is the sole contributor to the achieved output voltage. On that occasion, the power inductor must provide much more energy to the output, which explains why the duty cycle already reaches 50% for a much lower $|V_{OUT}|$.

We can reformulate this observation by stating that, as the ratio $|V_{OUT}|/V_{IN}$ decreases, the duty cycle drops at a much slower rate for the inverting buck-boost than for the boost. This is an important fact to consider during design, and its impact can be better understood by referring to *Figure 6*, where the first-order approximation of the duty cycle and coil current ripple are redrawn, but this time vs. V_{IN}.

As demonstrated in *Figure 6*, the coil current ripple (ΔI_L) is proportional to V_{IN} and D. In the case of the boost,



4. Duty cycle and coil current ripple vs. $|V_{OUT}|$ at V_{IN} = 12 V for inverting buck-boost and boost.



(a) Boost

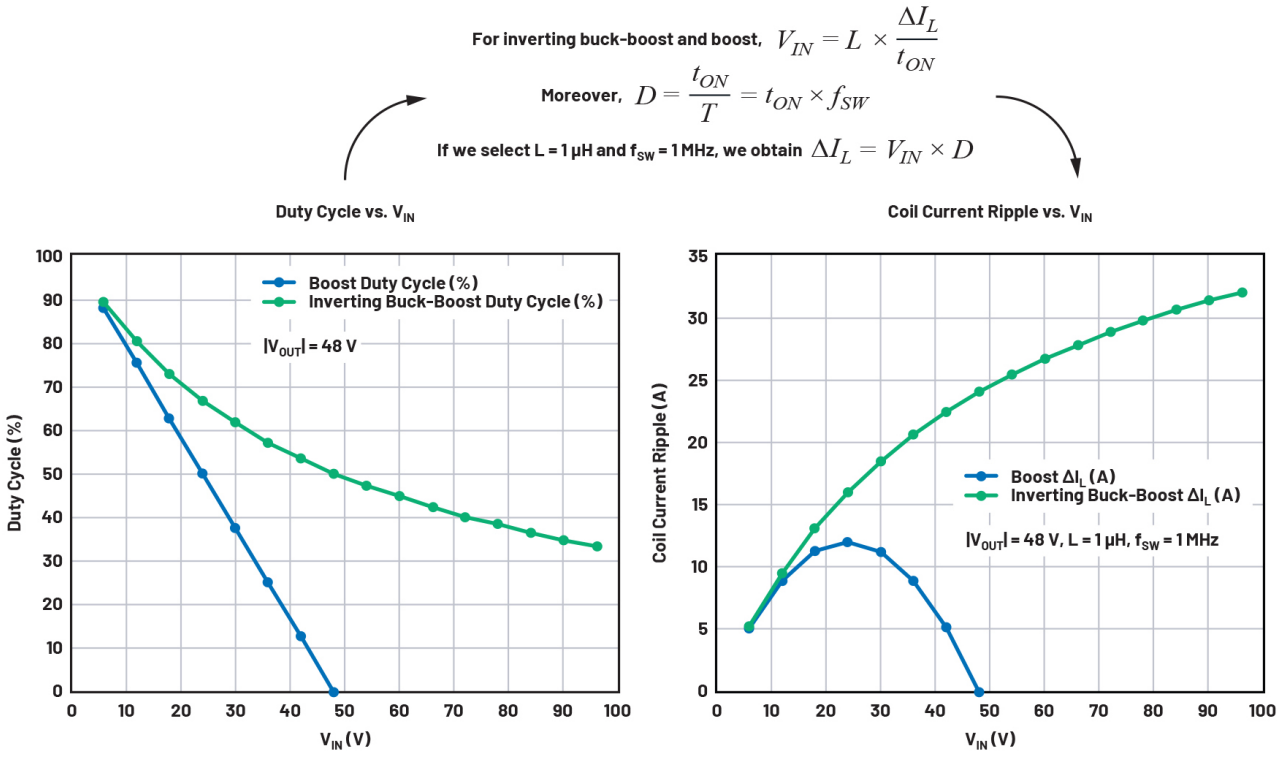
For the boost, V_L adds up to V_{IN} so that V_{OUT} can be higher than V_{IN}

(b) Inverting Buck-Boost

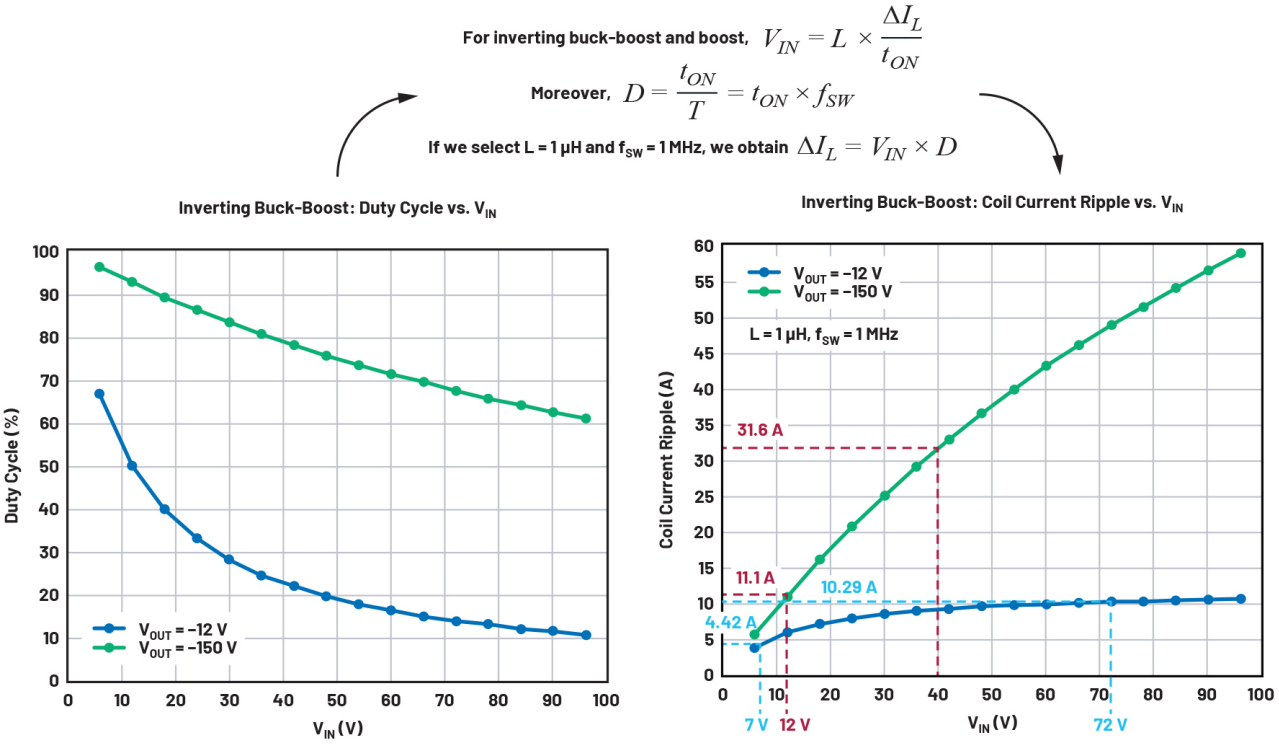
For the inverting buck-boost, V_L provides the full voltage amplitude seen at the output

Note that the output is in parallel with $-V_L$

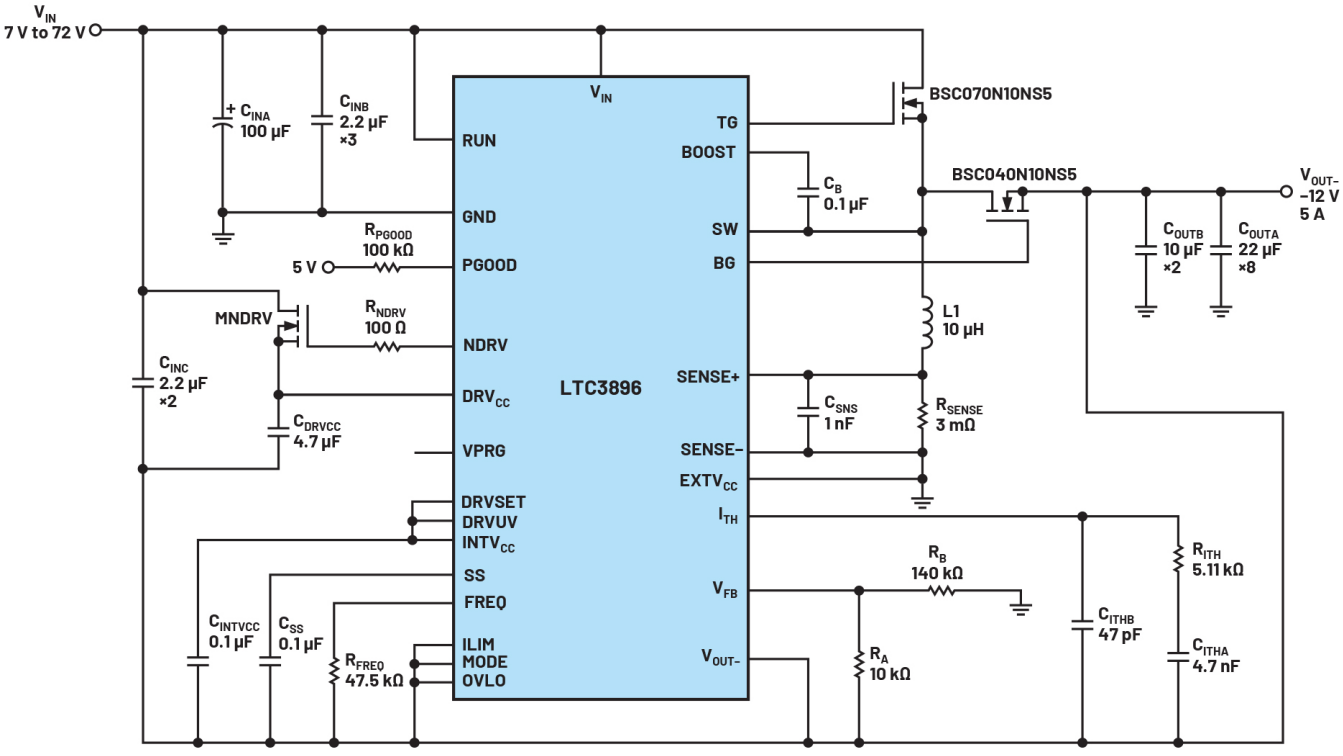
5. Impact of the coil positioning on the obtained output voltage.



6. Duty cycle and coil current ripple vs. V_{IN} at $|V_{OUT}|$ = 48 V for inverting buck-boost and boost.



7. Duty cycle and coil current ripple vs. V_{IN} at V_{OUT} = –12 V and –150 V for inverting buck-boost.



8. LTC3896 circuit with V_{IN} = 7 to 72 V, V_{OUT}- = –12 V, and f_{SW} = 300 kHz.

as V_{IN} becomes higher than half of V_{OUT}, the duty cycle decreases faster than V_{IN} increases, going from 50% at V_{IN} = 24 V to a quarter of this value at V_{IN} = 42 V for the blue curve in the left graph of *Figure 6*. Consequently, ΔI_L decreases quickly for V_{IN} above 24 V for the boost on the right graph of *Figure 6*.

But, for the inverting buck-boost, we previously saw in *Figure 4* that D decreases very slowly when $|V_{OUT}|/V_{IN}$ decreases. In other words, when V_{IN} increases for a fixed $|V_{OUT}|$. This can be seen for the green curve on the left graph of *Figure 6*, where the duty cycle loses only 25% when V_{IN} increases by 62.5% from 48 to 78 V. Since the decrease in D doesn't compensate for the increase in V_{IN}, the coil current ripple increases significantly with V_{IN}, as illustrated by the green curve in the right graph of *Figure 6*.

Overall, the higher coil current ripple potentially faced under high-voltage conditions by the inverting buck-boost compared with the boost explains why the former topology requires higher coil values if operating at the same f_{SW}. Let's use this knowledge in a concrete case with the help of *Figure 7*, which also is based on first-order approximations.

Application with Wide Input Voltage Range and High Output Current

Let's consider an application with V_{IN} = 7 to 72 V and V_{OUT} = –12 V at 5 A. Given the high output current, we opt for a synchronous controller (LTC3896) to achieve high efficiency.

Selecting the Inductance

When operating the LTC3896 in CCM, it's recommended to keep ΔI_L between 30% and 70% of $I_{OUT,MAX}$, which is 5 A for our example. Consequently, we want to design for ΔI_L between 1.5 and 3.5 A over our whole input voltage range.

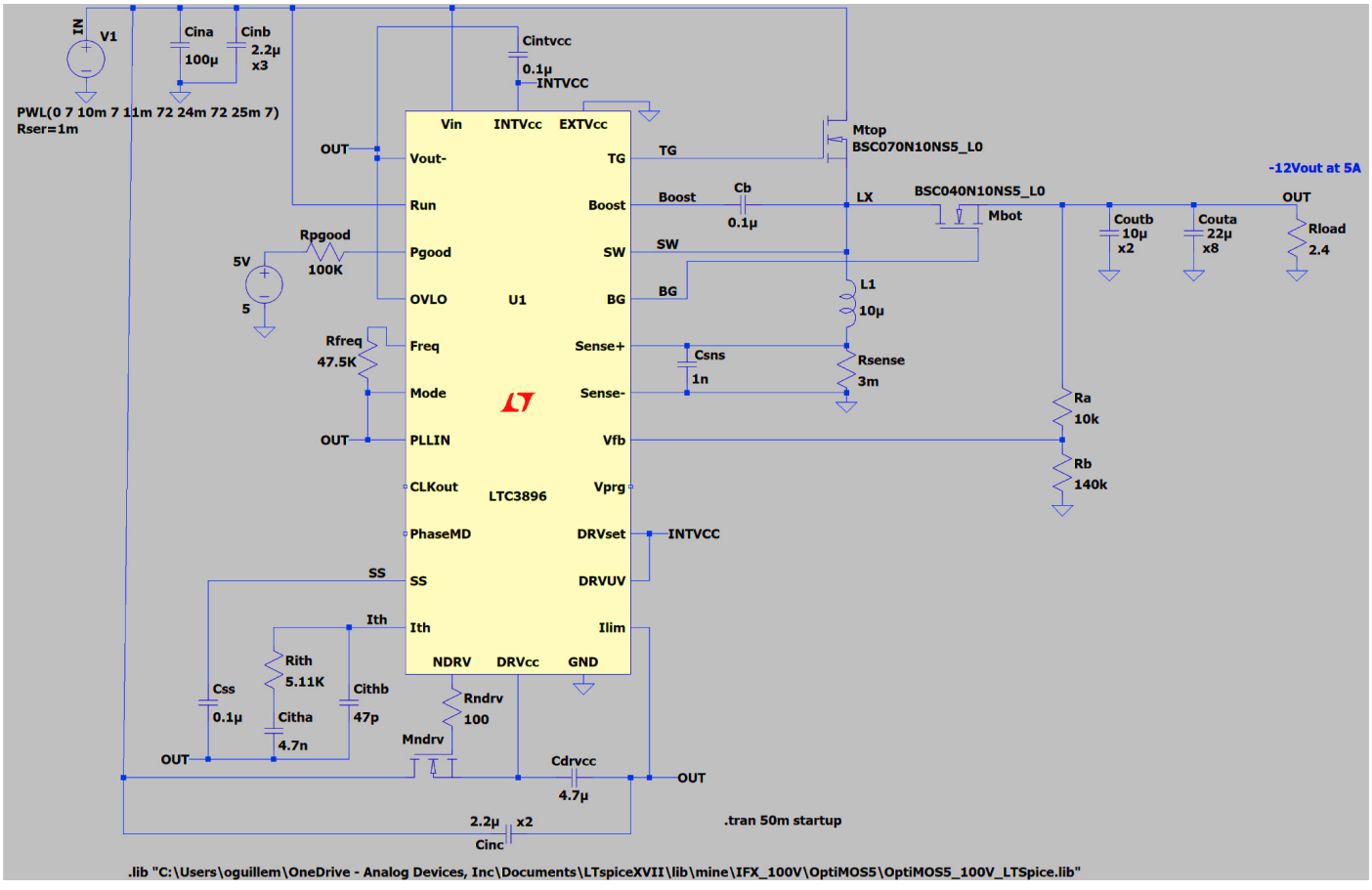
Moreover, staying within this recommended range between 30% and 70% of $I_{OUT,MAX}$ means that we can only afford a ratio of up to 2.33—that is, 70% divided by 30%—between the highest and lowest current ripple over our input-voltage range. This isn't a trivial task for a topology such as the inverting buck-boost, where ΔI_L varies significantly with V_{IN}, as previously observed.

Referring to *Figure 7*, when using f_{SW} = 1 MHz and L = 1 µH, the coil current ripple would vary between 4.42 and 10.29 A, which is far too much. To position the lowest ΔI_L to our recommended lower limit of 1.5 A or 30% of $I_{OUT,MAX}$, we need to reduce the existing value of 4.42 A by a factor of three. This can be achieved by setting f_{SW} to 300 kHz with a 47.5-kΩ resistor at the FREQ pin and selecting a 10-µH inductance. Indeed, this scales down ΔI_L by (1 µH × 1 MHz)/(300 kHz × 10 µH) = 1/3.

Thanks to this scaling, the coil current ripple, or ΔI_L, should now vary between about 1.5 and 3.4 A (between 30% and 68% of $I_{OUT,MAX}$) over the whole input voltage range, which is just within the recommended range. We obtain the circuit provided on the last page of the LTC3896 datasheet, which is reproduced in *Figure 8*.

Validating Our Inductance Selection with LTspice

Regarding the coil current ripple, more accurate values can be obtained by simulating the same LTC3896 circuit with

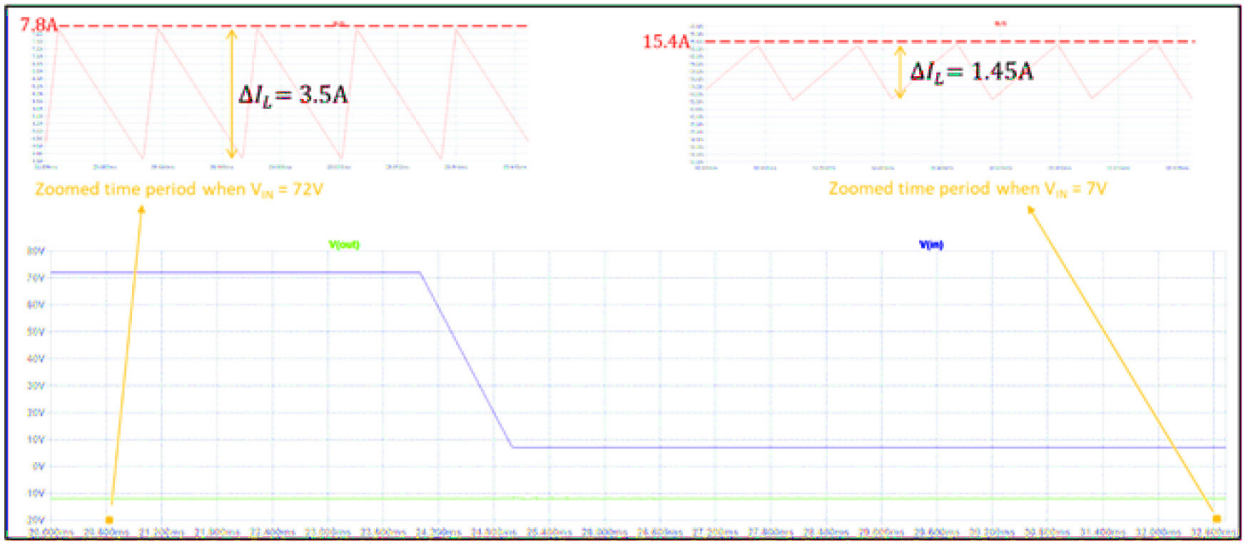


9. LTC3896 circuit simulated with LTspice.

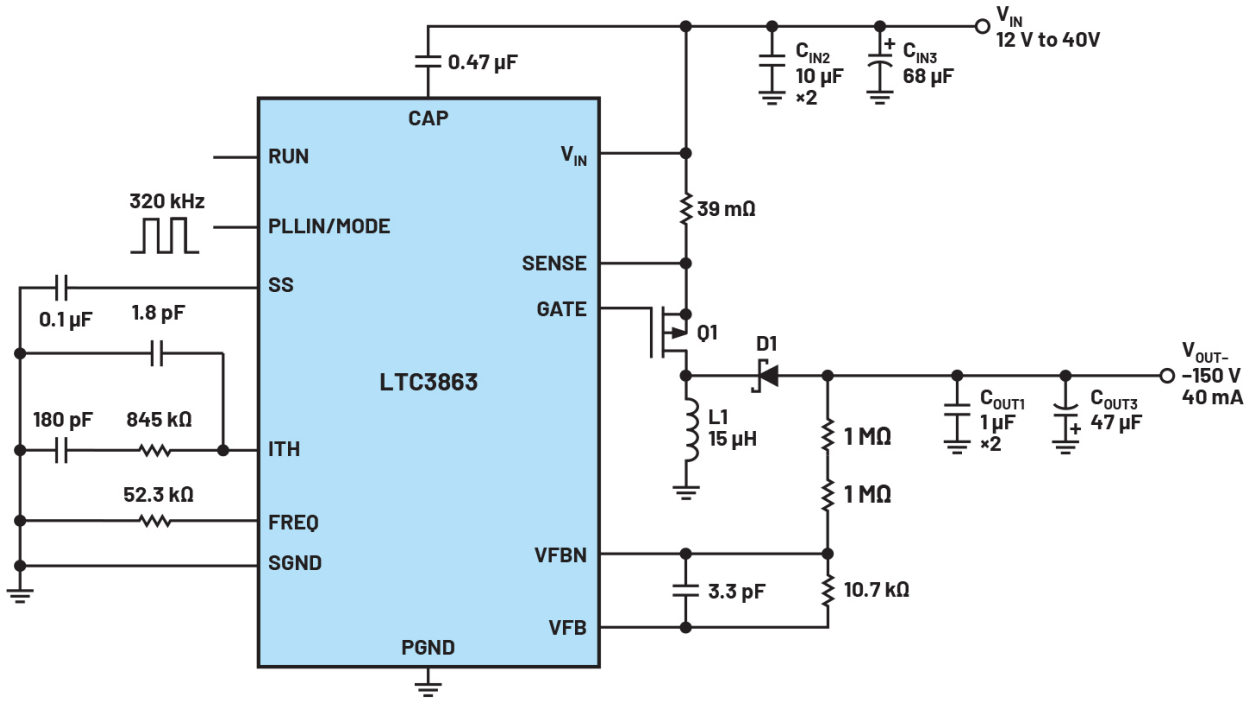
LTspice, as demonstrated in *Figure 9*.

In *Figure 10*, ΔI_L equals about 1.45 A and 3.5 A at V_{IN} = 7 V and 72 V, respectively, which is consistent with the first-order approximation values previously extracted with the help of *Figure 7* and the scaling of the f_{SW} and L. Please note that the coil current probed in *Figure 10* is considered positive when flowing toward R_{SENSE}.

An additional benefit of the LTspice simulation is to determine the peak coil current faced during operation, which is obtained at the lowest input voltage of 7 V. As seen in *Figure 10*, our application will face a peak coil current close to 15.4 A. By knowing this value, a power inductor with a high



10. Measuring ΔI_L at V_{IN} = 7 and 72 V and extracting the peak coil current with the previous LTspice circuit.



11. An LTC3863 circuit with V_{IN} = 12 V to 40 V, V_{OUT-} = –150 V, and f_{SW} = 320 kHz.

enough current rating can be selected.

Designing with Even Higher Output Voltages

Returning to *Figure 7*, current ripple values also were provided for a hypothetical case with a V_{IN} range from 12 to 40 V and a V_{OUT} equal to –150 V.

The first remark is that the current ripple is getting significantly higher for higher V_{OUT} when keeping the same f_{SW} and L. Such high ΔI_L are often unacceptable. Therefore, we would have to apply a higher scaling down factor compared with the previous example, which means a higher inductance for the same f_{SW}.

The second remark refers to the variation of ΔI_L over the whole input voltage range. For the previous example with V_{OUT} = –12 V, ΔI_L was only increasing by about 2.33 from lowest to highest ripple, with the input voltage increasing more than tenfold. For the present case with V_{OUT} = –150 V, ΔI_L already increases by 2.85 from lowest to highest current ripple—and this despite the input voltage only increasing by a factor 3.33 from 12 to 40 V.

Luckily, such challenges only exist in CCM. When in discontinuous conduction mode (DCM), limitations such as 30% to 70% of $I_{OUT(MAX)}$ no longer apply. As it is, it would be too strenuous to convert V_{IN} = 12 V to V_{OUT} = –150 V at $I_{OUT(MAX)}$ = 5 A in a single step. In any case, when such voltage conversions are required, the output-current requirement is generally low, meaning that we operate in DCM. This is, for example, the situation for the circuit on the last page of the LTC3863 datasheet, reproduced in *Figure 11*.

Due to the low dc currents, using a nonsynchronous controller such as the LTC3863 was good enough to provide an acceptable efficiency under these conditions. In the case of this LTC3863 design in DCM, the LTC3863 circuit provided with LTspice is a nice tool to optimize the coil selection.

Conclusion

The hot loop of the inverting buck-boost topology includes components located on both the input and output sides, making its layout more difficult to implement than the buck and the boost topology.

Although there are some analogies to the boost, the inverting buck-boost faces much more current ripple under similar application conditions because its coil constitutes the only source of energy to the output (if we ignore the output capacitance).

For inverting buck-boost applications with high input and/or output voltages, the coil current ripple is potentially even higher. To contain it, higher inductance values are used compared with the boost topology. A practical example was used to demonstrate how to quickly scale the inductance based on the application conditions.

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Reference

1. Dostal, Frederik. "The Art of Generating Negative Voltages." Power Systems Design, January 2016.