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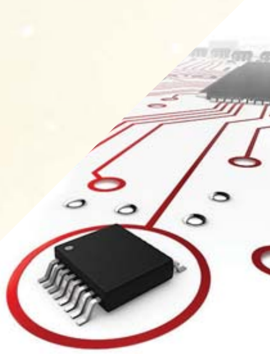

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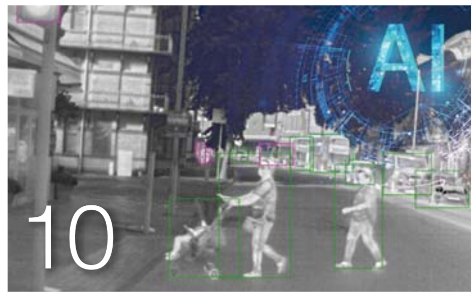

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To provide the most current, accurate, and in-depth technical coverage of the key emerging technologies that engineers need to design tomorrow's products today.

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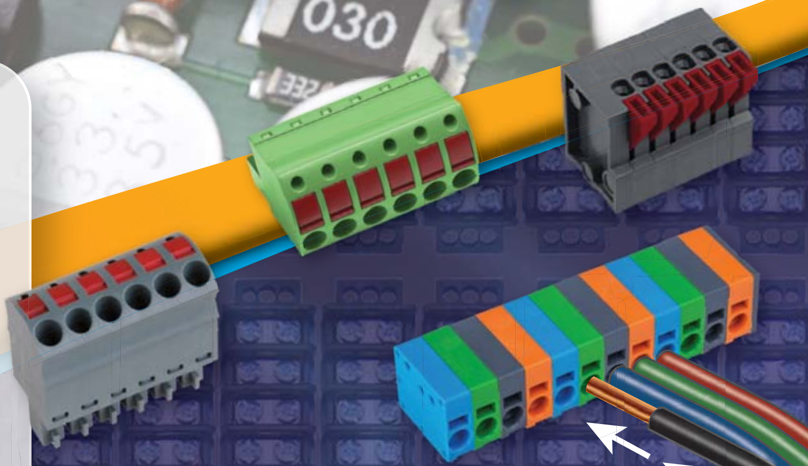

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ElectronicDesign 70 YEARS

Editorial

WILLIAM WONG | Senior Content Director

Looking Forward to the NEXT 70 YEARS

We take a look forward and back at *Electronic Design* and the industry it covers.

THIS YEAR MARKS the end of *Electronic Design's* 70th anniversary, while 2023 is the launch of our next 70 years of covering the electronics industry. It's been an amazing ride—I've had the chance to read about it in *Electronic Design* when I was a budding engineer and later as a programmer and finally as the editor.

Much has changed over the years in both the technology we cover as well as the way we do it. When it started, the idea of the internet was strictly science fiction and laying out a print issue took weeks. Video was film and color televisions were just starting out. Computers filled rooms.

Now everyone is making their own videos using smartphones that fold and fit in a pocket with resolutions pushing the limits of the viewer. Forms of artificial intelligence (AI) have become ubiquitous, providing natural-language processing and support for self-driving cars. A single chip has more computing power than the entire world had decades ago.

We've been changing as well. Articles tend to be shorter, but we've been collecting and linking related content in our TechXchange and library with updates and additions that weren't possible with a static print edition. Our sister publication, *Microwaves & RF*, is launching its bi-monthly digital edition with embedded video.

While many will marvel at the latest technology, it's worth noting that even at its inception, the technology covered by *Electronic Design* exceeded what one engineer or programmer could hope to understand or utilize. It continues to be a team effort that builds on existing technology to deliver new products as well as create new technology to exceed what's currently available.

Yet, much remains useful from the past as evidenced by our Ideas for Design series. Power and analog technology is a mainstay in this series, where articles from decades ago are still relevant and useful today. The interest in our archived evergreen content persists even as the search mechanisms on our site and the internet in general improve to help find that needle in the haystack.

We can only guess what will be available in 2092, assuming AI hasn't taken over or global warming has shut everything down. Women and men have come up with amazing technologies and solutions to a host of problems and we can hope that this will continue. Though we've hit many limitations like raw clock speeds for processors, innovation keeps popping up in the most unexpected places.

In closing, I wanted to mention the passing of one of *Electronic Design's* notable editors, Roger Allan. Roger was executive editor for 23 years and contributing editor for over 50 years. He kept us in line when managing the publication, while covering topics from transistor technology to MEMS. He will be missed. ed

Roger Allen

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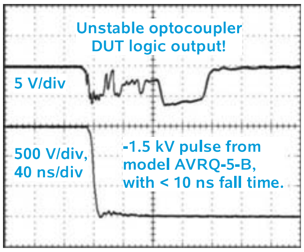
The Avtech AVRQ series of high-voltage, high-speed pulsers is ideal for testing the common-mode transient immunity (CMTI) of next-gen optocouplers, isolated gate drivers, and other semiconductors. GPIB, RS-232, Ethernet ports are standard.



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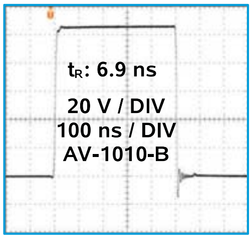

AV-1015-B:	±50V, 10 MHz, 20 ns - 10 ms, 10 ns rise
AV-1010-B:	±100V, 1 MHz, 20 ns - 10 ms, 10 ns rise
AV-1011B1-B:	±100V, 100 kHz, 100 ns - 1 ms, 2 ns rise
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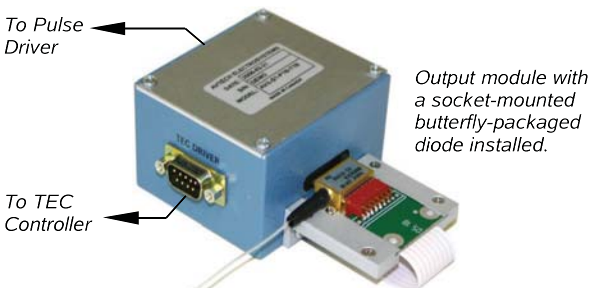

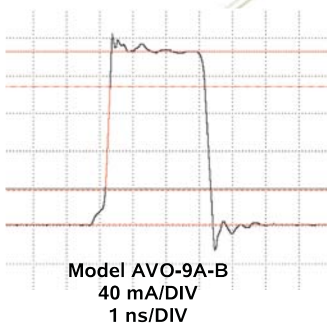

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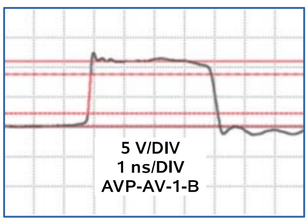

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20 V	120 ps	1 MHz	AVP-AV-HV2-B
20 V	200 ps	10 MHz	AVMR-2D-B
40 V	150 ps	1 MHz	AVP-AV-HV3-B
50 V	500 ps	1 MHz	AVR-E5-B
100 V	500 ps	100 kHz	AVR-E3-B
100 V	300 ps	20 kHz	AVI-V-HV2A-B
200 V	1 ns	50 kHz	AVIR-1-B
200 V	2 ns	20 kHz	AVIR-4D-B
400 V	2.5 ns	2 kHz	AVL-5-B-TR

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JAMES MORRA | Senior Editor

Engineers Are in High Demand:
Most Are Not Missing the Opportunity

Electronic Design's latest Salary Survey revealed that 70% of engineers expect to see their compensation go up this year, as employers continue to compete over hard-to-find expertise.

As electrical and electronics engineers find themselves in high demand, they're pushing their employers to raise salaries, increase bonuses, and offer other perks to complement their pay increases this year.

Around 70% of respondents say that they will see their compensation grow in 2022, up from about 60% in the same situation just last year, according to data from the latest annual survey from *Electronic Design* and Endeavor Business Media's Design Engineering Group. The results signal that engineers still have a strong hand to play when it comes to getting raises and bonuses, as companies compete over scarce talent to fill open positions.

Only a fraction of the nearly 600 respondents, ranging from rank-and-file design engineers to those in executive and engineering management roles, anticipate a reduction in their overall pay this year.

"There will always be new technologies to integrate and old systems becoming obsolete," said one of the respondents to the survey, which polled engineers about their salaries and other forms of compensation. "The opportunities to contribute will never go away."

As most electrical and electronics engineers will tell you, not everyone can do what they do. But while they tend to regard engineering as more of an identity than a profession, they always have money on the mind. Each year, compensation ranks as one of the top factors in their job satisfaction, rivaling the rush that comes with the challenges of designing a new product and the impact their innovations have on the world at large.

While engineers continue to struggle with long hours, tight deadlines, and continuous education, they're prospering for the most part, as rising consumer prices and strong demand for workers help drive up wages.

Bonus Points

While the economic fallout from the pandemic weighed on wages in 2020, times are changing. Last year, many employers doled out bigger pay increases to attract and retain skilled engineers in a tight labor market.

Some warned that high inflation threatens to wipe out many of their pandemic-era pay increases. However, the survey reveals that most professional engineers will still see strong gains in overall compensation this year.

Employers are apparently putting more money into the pockets of electrical and electronics engineers across the board. Among the engineers who responded to the survey, about 23% say that they expect to have a median base salary of $125,000 to $149,999 in 2022 *(see figure, page 9)*. More than 60% of respondents said their base salary will fall into the range of $100,000 to $199,999, signaling that companies are willing to pay for engineering talent.

Nevertheless, compensation for engineers is rising at uneven rates in different industries, and it often depends on a wide range of other factors like education, title, experience, age, and geographic location, among others.

"Technology is constantly evolving," said one of the engineers who responded to the survey. "Those that can train themselves in a skill that is or will be in high demand will do well."

The vast majority of employers plan to pay out bonuses this year, supplementing engineers' salaries with a median bonus of $2,000 to $2,999. About 21.5% of respondents are in store for $5,000 or more in bonus pay this year.

Lots of factors are at play when it comes to calculating bonuses. Many of the respondents (42.7%) get bonus pay based on their personal performance, while others (45.6%) said that their bonus depends on the company's performance.

Still others (19.7%) indicated that they partake in profit sharing. It's relatively rare for engineers to get bonuses for anything else, such as finishing a design, hitting a project milestone, or being awarded a patent.

Only around a third of respondents said they expect stocks to be part of their compensation package this year. About 15% noted their employers offer purchase plans so that they can buy stock at a discount. And approximately 13% of professional engineers are counting on $10,000-plus in stock awards in 2021, according to the survey.

In terms of compensation, about 25% said that it will rise by more than 6% this year—almost double the total in 2021—signaling that companies are raising engineering pay even as the global economic outlook darkens.

According to the results, around 45% report they will see wage growth of between 1% and 6% in 2022. But as inflation rises rapidly, these paychecks will not go as far as they once did—or as far as they want.

About 22% said their compensation will be unchanged, whether because of economic pressures, business challenges, cost-saving measures, or other factors, such as older workers reaching the top of their pay range or retiring. Only about 8% of engineers said their wages will decrease this year, about the same percentage as last year.

The gains in compensation come as companies confront what they claim is a widening talent shortage. The apparent shortage of engineers—or at least the perception of it—has been worsening for years at this point.

In 2020, 54% of survey respondents said their companies were having hiring troubles. In 2021, the figure soared to 67%. Now, over 76% say they're struggling to find qualified candidates for open positions.

And while many engineers complain that they have to move into management or executive roles to start seeing strong gains in compensation, the shortage of engineering talent is paying off for workers with the skills sought by companies.

As one pointed out, "I think companies are starting to realize they need to pay better to keep their top talent."

Staying Competitive

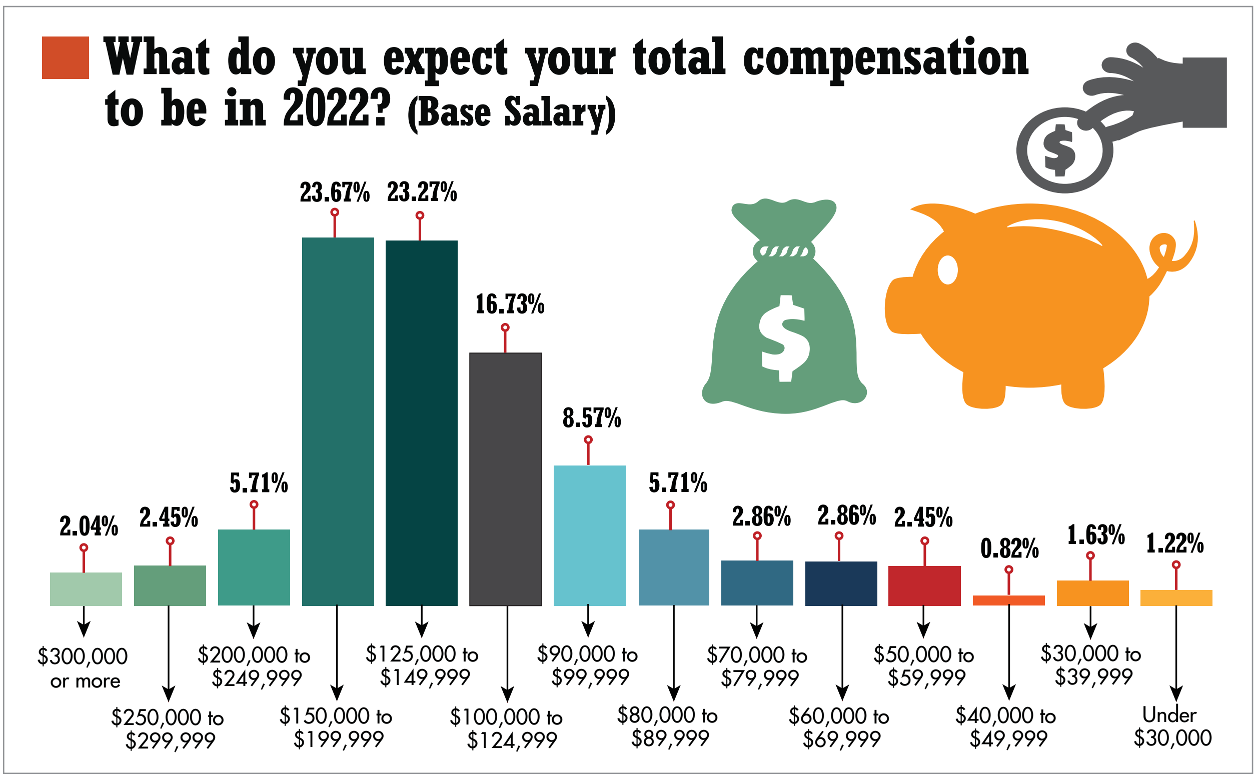
While many engineers feel as though they deserve to be making more money, around 90% say they would recommend engineering as a career path to young people looking for competitive pay and room for growth.

Said one respondent, "The need for engineers will always be there and, if history proves anything, new fields of engineering will be developed in future generations."

Around two-thirds of engineers say their employers sufficiently compensate them for their work, a slight increase compared to last year. But many can't shake the feeling that the grass is greener on the other side of the electronics industry.

About 36% feel their compensation is as competitive as what other companies are paying for the same job, while only 25% said they're probably better compensated than their peers at other employers.

(Continued on page 30)



ART STOUT | Director of Product Management, AI Solutions, Teledyne FLIR

Teledyne FLIR

Improving Convolutional Neural Networks at the Edge

Artificial intelligence and more specifically, machine learning, with human augmentation requires a thorough strategy to achieve a breakthrough.

The concept of a perception neural network was first described as early as the 1950s. However, it wasn't until recently that the necessary training data, neural-network frameworks, and the requisite processing power came together to help launch an artificial-intelligence (AI) revolution. Despite the tremendous growth of AI technology, the AI revolution continuously requires new tools and methods to take full advantage of its promise, especially when dealing with imaging data beyond visible wavelengths of the electromagnetic spectrum.

One such data type is thermal imaging, or the ability to capture long-wave infrared (LWIR) data. Thermal is a subtype of a much larger world of imaging that emerged in the latter half of the 20th century, including LiDAR and radar.

Thermal imaging has proven critical for many applications. Specific properties make it complementary to other image modalities, as it provides both humans and machines the ability to "see" at night, through smoke and fog, and it's unaffected by sun glare.

Today, organizations are focusing on extracting automated decision support from infrared imagers. Then they combine that data with visible video cameras, radar, and LiDAR, which are deployed in a wide range of systems including automotive safety, autonomy, defense, marine navigation, security, and industrial inspection.

However, leveraging the power of thermal imaging for AI through machine learning, with the help of human augmentation, is easier said than done. Critical to the task is ensuring captured data can be processed closest to each camera. Thus, deep learning and its attendant processing should happen at the edge.

Engineering Focus: Considerations for AI, Compute, and Hardware

There are several important considerations when evaluating AI computing platforms for thermal imaging, The first is the effective number of arithmetic logic units (ALUs) available to perform AI workloads. It's common to utilize neural-network accelerators, GPUs, DSPs, and CPUs for portions of the workload.

When making a hardware selection, it's key to understand the strengths and weaknesses of each platform, and to budget resources accurately. The ability to run multiple software routines simultaneously is critical to automatic target recognition software. Without adequate processing power, the software must fit the various routines into the time slice available, which results in dropped frames.

A second consideration is the type and amount of memory the processor can access. Fast and sufficient memory is vital to achieve inference at high frame rates while running all of the software routines, such as warp perspective, optical flow, object tracking, and the object detectors.

A fitting example involves processors featuring integrated LPDDR5 memory with at least 8 GB designed into several intelligent cameras. For example, one widely used type of AI stack software requires between 1 to 5 W when running on an Ambarella CV-2 or Qualcomm RB5165 processor.

Power consumption is managed by selecting networks that fit the power budget specified by the integrator and still meet performance requirements. Object-detection performance is impacted by these configurations, but performance gains continue to be made with more efficient neural networks and new node generation vision-processor hardware.

Processor Choices

Product developers make many decisions when designing cameras with onboard intelligence at the edge. The most impactful is the selection of the vision processor. NVIDIA is a leader in AI compute platforms due to graphics processing technology being ideal for the highly parallel computational demands of neural networks, and for their ecosystem of open-source intellectual property (IP) for network training and runtime deployment.

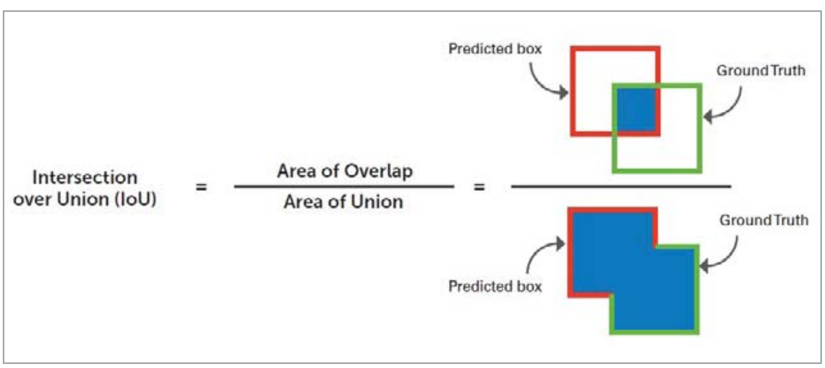
While NVIDIA's platforms continue to be powerful, other leading vision processor suppliers, such as Altera, Ambarella, Intel, MediaTek, NXP, Qualcomm, and Xilinx, also have developed highly competitive chip architectures that feature neural-network cores or computational fabrics designed to process neural-network computational loads at significantly lower power and cost.

A growing number of suppliers offer powerful vision processors. However, it's often not feasible for smaller developers to source cutting-edge processors directly from the manufacturers who typically direct smaller volume customers to partner firms offering system-on-module (SOM) solutions and technical support. It can be advantageous to work directly with the vision processor supplier, because the integration of complex multi-threaded runtime routines requires close support from them.

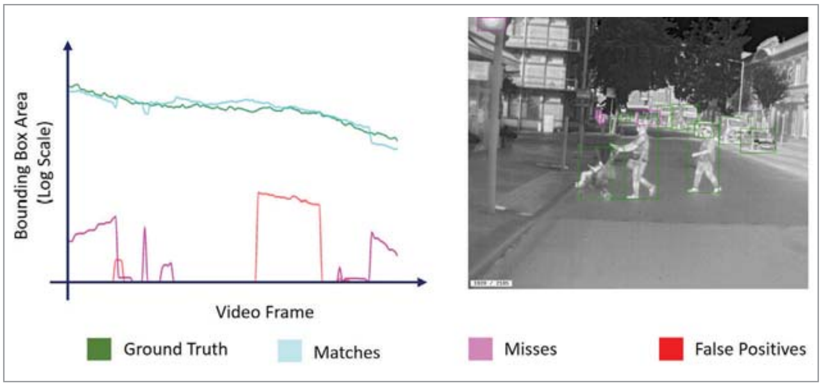
Performance for Convolutional Neural Networks (CNNs)

While an increased number of processor choices exist for running models at the edge, model training is typically done on NVIDIA hardware due to its mature deep-learning development environment built around the company's GPUs.

Neural-network training is computationally demanding, to extremes, and when training a model from scratch, a developer can expect training times of up to five days on a high-end multi-GPU machine. Local



1. The intersection-over-union (IoU) model can help identify performance measures.
Teledyne FLIR



2. This image is an example of visual model performance software output and its associated infrared image. *Teledyne FLIR*

servers are typically used for cost considerations, although training also can be performed on popular cloud services.

The second decision a developer must make is to select the neural-network architecture. In the context of computer vision, a neural network is typically defined by its input resolution, operation types, and configuration/number of layers. These factors all translate to the number of trainable parameters that have a high influence on the computational demand. Computational demands translate directly to power consumption and the thermal loads that must be accounted for during the design of products.

The trade space dictates tradeoffs between object-detection accuracy and frame rates for a given vision processor's computational bandwidth. Video camera users typically demand fast and accurate object detection that enables both human and automatic feedback response by motion-control systems or alarms.

A good example is automatic emergency braking (AEB) for passenger vehicles: A vision-based system detects a pedestrian or other objects within milliseconds and then initiates braking to stop the vehicle, leveraging data from multiple sensor types including radar, visible, and now thermal imaging.

In addition to understanding the performance of models *(Fig. 1)*, data scientists need to analyze the cause of false positives and false negatives or "misses." Here, a subscription-based dataset management cloud software tool can be ideal, especially one that includes a local visual model-performance tool capable of visualizing model performance.

Such a tool can be used to interactively explore and identify areas where the model performs poorly, enabling the data scientist to more effectively investigate the specific training dataset images that cause the missed detections. Developers can then quickly modify or augment the training data, retrain, retest, and iterate until the model converges on the required performance.

It's also instructive to understand the number of calculations performed by neural networks. For video applications such as automotive safety systems, computations are performed on every video frame *(Fig. 2)*. It's critical to get rapid object detections to eliminate latency. For other applications, including counter unmanned aerial systems (C-UAS), quick detection and object location meta data is a critical input into a video tracker that controls the camera and counter-measure pointing actuators.

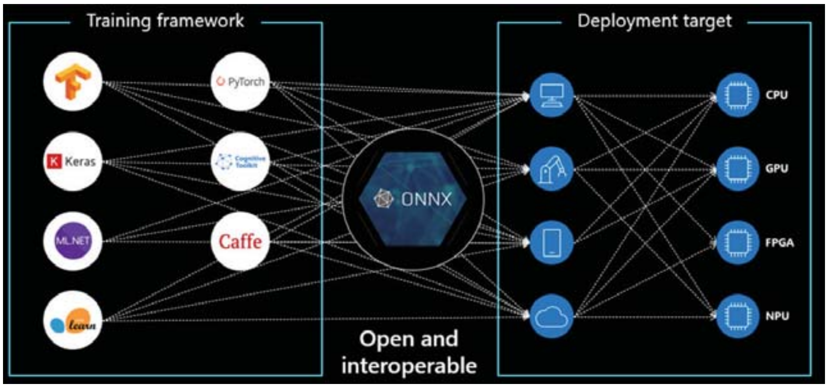
The *table (below)* includes neural-network parameters, input resolution, and the associated processing demands for four example models for informational and comparison purposes. These estimations don't account for how well the architecture utilizes the specific hardware, so it's important to note that the most reliable way to benchmark a model is to run the model on the actual device.

At the end of a training process, the model typically needs to be converted to run on the target vision processor's specific execution fabric. The translation and fit process is extremely complex and requires a skilled software engineer. This has been a significant point of friction in preventing a faster deployment of AI at the edge.

In response, an industry consortium established ONNX AI, an open-source project that established a model file-format standard and tools to facilitate runtime on a wide range of processor

Model	Input Resolution	Number of Trainable Model Parameters (M)	Multiply-Accumulators (MACs) (GFLOPS)
Inception_v3	300 x 300	27.16	5.75
Resnet50	224 x 224	25.56	4.14
FLIR Compact	480 x 480	8.51	2.41

The table includes neural-network parameters, input resolution, and the associated processing demands for four example models for informational and comparison purposes. *Teledyne FLIR* targets *(Fig. 3)*. As ONNX becomes fully supported by vision-processor suppliers and the developer community, the efforts required to deploy models on different hardware will significantly reduce a pain point for developers.



3. This image depicts the OXXN AI open-source operational model to help standardize a model file format and associated tools. *(https://microsoft.github.io/ai-at-edge/docs/onnx/)*

AI Stack Development

Figure 4 includes examples of the frameworks, datasets, libraries, neural networks, and hardware that make up the typical AI stack. Vendors continue to develop and manufacture LWIR, mid-wave infrared (MWIR), and visible light cameras that can and are being developed to utilize AI at the edge. Given the requirements and lack of mature tools associated with multispectral sensing, in particular, unique software, datasets, and more, must be developed to support AI at the edge for different sensor types.

To achieve this, a PyTorch framework can be implemented, which is tightly integrated with Python. PyTorch supports dynamic computational graphs, allowing the network behavior to be changed programmatically at runtime. In addition, the data parallelism feature allows PyTorch to distribute computational work among multiple GPUs as well as multiple machines to decrease training time and improve accuracy.

Datasets for object detection are large collections of images, whether or not they consist of thermal or visible images, that have been annotated and curated for class balance and characteristics such as contrast, focus, and perspective. It is industry best practice to manage a dataset like software source code and utilize revision control to track changes. This ensures machine-learning models maintain consistent and reproducible performance.

If a developer encounters performance issues with a model, data scientists can quickly identify where to augment the dataset to create a continuous improvement lifecycle. Once a verified improvement is made, the data change is recorded with a commit entry that can then be reviewed and audited.

While open-source datasets like Common Objects in Context (COCO) are available, they are visible light image collections containing common objects at close range captured from a ground-level perspective. Meanwhile, many emerging applications, as mentioned above, are now requiring multispectral images taken from a variety of angles and contexts, from air to ground, ground to air, across water, and of unique objects, including military objects.

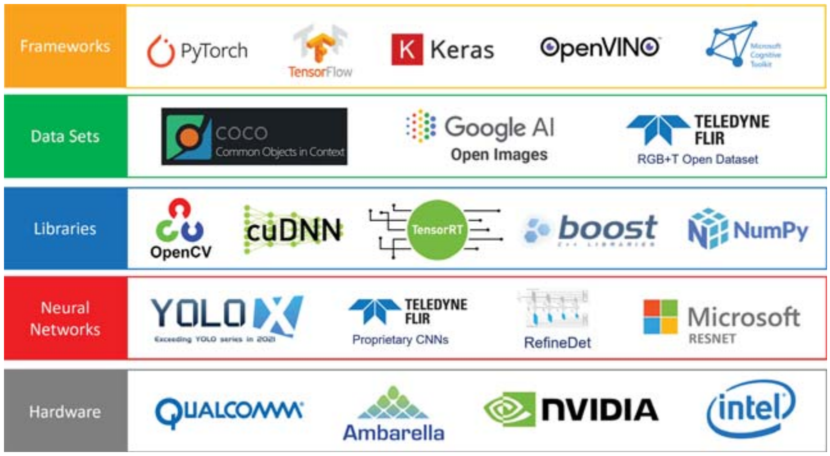
For example, to facilitate the evaluation of thermal imaging for automotive safety and autonomy systems developers, open-source datasets can show matched thermal and visible frames. This way, images of targets at various distances can be added to ensure models work well as small object detectors.

Incorporating Synthetic Data to Improve CNN Efficiency and Performance

In the real world, objects are viewed in near-infinite combinations of distance, perspective, background environments, and weather conditions. The accuracy of machine-learning models largely depends on how well training data represents field conditions.

Modern tools that analyze a dataset's imagery and quantify the data distribution based on object label (e.g., the percent of images of person, car, bicycle, etc.), object size, contrast, sharpness, and brightness are extremely helpful. Correlating model performance to data characteristics and then producing a datasheet for each new model release is valuable to data scientists and critical in the ongoing iteration of model development.

The challenge for data scientists is the significant time and expense requirements



4. Shown are notable organizations across the entire AI stack. *Teledyne FLIR*

5. Here's an example of synthetic training data of a tank in thermal imaging and in visible light. *CVEDIA* to build large training datasets, requiring field data collection, curation of frames, annotation, and quality control of label accuracy. This is a bottleneck in deploying AI, but advances in synthetic data can help reduce development time.

Synthetic data helps to create multispectral data and models using computer-generated imagery (CGI), allowing for the creation of multispectral imagery of almost any object from any perspective and distance *(Fig. 5)*. The result is the ability to create datasets of unique objects like foreign military vehicles, or in relatively rare weather environments, such as heavy fog, that would be extremely challenging to do when relying on field data collection only.

Software tools and standards to simplify model creation and deployment are promising and ensure developers can add AI to their respective cameras with lower monetary investment.

AI at the Edge in Production

There's a convergence of development and technology enabling a clearer path to deploy affordable and functional AI at the edge. Lower-cost hardware is being released with improved processing performance that can be used with more efficient neural networks.

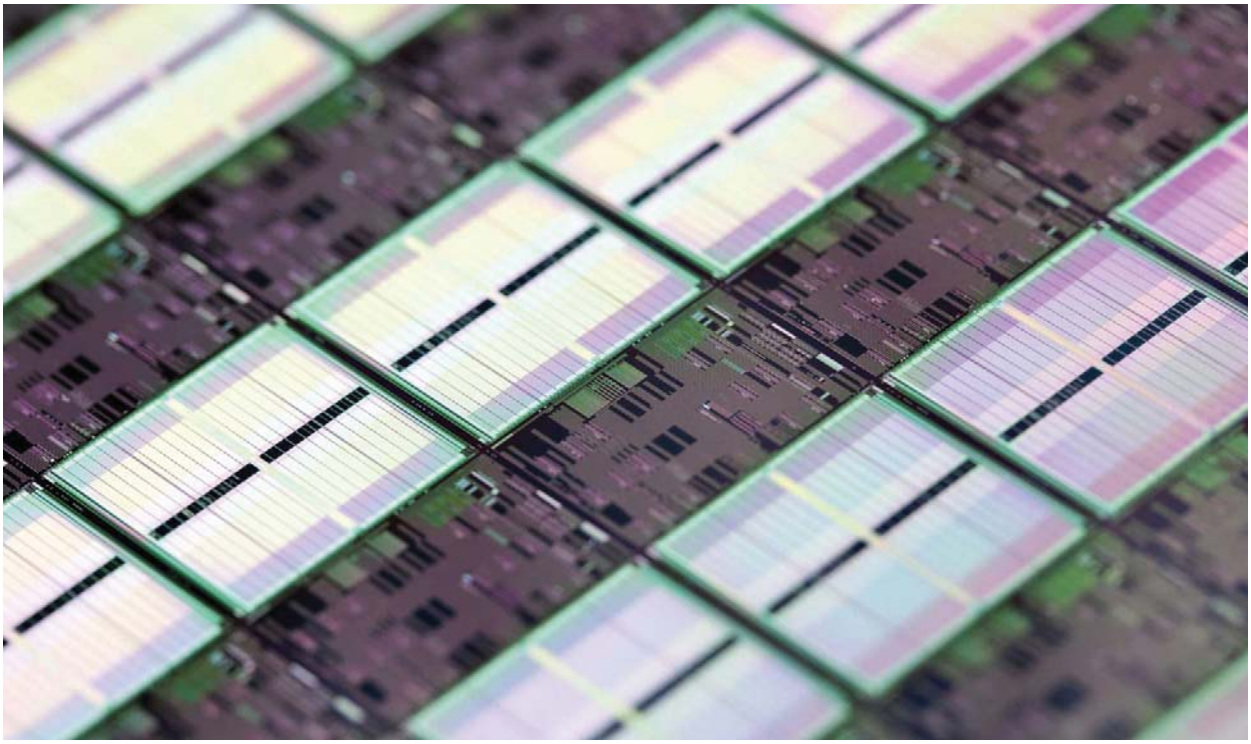
Software tools and standards to simplify model creation and deployment are promising and ensure developers can add AI to their respective cameras with lower monetary investment. The open-source community and model standards from the ONNX community are contributing to this while also aiding in the acceleration of AI at the edge.

As integrators demand AI at the edge in industrial, automotive, defense, marine, security, and other markets, it's important to recognize the engineering effort required to move a proof-of-concept demonstration of AI at the edge to production.

Developing training datasets, addressing performance gaps, updating training data and models, and integrating new processors requires a team with diverse skills. Imaging-system developers will need to carefully consider the investment required to build this capability internally or when selecting suppliers to support their respective AI stacks. ed

JIM HANDY | General Director, Objective Analysis

Dreamstime | Jason-Hippl_17660584



How Embedded Memory Will Drive an Emerging Technology to Success

It seems a new memory technology is needed to shrink MCUs and SoCs without redesigning the memory system and keep costs in check. It's expected that, over the next decade, an emerging memory (PCM? MRAM? FRAM?) will answer that call.

The memory business is at a strange turning point. DRAM process migrations seem to have slowed and there's talk of going 3D… NAND flash has already gone through a relatively painful 3D transition and is now performing extremely well as a 3D memory… and CMOS logic has reached process geometries that can't support on-chip memory.

"WHAT?" you say about that last point. What has that to do with discrete memory chips, and who says that memory can't be supported on CMOS logic? Well, that's an important point, so let's give it a look.

NOR Flash Stops at 28 nm

Most MCUs include NOR flash for their code store, as do many other SoCs. NOR is cheap, and it's available on nearly all foundry CMOS logic processes. This has been the case for decades. But nobody has developed a way to make inexpensive NOR flash on a FinFET process, so NOR is unavailable at process geometries finer than 28 nm. This shows as the leveling off of the red line in *Figure 1*, which represents the relative cost of embedded NOR across process shrinks.

That leveling off might not present a problem if MCUs don't migrate past 28 nm, and as long as none of the other SoCs that use NOR scale past 28 nm. History tells us that this is unlikely.

Some MCU designs that have already passed 28 nm use external serial NOR chips to carry code downloaded on demand to SRAM caches on the MCU. While that can get expensive, since SRAM used six transistors per bit and NOR uses only one, it solves the current problem, and serial NOR chips are pretty cheap.

But that's only a temporary solution, as SRAM also is challenged.

SRAM isn't Far Behind

As processes shrink, it becomes increasingly challenging to make SRAM shrink along with the process. The IEEE International Solid State Circuits Conference (ISSCC) tracks SRAM bit sizes in a historical chart that's updated every year.

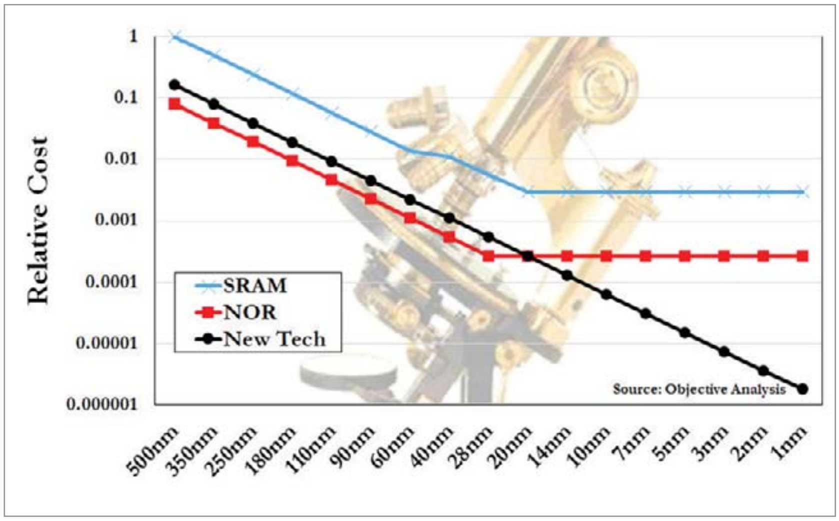
The data in this chart, which runs from 90 nm to 5 nm, shows that the area of SRAM cells in research chips has shrunk an average of 17% per process node while the process has shrunk an average of 21%. At around 20 nm, in some processes, SRAM size and cost stops shrinking altogether *(blue line in Fig. 1)*. Either way, it's less economical to shrink SRAM than it is logic, rendering the SRAM increasingly costly (as a share of overall chip costs) over time.

The industry seems to need a new memory technology that will allow designers to shrink their MCUs and SoCs with process advances and not have to worry about re-architecting their memory system or putting up with a sub-optimal cost improvement.

Is there something that can be used to solve this conundrum?

Emerging Memories to the Rescue

In fact, there is, and it comes in the form of emerging memories—those memories that aren't mainstream today, but could allow the industry to continue to reduce chip costs through pro-



1. NOR levels off at 28 nm. It's not a problem as long as MCUs don't migrate past that point.
Images courtesy of Objective Analysis

cess shrinks *(black line in Fig. 1)*. These emerging memories are the subject of a new report from Objective Analysis and Coughlin Associates: *Emerging Memories Enter Next Phase*. This article is based on a small fraction of the information contained in the 231-page report.

The leading emerging memory technologies today are PCM, MRAM, FRAM, and ReRAM. Each is already in production and has shipped for over five years. Several others are in development in the hope of making their mark on the industry.

In their discrete form, as standalone memory chips, these products have sold into niches, and haven't made great inroads largely due to cost. A paradox is preventing them from making great inroads: They must be cheaper than a mainstream memory (DRAM, SRAM, NOR and NAND flash, and EEPROM) to gain mass acceptance, but until they ship in volumes comparable to the established technologies, they will remain costlier than these established technologies. For years, this has prevented their growth and relegated them to market niches.

The leading emerging memory technologies today are PCM, MRAM, FRAM, and ReRAM. Each is already in production and has shipped for over five years.

However, in embedded applications like MCUs and SoCs, where there's a brick wall preventing the use of NOR flash, these technologies are gaining acceptance. It's also likely that their wafer volume will undergo a dramatic increase in the near future.

With this understanding, we have been able to compile a 10-year forecast for memory revenues that projects the annual revenues for both embedded and standalone emerging memories shown in *Figure 2*, which was taken from the report. We had to use a semi-logarithmic chart to allow the early years to simply show up, since they are so small today.

The chart shows the emerging memory as MRAM, but in reality, it's too soon to tell which technology will actually win the race. What we know is that there's room for only one of these to succeed in a big way, and the others will continue to serve market niches.

While NAND flash and DRAM revenues are growing very modestly, thanks to these technologies' maturity, the MRAM line is growing at a hefty 66% rate, expected to reach $44 billion by the 2032 end of the forecast window. Note that the MRAM line represents combined discrete and embedded memory.

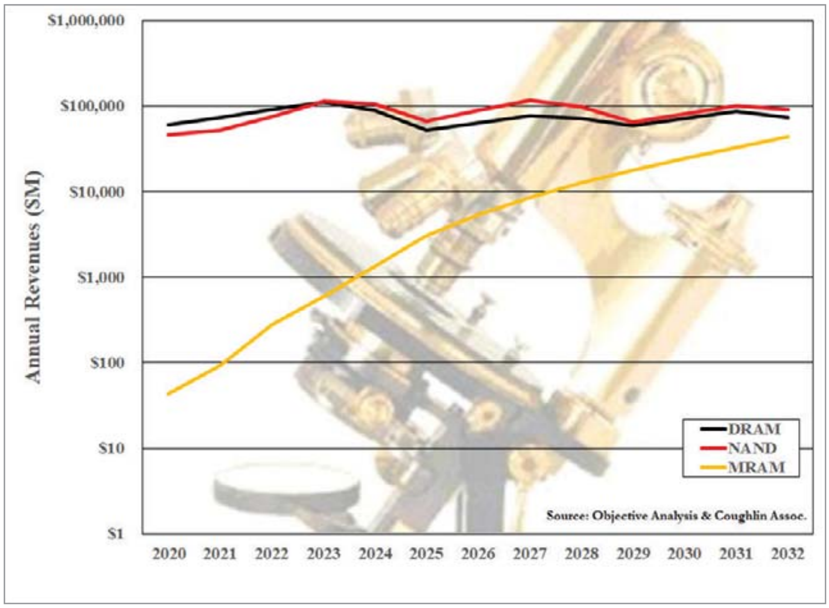
Economies of Scale are Key

The most important determinant of any memory technology's success is cost, and cost can only be reduced by optimizing two factors: process technology and wafer volume. The second of these is a key reason for Intel's recent announcement that Optane was to be "wound down."

For discrete memory chips, this fact presents a nearly impenetrable barrier that stands in the way of widespread adoption. With the help of embedded memories, this should not be as important of an issue for tomorrow's emerging memory technology.

The economies of scale count embedded-memory wafers into the volume equation. Therefore, high-volume production of SoC and MCU wafers that include MRAM, for example, would drive down the production cost of discrete MRAM at the same time. As a result, its market could grow more quickly than without this embedded element. This process feeds upon itself, to drive the costs out of the emerging technology faster than would occur without this embedded element.

In the end, we expect to see rapid growth of an emerging memory over the next decade in both embedded and discrete forms, raising to a level that puts it in competition with today's established technologies. ed



2. It's too soon to tell if emerging memories like MRAM will actually win the race.

ANTON PATYUCHENKO | Field Applications Engineer

RF Demystified: The Different Types of Scattering Parameters

Development of RF applications relies heavily on S-parameters to describe integral structures and constituent RF components at different frequencies and for different power levels of a signal.

Scattering parameters (S-parameters), which describe the fundamental characteristics of RF networks, come in many flavors, including small signal, large signal, pulsed, cold, and mixed mode. They quantify how RF energy propagates through a system and thus contain information about its fundamental characteristics.

Using S-parameters, we can represent even the most complex RF device as a simple N-port network. *Figure 1* shows an example of a two-port unbalanced network, which can be used to represent many standard RF components such as RF amplifiers, filters, or attenuators, to name a few.

The wave quantities, schematically shown in *Figure 1*, are complex amplitudes of the voltage waves incident on Port 1 and Port 2 of the device. If we stimulate one port at a time with the corresponding wave quantity a1 or a2 when the other port is terminated into the matched load, we can define the forward and reverse responses of the device in terms of the wave quantities b. These quantities represent voltage waves reflected from, and transmitted through, the ports of the network.

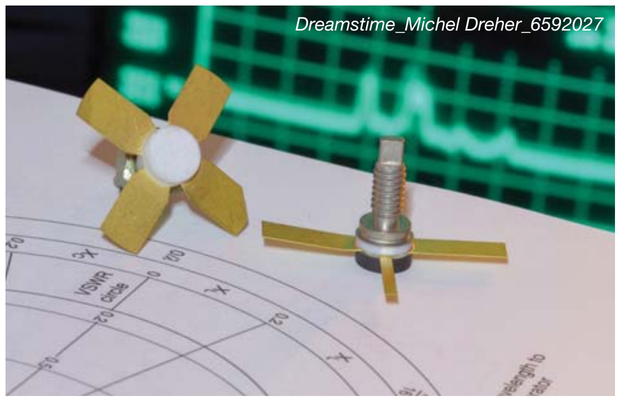
If we take the ratio of the resulting complex responses and the initial stimulus quantities, the S-parameters of a two-port component can be defined as shown in Equation 1:

$$S_{11} = \frac{b_1}{a_1};\ S_{12} = \frac{b_1}{a_2};\ S_{21} = \frac{b_2}{a_1};\ S_{22} = \frac{b_2}{a_2} \qquad (1)$$

The intrinsic response of the network can then be expressed by grouping S-parameters together into a scattering matrix (S-matrix), which relates the complex wave quantities at all its ports. For the two-port unbalanced network, the stimulus-response relation will obtain the form in Equation 2:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad (2)$$

The S-matrix can be defined in a similar manner for an arbitrary N-port RF component.[1,2]



Types of S-Parameters

Small Signal

If not explicitly stated otherwise, the term "S-parameters" usually refers to the small-signal S-parameters. They represent an RF network response to a small signal-stimulus quantifying its reflection and transmission characteristics over frequency in a linear operational mode. Using small-signal S-parameters, we can determine basic RF characteristics including voltage standing wave ratio (VSWR), return loss, insertion loss, or gain at given frequencies.

Large Signal

However, if we continuously increase the power level of a signal that's passing through an RF device, it will often result in more pronounced nonlinear effects. These effects can be quantified using another type of scattering parameter called large-signal S-parameters. They vary not only across different frequencies, but also across different power levels of a stimulus signal. This type of scattering parameter can be used to determine nonlinear characteristics of a device such as its compression parameters.

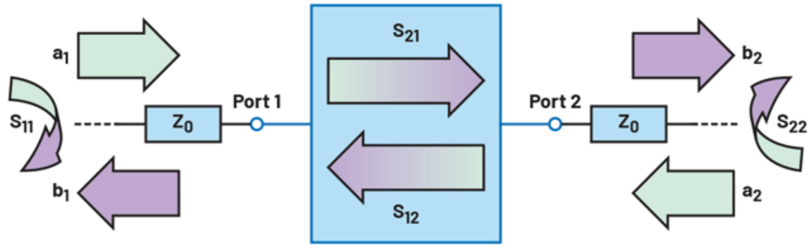
Both small- and larger-signal S-parameters are usually measured using continuous-wave (CW) stimulus signals and applying a narrowband response detection. However, many RF components are designed to be operated with pulsed signals, which have a broad frequency-domain response. This makes it challenging to accurately characterize an RF component using the standard narrowband detection method.

Pulsed

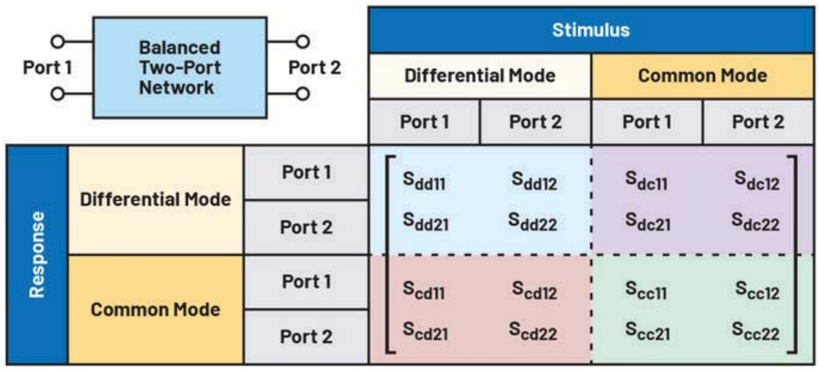
Therefore, for the characterization of devices in a pulsed mode, the so-called pulsed S-parameters, are typically utilized. These scattering parameters are obtained using special pulse-response-measurement techniques.[3]

Cold

Another type of S-parameter that's rarely talked about, but which might sometimes become important to consider, is cold S-parameters. The term "cold" means that the scattering parameters are obtained for an active device in a nonactive mode (i.e., when all of its active elements are inactive; for example, transistor junctions are reverse- or zero-biased and no transfer currents flow). This type of S-parameter can be used, for instance, to improve matching of the signal-chain segments with off-state components that cause high reflections in the signal path.



1. Shown is a two-port unbalanced RF network that could represent a number of RF components. *Images courtesy Analog Devices*



2. This is a two-port balanced RF network and its mixed-mode scattering matrix.

Mixed Mode

Up until now, we've defined S-parameters for a typical single-ended component when the stimulus and response signals are referenced to ground. However, for balanced components that have differential ports, this definition isn't sufficient. Balanced networks require a broader characterization approach, which must be able to fully describe their differential- and common-mode responses.

This can be achieved by using mixed-mode S-parameters. *Figure 2* shows an example of the mixed-mode scattering parameters grouped together into an extended S-matrix representing a typical two-port balanced component.

Subscripts of the mixed-mode S-parameters in this matrix use the naming convention b-mode, a-mode, b-port, and a-port. The former two describe the modes of the response port (b-mode) and stimulus port (a-mode), and the latter two specify index numbers of these ports, where b-port corresponds to the response and a-port to the stimulus port.

In our example, the port modes are defined either by the subscript d—differential—or c—common mode. However, in a more general case of a component that has both balanced and unbalanced ports, a mixed-mode S-matrix also will have additional elements with subscript s describing the quantities obtained for the single-ended ports.

The mixed-mode scattering parameters enable us to determine the basic parameters of an RF component such as return loss or gain. In addition, they make it possible to determine the key figures of merit used to characterize performance of the differential circuits, such as common-mode rejection ratio (CMRR), magnitude imbalance, and phase imbalance.

Conclusion

This article presented basic definitions and briefly discussed the key types of scattering parameters. The S-parameters can be used to describe fundamental characteristics of RF components at different frequencies and for different power levels of a signal.

The development of RF applications relies on the use of S-parameter data describing integral structures and constituent components of RF designs. RF engineers measure or rely on already existing S-parameter data, which is typically stored in standard text files known as Touchstone or SnP files. These files are often freely provided for the most popular RF components available on the market today. ed

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3. "Pulsed Measurements Using Narrowband Detection and a Standard PNA Series Network Analyzer," Keysight Technologies, December 2017.

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11 Myths About Hall-Effect Sensors

As system performance demands escalate in industrial and automotive systems, Hall-effect sensors will continue to see widespread use. This article explores misconceptions regarding these sensors and their impact on real-world applications.

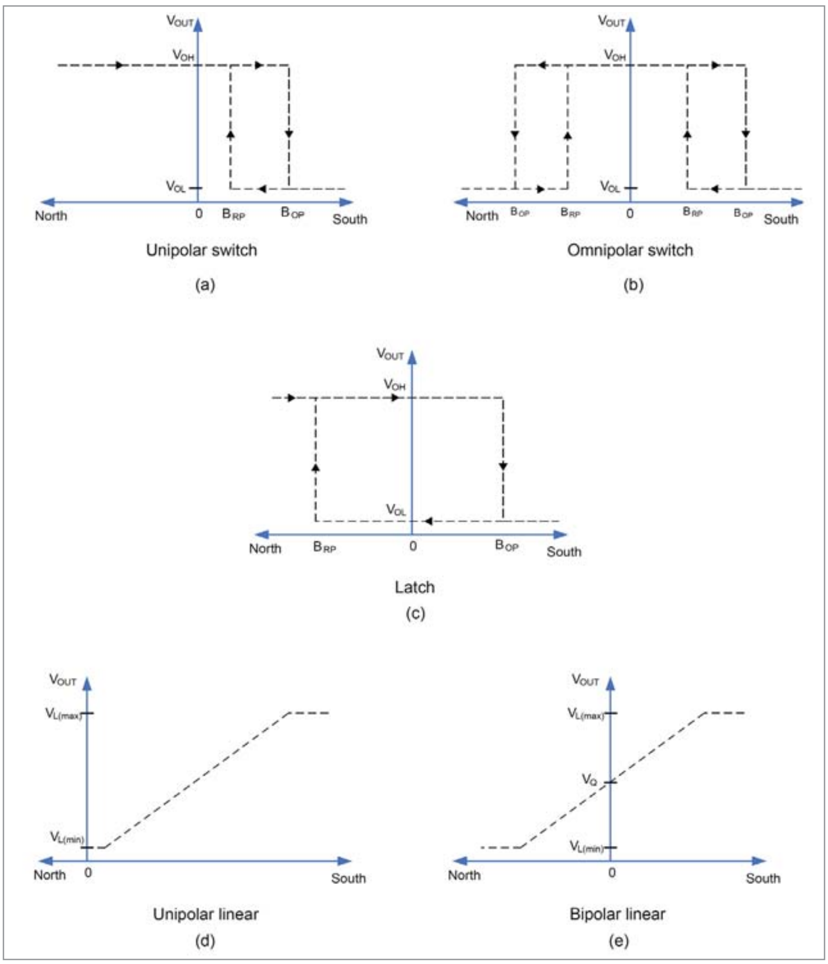
For many years, designers have used Hall-effect sensors in industrial and automotive systems for proximity detection, linear displacement measurements, rotary encoding, and many other applications. Over time, higher system performance demands have pushed integrated-circuit (IC) providers to increase sensitivity accuracy, integrate more functionality, offer different sensing directionalities, and lower power consumption, extending the use of Hall-effect sensors for decades to come.

This article will examine common misconceptions regarding Hall-effect sensors and tie in real-world applications when appropriate.

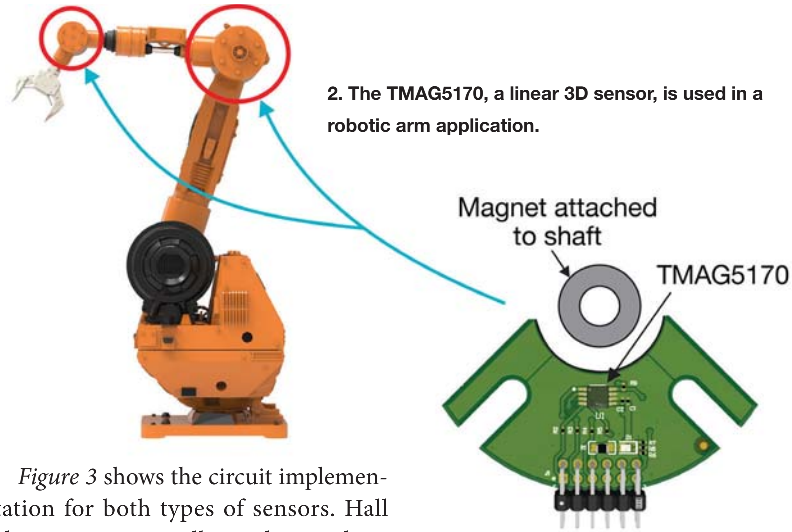
1. Hall-effect sensors provide only simple on and off information.

Many electromechanical designs require the detection of an object with a sensor, which provides a simple logic signal indicating its presence or absence. One example is the closing and opening of a laptop lid, indicating when to power it on or off. Another example is an intrusion event in a door and window sensor. These applications typically use a simple Hall-effect switch that toggles its output voltage once an internal magnetic threshold has been crossed.

While those Hall-effect switches are very useful, they're not the only type of Hall-effect sensor available—latches and linear devices also are quite common. In contrast to a switch, a latch, which is mainly used in rotary encoding, will toggle its output only in the presence of an opposite magnetic polarity to what it had previously experienced.



1. This diagram shows Hall-effect switches (a) and (b), latch (c), and linear sensors (d) and (e) output responses.



2. The TMAG5170, a linear 3D sensor, is used in a robotic arm application.

For precise displacement measurements, linear Hall-effect sensors are preferable because they can define, with high resolution, where an object is relative to the sensor. In other words, they provide much more than on and off information. *Figure 1* illustrates the transfer functions for each type of sensor, including the variations available.

2. Linear Hall-effect sensors are not accurate.

Linear Hall-effect sensors are without question cost-effective solutions that provide reliable magnetic information. Users of such sensors know this fact, but often consider other technologies to meet their high-accuracy requirements.

In industrial robotics, for example, the moving arms must be precisely positioned in relation to the target object. Using a high-accuracy, linear 3D Hall-effect sensor, such as the TMAG5170 from Texas Instruments (TI), offers the precision needed for such applications *(Fig. 2)*. Furthermore, the device's high precision and low-sensitivity drift over temperature potentially eliminates the need for system-level calibration.

3. Hall-effect sensors are the same as Hall elements.

It's simply not true that Hall elements are essentially the same as Hall-effect sensors. The Hall element, which requires bias circuitry and a differential amplifier, is the most basic structure needed to produce a usable voltage. In contrast to Hall-effect sensors, Hall elements don't have all supporting circuitry integrated into a single package.

Figure 3 shows the circuit implementation for both types of sensors. Hall elements are typically used in applications where accuracy isn't critical, cost is extremely important, and a differential amplifier is nearby to minimize external noise coupling. In addition, Hall elements have an inherent nonlinear variation over temperature, while Hall-effect sensors have built-in compensation to ensure stable measurements across a wide temperature range of –40 to 125°C.

4. Hall-effect switches are not useful replacements for reed switches.

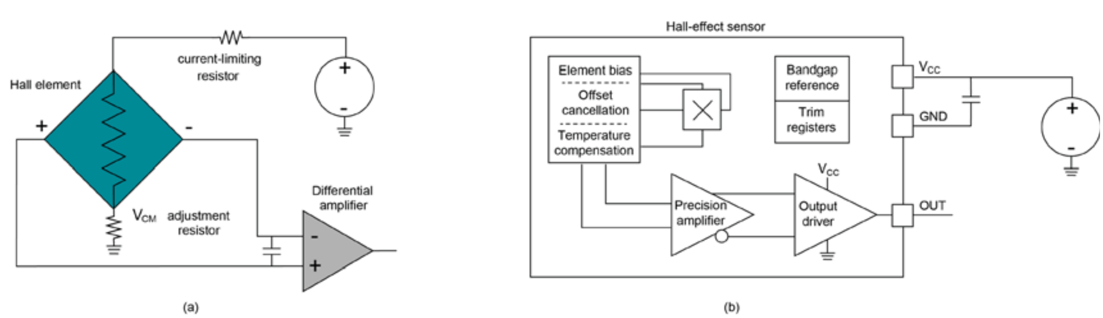
Reed switches are still prevalent today in many applications, such as door and window sensors. The main drawback to using reed switches in security alarm systems is the inability to detect a tampering event. By using a linear 3D Hall-effect sensor, designers can take advantage of any channel not used for active measurement to detect this event.

Another example is in a refrigerator door to control the exact position, where the inside light is turned on or off. Hall-effect switches offer consistent open-and-close distance detection given their tight threshold hysteresis specifications.

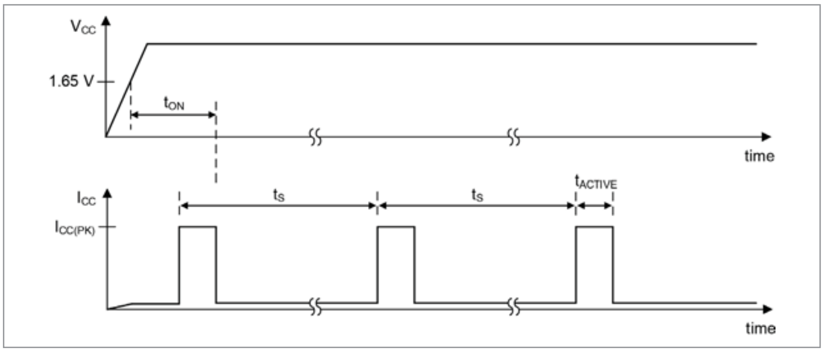
A second major drawback to using reed switches is their inability to use standard printed-circuit-board (PCB) assembly procedures. These devices must be hand-soldered onto the board, thus complicating the assembly process and increasing costs. *Table 1 (on page 24)* compares the two technologies.

5. Low-power solutions are not achievable with Hall-effect sensors.

While it's true that some Hall-effect sensors consume current in the single-digit milliampere range, making them unsuitable for battery-operated applications, other Hall-effect switches support low sampling rates (5 Hz or less) and consume an average current less than 1 µA. These devices cycle between a high-power active measurement state and an ultra-low-power sleep state to achieve low power consumption. Because the active state (tactive) duration is much shorter than the sleep interval (ts), the total average current consumption is very low *(Fig. 4)*.



3. This is the circuit implementation for a Hall element (a) versus a Hall-effect sensor (b).



4. Here, a timing diagram shows the low-power current consumption when in an ultra-low-power sleep state.

Table 1: Comparison of Hall-Effect and Reed Switches

Specifications	Hall-effect switches	Reed switches
Magnet orientation sensitivity	Orthogonal and in plane	Parallel (same as in plane)
Current draw	Microampere range (low-frequency duty cycle)	Microampere to milliampere range (pulsed by microcontroller general-purpose input/output)
Polarity sensitivity	Both poles (omnipolar)	Both poles
Hysteresis	Single-digit milliTesla range	40%-95% variation
Switch loads directly?	Requires additional circuitry	Yes (up to 3 A)
Response time	≅10 µs	25 to 100 µs
Life expectancy	Effectively unlimited operations—limited by silicon life expectancy	From thousands to billions of operations depending on load
Shock susceptibility	None	Yes
Assembly	Standard PCB assembly	Manual assembly with high yield loss (10%)
Operating temperature	–40 to 125°C	–55 to 200°C

Table 2: Head-On Sensing Distances for Two DRV5032 Hall-Effect Switch Variants

DRV5032 variations	Maximum B_{OP}	Distance of maximum B_{OP} (mm)	Minimum B_{RP}	Distance of minimum B_{RP} (mm)
DRV5032FA	±4.8	18.7	±0.5	44.6
DRV5032ZE	±63	4.0	±30	7.5

6. Hall-effect sensors require three wires for offboard sensing.

The vast majority of Hall-effect sensors on the market have only three pins—VCC (power supply), output and GND (ground)—so the general thought is that three wires must be wired to the sensor. This is not true. As shown in *Figure 5*, an open-drain, voltage-output, three-pin Hall-effect switch connects remotely with only two wires.

When sensing a magnetic field, the device will produce a current output through the GND pin. If no field is detected, the device's output will not produce any current and, in turn, produce no output current through the GND pin. Note that determining the logic state of the resistor requires an analog-to-digital converter (ADC), which may be integrated into a microcontroller, and an external resistor. The problem with this configuration is that it can produce invalid voltage levels under noisy conditions.

Ensuring reliable data transmission requires a current-output device to reduce or eliminate signal distortion. The TMAG5124, for example, is a two-pin solution requiring only a power-supply voltage and ground to operate. *Figure 5* shows how to implement the device by using the GND pin to transmit either a low- or high-level current (both in the milliampere range).

7. There's no flexibility in magnet placement when using Hall-effect sensors.

Magnet placement relative to the sensor depends on many factors—some are system-level factors, while others are inherent to the sensor itself. External system factors that dictate the placement of the magnet are mainly the magnet size, magnet material type, and the temperature operating range. The larger the magnet, the larger the magnetic field produced.

Of the most common magnets used, neodymium iron boron (NdFeB) magnets produce the strongest magnetic fields. Thus, they're generally smaller in size.

It's also important to consider heat when selecting a magnet, as it typically degrades the magnetic field produced.

The main factors impacting magnet placement that are specific to the sensor involve sensitivity levels, sensing directionalities (in plane vs. out of plane), package offerings, number of sensors onboard, and configurability. A Hall-effect sensor with higher sensitivity can detect a magnet farther away.

Most Hall-effect switches and latches detect magnetic fields perpendicular to the surface of the package, but some can detect horizontally (or in plane) with the package. A good example of this is the TMAG5123, which provides more mechanical flexibility in designs when vertical displacement isn't possible. Another example is the use of 2D dual-channel latches that are able to monitor multiple axes. You can place them virtually anywhere in relation to the magnet.

8. Hall-effect sensors are not useful for measuring angles.

Hall-effect sensors are popular in many displacement applications, but they're also used for absolute angle measurements. By strategically positioning two single-axis linear Hall-effect sensors about a rotating dipole magnet, each sensor picks up a magnetic field vector that's out of phase with the other. With this information, it's easy to calculate the exact angle of the rotating magnet by using the arctangent function.

Figure 6 shows two implementations using linear sensors in two different package types. Another more elegant way to perform angle measurement is with a single linear 3D Hall-effect sensor *(see Figure 6b for various configurations)*. To learn about angle measurements, go to www.ti.com and check out "Absolute Angle Measurements for Rotational Motion Using Hall-Effect Sensors" and "Angle Measurement With Multi-Axis Linear Hall-Effect Sensors."

9. Hall-effect sensors have a very limited operational range.

There are also those who believe that Hall-effect sensors don't have a good range for practical use because magnetic fields decay exponentially over distance. However, Hall-effect sensors with high sensitivities can detect useful magnetic fields from a good distance away.

For example, take TI's DRV5032. *Table 2* shows the head-on sensing distances of all device variants offered using a small low-cost ferrite magnet (12 ×12 × 6 mm). The lowest-sensitivity DRV5032ZE can detect this magnet from 4.0 to 7.5 mm, while the DRV5032FA version ranges between 18.7 and 44.6 mm. If using a stronger, same-sized NdFeB-grade-52 magnet, this detection distance increases to almost 3 in.

10. Only TMR sensors can take in-plane measurements.

Designers typically consider tunnel magnetoresistance (TMR) sensors because of their high magnetic sensitivity, high linearity, and low power consumption. Plus, TMR sensors can sense magnetic fields horizontally (or in plane) with the package. Most Hall-effect sensors available today are sensitive to perpendicular fields, but a few, such as the TMAG5123, have in-plane sensing capability. However, one advantage in using Hall-effect sensors is a lower total system cost. *Figure 7* shows the sensitivity directionality of an in-plane sensor.

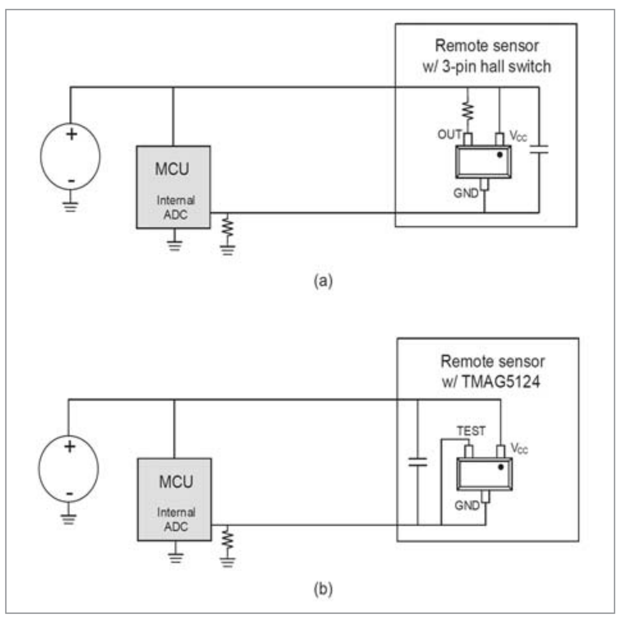
11. It's easy to tamper with systems using Hall-effect sensors.

This is true—it's possible to tamper with systems using reed switches and basic Hall-effect switches. Large external magnetic fields can fool the system into believing that everything is working properly.

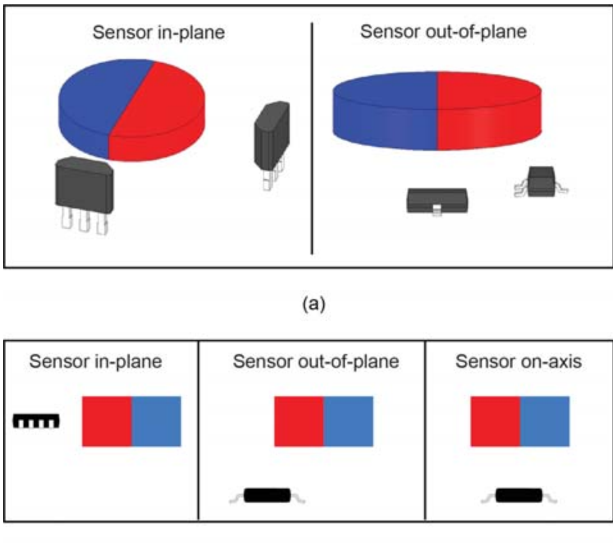
A good way to fix this problem is to use a linear 3D Hall-effect sensor. One axis monitors the presence of the intended magnet, while the other two channels detect external magnetic fields. By using a linear 3D sensor with a configurable magnetic threshold per channel, you have much more flexibility in setting the proper "tamper detection" threshold. In the example shown in *Figure 8,* the MCU receives an interrupt signal once the threshold is crossed.

Conclusion

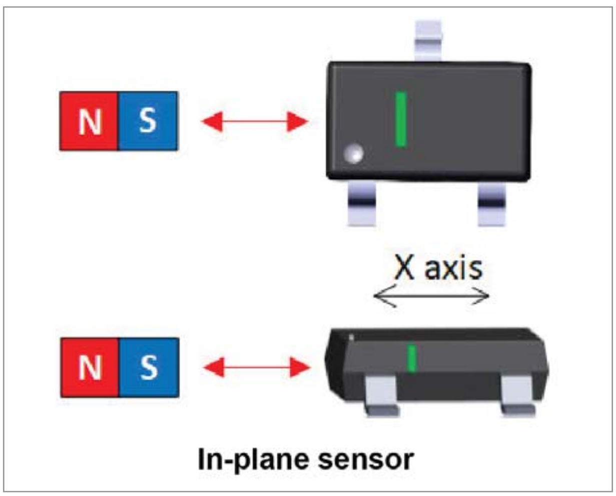
The use of Hall-effect sensors is so widespread that I hear about a new application that's novel and interesting on a near-daily basis. My expectation is that this set of 11 myths will spur an idea for your next-generation design. Care to share yours? ed



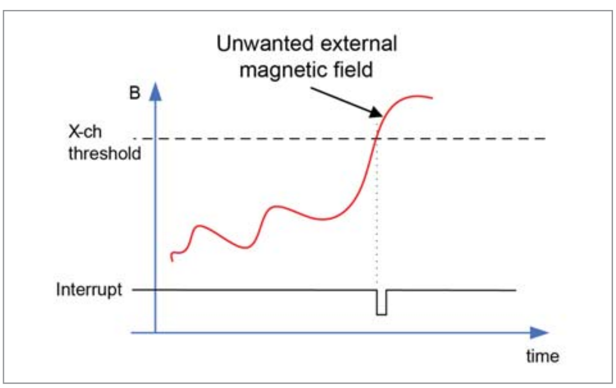
5. Two-wire remote sensing using a voltage-output Hall-effect switch (a) and a current-output TMAG5124 (b).



6. An absolute angle measurement using two single-axis linear Hall-effect sensors (a) and one linear 3D Hall-effect sensor (b).



7. The sensitivity directionality of an in-plane sensor.



8. This graph shows the detection of an interrupted single using a linear 3D Hall-effect sensor.

CABE ATWELL | Contributing Editor

The Ins and Outs of Time-Sensitive Networking

Time-sensitive networking provides a set of standards that looks to drive innovation for automated systems in industrial applications.


Dreamstime | Andrey-Armyagov_143484715

Ethernet has been cemented as a dependable wired solution for computer and automation networks. The open standard enables terminals to be quickly and easily connected and scaled to exchange data with relatively inexpensive hardware.

Ethernet was, however, not originally designed to meet the requirements posed by automation technology, particularly when it comes to big data and real-time communication. Due to those restrictions, various bus systems in automation have evolved using Ethernet on a physical level while implementing proprietary real-time protocols on the top end.

Such systems often lead to the exclusive use of the network infrastructure and vendor dependencies. Networks currently tasked with handling time-critical data are separated from networks directing less-critical data traffic to eliminate reciprocal negative interference.

In the future, Industry 4.0 applications will increasingly require more consistent and robust Ethernet networks. These networks can only be produced at a significant cost with the current infrastructure. To that end, time-sensitive networking (TSN) offers a solution to change these current conditions and provide increased throughput for many industries.

What is TSN?

TSN is a set of standards under development by the Time-Sensitive Networking Task Group, which is part of the IEEE 802.1 working group—an offshoot of the IEEE 802 project created by the IEEE Standards Association (see figure). TSN focuses on creating a convergence between information technology (IT) and industrial operational technology (OT) by extending and adapting existing Ethernet standards.

While it may sound like it, TSN is an Ethernet standard and not an Internet Protocol Standard (IPS). However, the extensions in particular address the transmission of very low transmission latency and high availability.

Now that we're up to speed on lineage, the standards define mechanisms for the time-sensitive transmission of data over deterministic Ethernet networks. Most projects define extensions to the IEEE 802.1Q (aka VLAN support) Bridges and Bridged Networks, which describes virtual LANs and network switches.

TSN technology aims to standardize features on OSI-Layer 2 so that different protocols can share the same infrastructure. The challenge here lies in configuring critical and non-critical data traffic so that neither real-time characteristics nor performance is impaired.

TSN Breakdown

Typically, traditional Ethernet networks involving automated sectors, such as those found in manufacturing, are based on the hierarchical automation pyramid, separating information technology (IT) from operational technology (OT). IT includes classic office communication with typical end devices, such as computers and network-attached-storage (NAS) systems. The OT end comprises systems, machines, and software used for process control and automation.

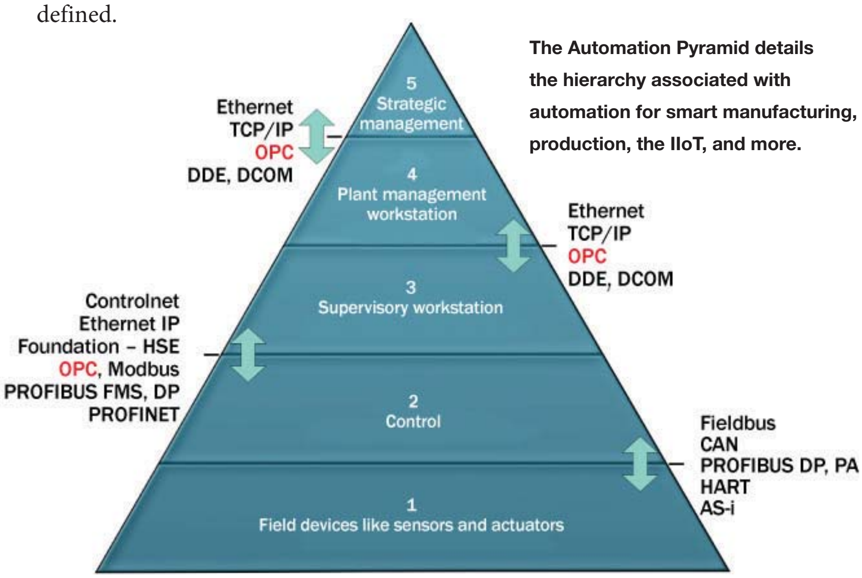
Those areas are essentially different in how they communicate, with IT relying on bandwidth and OT tasked for high availability. Data traffic at the IT level is often classified as non-critical, while data traffic is designated time-critical on the OT end. Because of this separation, each level uses a particular communication standard.

While the Ethernet bus system with TCP/IP is largely prominent at the IT level, various bus systems (aka fieldbus systems) that meet requirements for guaranteed latency times are widespread at the OT level. Each control vendor usually promotes a specific fieldbus system.

For the end-user, it means that selecting the controller also determines the selection of the bus. As a result, the user often became dependent on the manufacturer since the different bus systems were incompatible. This is no longer the case, as continuous data transmission is a fundamental necessity for digitized enterprises, regardless of industry.

Industrial automation is already undergoing a phase of restructuring based on the establishment of flexible and intelligent manufacturing, typically described or already implemented in the context of Industry 4.0, smart production, and the IoT. This is detailed in the automation pyramid, which incorporates TSN and divides the structure in half, with the top portion (strategic management, plant management, supervisory) dedicated to IT and the bottom (control, field devices, etc.) implemented with OT.

The separation of control and field levels is blurring, creating the need for a uniform, convergent network where critical data traffic can be simultaneously transmitted with non-critical data without adverse effects. Thus, the existing Ethernet must be adapted to meet these requirements. This is where the TNS Task Group comes into play, as sub-standards intended to enable converged critical and non-critical data traffic over a shared Ethernet infrastructure are currently being defined.



The Automation Pyramid details the hierarchy associated with automation for smart manufacturing, production, the IIoT, and more.

Time is the Key

All network equipment needs the same understanding of time to meet that aforementioned convergence, which means all switches and terminals on a network must be time-synchronized. To accomplish that task, two different approaches are currently in play.

One is the IEEE 1588-2008 standard, which prompts the provision of the clock with the most accurate time to be designated to act as a Grandmaster Clock, or centralized time element. The Task Group also created a unique profile that outlines the use of IEEE 1588 specifications in conjunction with IEEE 802.1Q, especially those applications that don't require full throughput.

Another important functionality deals with transmitting critical and non-critical data traffic within a converged network. Critical data traffic is prioritized for delivery at a scheduled time, while non-critical data traffic is designated a lower priority. Eight traffic classes are already established according to IEEE 802.1Q, and they're used to prioritize different types of data traffic.

That said, the standard's QoS (Quality of Service) was not designed to send critical and non-critical data traffic in parallel. Due to buffer mechanisms in Ethernet switches, a low-priority Ethernet data packet can delay data streams, even if they're tasked with high priority. New prioritization mechanisms have been introduced to allow and regulate this coexistence.

Enter IEEE 802.1Qav, which is designed for data streams with real-time requirements to be prioritized over best-effort traffic. A great example of that prioritization includes the Credit-Based Shaper (CBS), which was created by the IEEE 802.1 working group to handle priority transmission for the TSN Audio/Video Bridging (AVB) predecessor technology.

The shaper assigns sending credits to data streams. Data packets with reserved bandwidth are preferably transmitted as long as credit remains in the positive range. Those credits are spent during transmission until declining to a negative. Therefore, once a preferred transmission reaches a negative value, the best effort data packets next in line are transmitted. If this delays the forwarding of data packets designated with reserved bandwidth, credit is increased to allow for prioritized Ethernet frames to be transmitted in succession.

Due to the expansive range of TSN functions, integration is best handled by programmable microchips, such as field-programmable gate arrays (FPGAs). Compared to traditional ICs, where functions are predetermined, FPGAs can be programmed and configured to generate complex digital functions based on the application.

Conclusion

The standardization process is not complete, and the implementation of various standards is an ongoing process as new technologies are continually introduced to the market. Since TSN standards are currently still being revised and changed, the possibility to expand and reprogram is a critical factor in implementation and deployment in an industrial setting.

Nonetheless, TSN provides the foundation to meet those changing requirements and the spectrum makes it possible to fulfill the ever-changing latency, jitter, and reliability requirements to meet the latest application requirements. ed

(Continued from page 9)

Over 39% indicated that their compensation is likely less competitive than what other firms are willing to pay this year.

While most respondents said that their companies pay them what they're worth, others feel that they deserve to be making more money—in some cases a lot more. Many think that their salaries are out of step with the level of education that's required for the job, the level of expertise they need to bring to the table, and the increasingly wide range of responsibilities and technologies they must stay on top of to succeed.

Among the one-third of respondents who feel short-changed by employers, more than half believe they're entitled to a raise of 10% to 25%, while around 30% indicate that they should be paid more than 25% over their current salary.

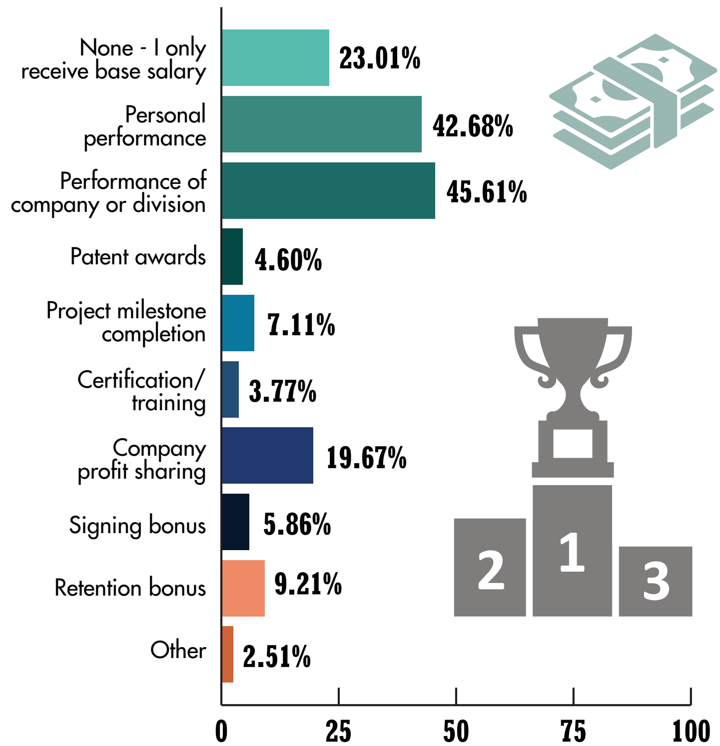
Employers also are increasing non-wage compensation and offering other perks to keep engineers from leaving for other jobs. Many are putting up the money for continuing education, as the engineering shortage pushes them to nurture new skills internally, and even reimbursing for tuition. Some respondents say they're also footing the bill for travel to in-person industry conferences and training courses to keep them up-to-date.

Covering the cost of healthcare continues to be one of the top priorities for employers, according to respondents, and many also are paying for work-from-home-related expenses and resources, including internet.

While electrical engineering can be a grind at times, most professionals said there is room for growth. The potential for salary advancement in engineering, said 68.5% of respondents, is at least as favorable as it was before the pandemic.

As one put it, "Business majors are not going to design these things." ed

Of the bonuses and other direct cash payments over and above base salary that you receive, please specify the primary reason(s) for them?



Ad Index

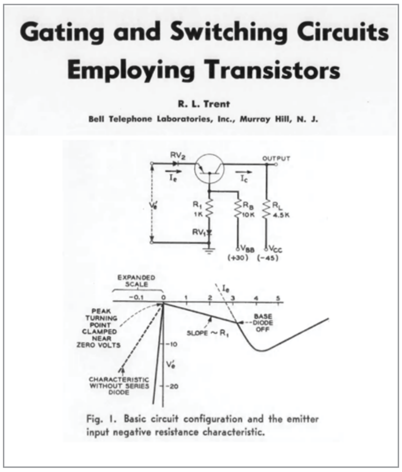
WILLIAM G. WONG | Senior Content Director

Electronic Design: Then & Now

We take a look back at *Electronic Design* issues over the years as we wrap up our 70th anniversary.

Electronic Design magazine has been around longer than me and I've been around a long time. My father was an electrical engineer, too, and would have read the first issues of our publication. I wish I had a copy of the first issue to show, but instead I will have to go with Issue 10 from 1953 *(Fig. 1)*. Hopefully I'll be able to provide access to these older issues in the future.

At that time, vacuum tubes, cathode ray tubes, and transistors were coexisting. One of the articles in Issue 10 was "Gating and Switching Circuits Employing Transistors" *(Fig. 2)*. It was written by R.L. Trent, who worked for Bell Telephone Laboratories in Murray Hill, N.J. The labs are still around but are now known as Nokia Bell Labs. It's credited with the development of numerous technologies from the transistor to the C programming language. The article talked about the use of transistors for logic functions as well as a monostable multivibrator for pulse generation.



2. This is the first figure in the "Gating and Switching Circuits Employing Transistors" article from Vol. 1 Issue 10 of *Electronic Design*.

The Ideas for Design section was part of the magazine back then, but it didn't formally get the name until later. These were short articles by engineers on projects they wanted to share; they often used hardware and software in different ways than originally intended.

Transistors were more popular as time moved on. Still, even in the 1960s, vacuum tubes continued to play a critical role *(Figs. 3 and 4)*. The article from Volume 8 Issue 7 titled "Automatic System Finds Taped Data" uses a dual-triode 12AX7 vacuum tube with a high voltage gain along with relays and switches.

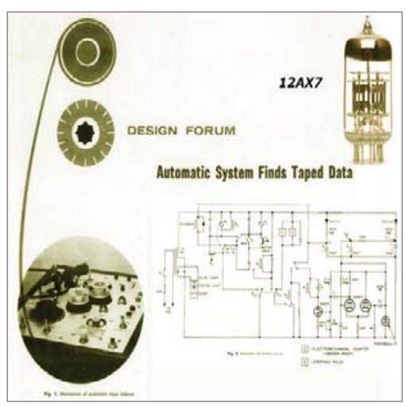
The 1960s had plenty of coverage on increased transistor integration. For example, the January 18 issue *(Fig. 5)* in 1966 asked about a "Computer on a Chip?" Though a novel concept back then, it's a far cry from the billions of transistors we have on a single chip these days. At that time, MOSFETs were just coming into being with only two companies selling MOS arrays. Motorola Semiconductor had announced a CMOS switching pair device.

I attended the Georgia Institute of Technology from 1973 to 1978 as a co-op electrical engineering student. I would regularly set up shop at Georgia Tech's library and grab all of the computer and electronics magazines, including *Electronic Design (Fig. 6)*, to read about the latest technology. I'd never have guessed that one day I would be the editor. I didn't join up with *Electronic Design* until 2000, but it was regular reading material for a budding electrical engineer and software programmer.

The May 24th issue in 1978 included the *Microcomputer Data Manual,* which was a listing of all microcomputers available

1. This is a scan of the cover of *Electronic Design* Vol. 1 Issue 10 from October 1953.

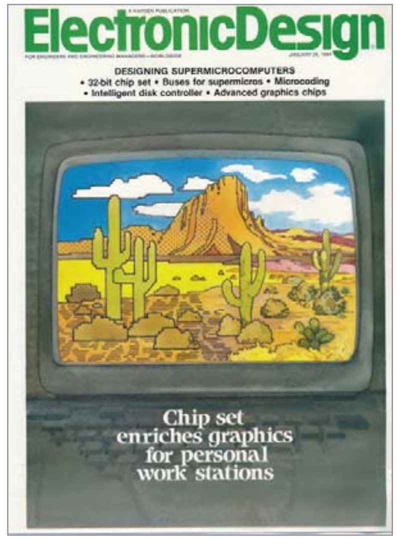
3. Shown is a scan of the cover of *Electronic Design* Vol. 8 Issue 7 in March 1960.



4. The magnetic tape controller employed vacuum tubes, including a dual-triode 12AX7.

5. Computers on a chip? Why not. This is the *Electronic Design* cover of Vol. 14 No. 2 in January 1966.

6. By 1973, microcomputers were emerging (*Electronic Design* Vol. 21, No. 11).



7. By the 1980s, 32-bit chipsets were becoming available and advanced graphics were coming into being.

at the time. At that point, it included platforms like the Motorola MC6802 and the Intel 8085; the microcomputers were on a single card. Amazing stuff at the time.

As we moved into the 1980s, I was spending some time at RCA's David Sarnoff Research Center reading *Electronic Design* and working on a home computer that never made it out the door. RCA was more focused on the RCA Selectavision VideoDisc Player, which used a diamond stylus versus the laser disks that I eventually bought.

Chip integration was starting to really ramp up and 32-bit chipsets were emerging *(Fig. 7)*. Mainframes and minicomputers still dominated high-end computing, but the personal computer was coming of age.

In the 1990s, I was doing freelance writing and software. I still read *Electronic Design*, though, to keep up with the latest engineering side of things. I was building PCs and writing about the process for various publications. It was an exciting time as microcontrollers and microprocessors were the main focus on the digital side. DSPs were challenging analog designs with their flexibility and FPGAs became more available as well.

I joined up with *Electronic Design* in 2000, taking over the Test and Measurement section from Joe Desposito, a future *ED* editor, who I worked with when I was Director of PC Labs at *PC Magazine* back in the 1980s. I eventually partnered with Ray Weiss, who had been working in the embedded side for a while, and we came up with the *Embedded in Electronic Design* section that ran for a number of years *(Fig. 8)*.

I also got to touch base with Bob Pease. whose Pease Porridge series has probably been the most popular column in the magazine's history. Ray and Bob have both passed away, but we still remember their contributions.

Most of you have followed us in 2010 and 2020 as we transitioned to an online publication that still includes a print component. Things are radically different in the industry as well as the publication side. We now do more videos, including our TechXchange Talks and Kit Close-Up series that are available on the website. And we recently started the Engineering Academy that's supported by all our brands in the Design & Engineering Group.

It's been a wild ride for me and hopefully you have enjoyed reading *Electronic Design*. We look forward to informing you in the days, weeks, and years to come about the latest machine-learning technology, the emergence of quantum computing, as well as breaking news on op amps, power supplies, and communications—because engineers and embedded developers need to know what's coming and how the parts are related. Join us for the next 70 years of *Electronic Design*.

8. *The Embedded in Electronic Design* section was written by Ray Weiss and Bill Wong.

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