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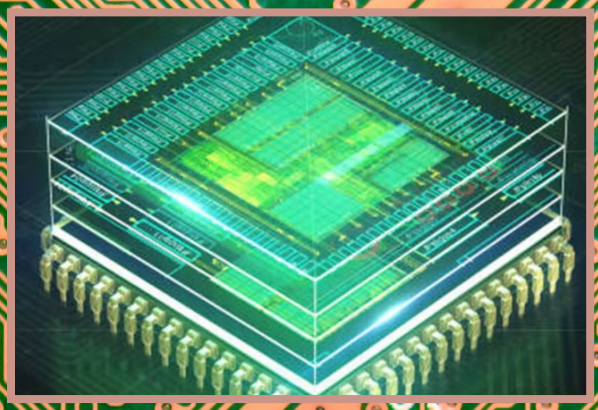
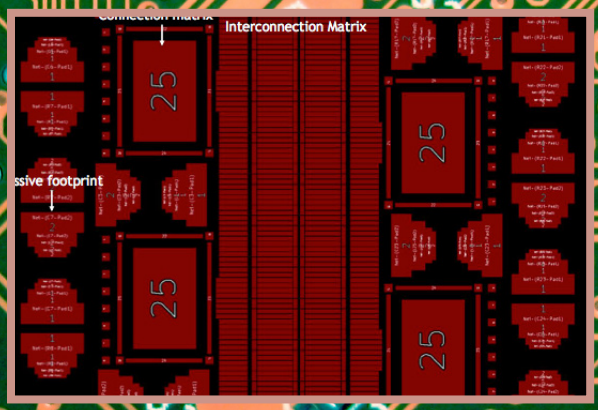
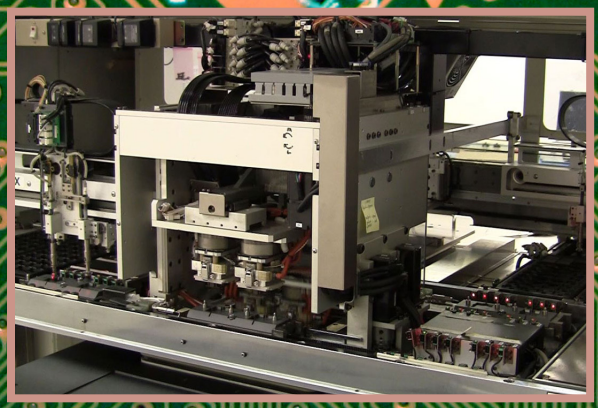
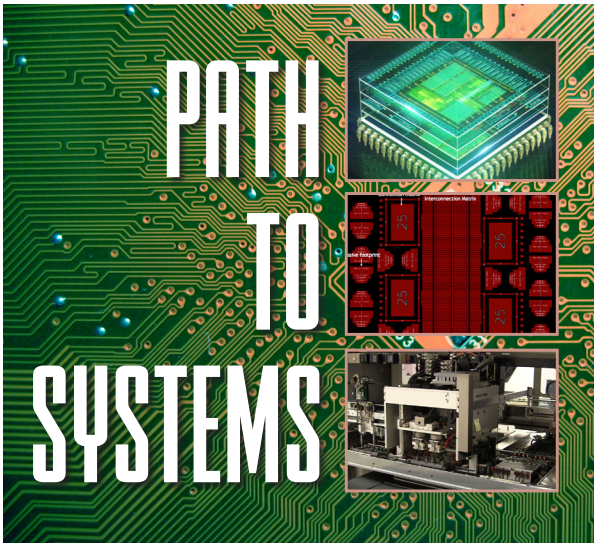
PATH TO SYSTEMS









INTRODUCTION

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This series explores challenges and solutions to the pace of integration and increased performance needed for tomorrow's embedded applications, and how system-in-package fits into it all.

Creating systems using the latest technology can be a challenge because it often takes advantage of the circuit board technology, high speed communication and advanced power management. Developers can become familiar with all these aspects and design a board and system or they can let someone else handle the heavy lifting by using a system-in-package (SiP).

A custom circuit board is still needed but the SiP provides a simplified interface making that board design easier. The board is often simpler with fewer layers because the SiP handles that complexity. This series examines issues, approaches and advantages of SiP technology for embedded developers.

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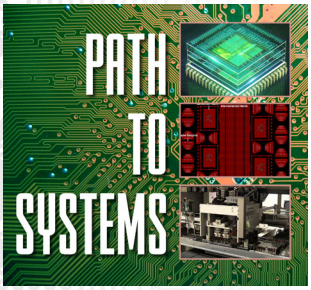
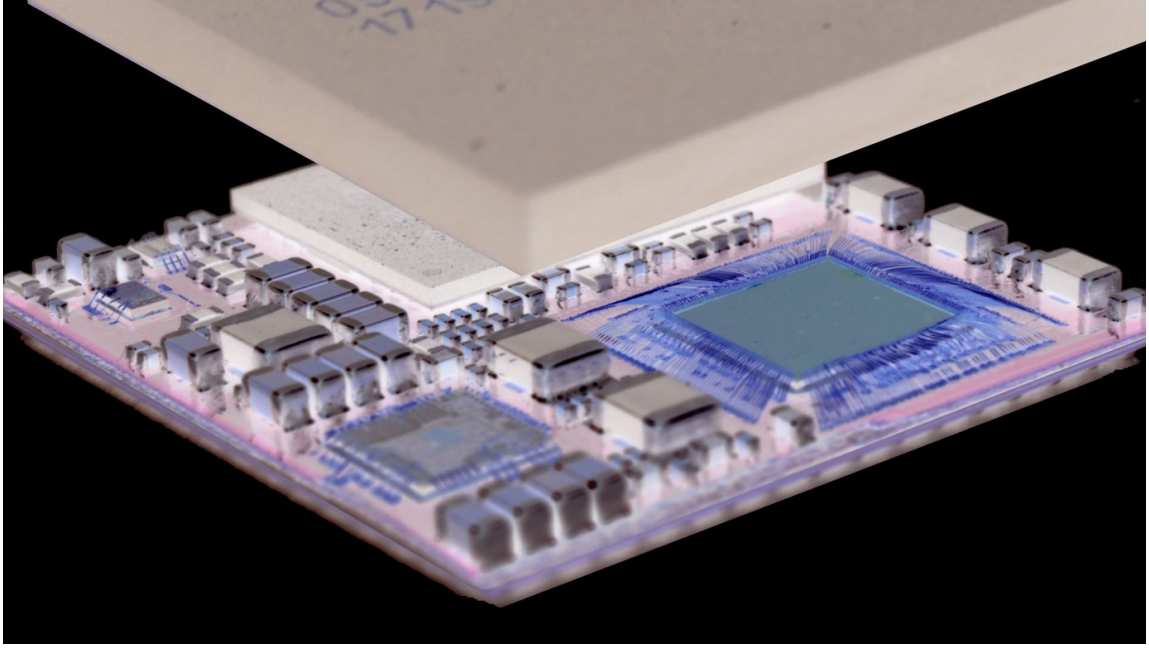




CHAPTER 1:

Opportunities and Challenges for the Next Generation of Semiconductor Integration

NEERAJ DANTU, Applications and Systems Engineer, MASOOD MURTUZA, Manager Package Engineering, and GENE FRANTZ, Chief Technology Officer, Octavo Systems

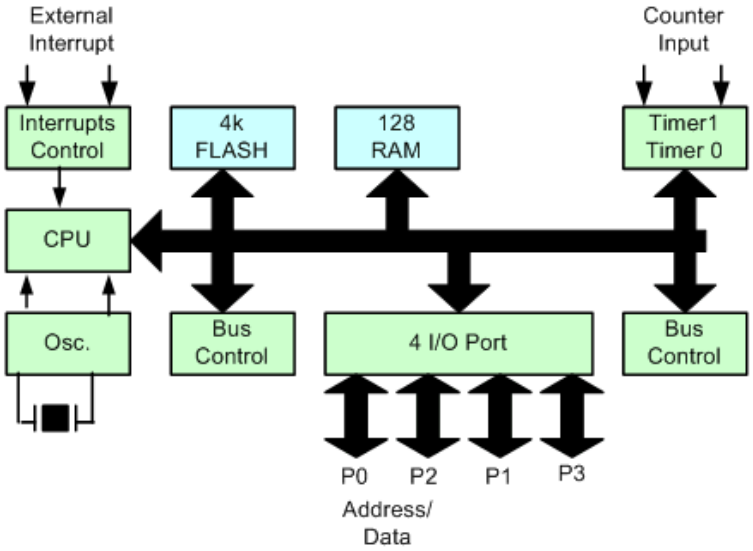
This article explores challenges and solutions to the pace of integration and increased performance needed for tomorrow's embedded applications, and how system-in-package fits into it all.

In the 70 years since the transistor was invented[1] and 60 years since the integrated circuit (IC) was invented,[2] we have taken the computer out of large rooms and put them into our pockets. It's been an amazing time where we have been able to impact every aspect of society with the innovations enabled by these two moments in history. Now we're in the process of taking the computer out of our pockets and putting it into our clothing, into our bodies, and into our imaginations.

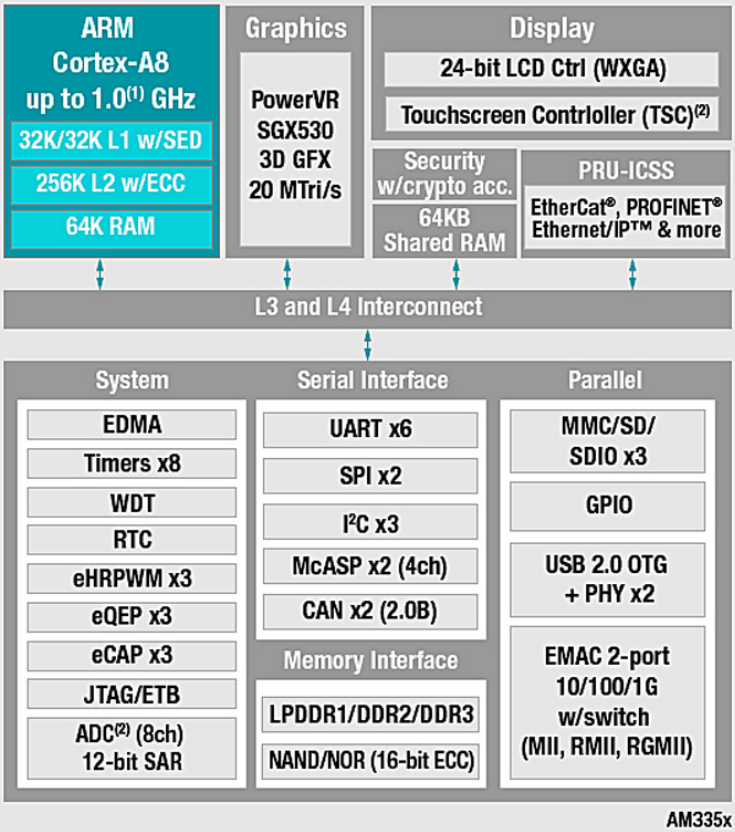
At the same time, we have completely removed the need for wires when communicating with other people throughout the world. Instead of having to fly halfway around the world for a face-to-face conversation, we can do that instantaneously with the push of a button. Now instead of suffering from "jetlag", we instead suffer from "netlag." It's amazing now to find ourselves on the threshold of computers talking and listening to us in the same ways we communicate with other people. Computers, of course, now talk to each other without human intervention. One can only guess what will be next.

These advances have created several challenges (or should we say opportunities) for electronic designs and therefore the semiconductor industry:

1. The focus of electronic design has moved from the component to the system.
2. The demand for performance has outstripped our capacity and capability.
3. |The demand for ultra-low power (e.g., long battery life) has become the new performance metric.
4. There's a continuous demand for faster product introduction cycles.
5. The innovation enabled by using technology no longer requires us to understand the



1. The first microcontroller was developed in 1971 by Texas Instruments, which had a block diagram similar to the one shown.



NOTES:
(1) >800MHz available on 15x15 package,13x13 supports up to 600MHz
(2) Use of TSC will limit available ADC channels
SED: Single error detection/parity

2. The block diagram represents Texas Instruments' AM335x ARM Cortex-A8 based microprocessor system-on-chip.

technology we're using.

In this article, we'll discuss the opportunities that are ahead for the semiconductor industry and how they will drive the next round of innovation. Then we'll propose an idea on how to enable the next round of innovation. Finally, we'll make some concluding remarks as to our view of that exciting future.

Opportunity

One of the interesting evolutions that has occurred in the semiconductor industry is the move in focus from the component to the system. That is, instead of just creating components, which can then be used to create systems, the focus is to now create a system design and then determine the optimal set of components needed to implement that system. This may seem to be a subtle change, but is a valuable insight to help us continue the integration path Dr. Gordon Moore envisioned in 1965.[3]

If we look back at early microprocessor and microcontroller devices, they had very little integrated memory and typically had no industry-standard peripherals *(Fig. 1)*. Compare that to contemporary microprocessors *(Fig. 2)*, which are complete systems with all (yes using the word "all" is a bit of an overstatement) of the memory and peripherals needed for a complete computer system.[4]

However, the pace of integration and increased performance in processor systems haven't exactly kept up with the demand for performance from the software and embedded-systems designers as they grow hungrier for more every year. The performance demands at the beginning of the microcomputer era to create new audio or video products were well within the state of the art of semiconductor technology.

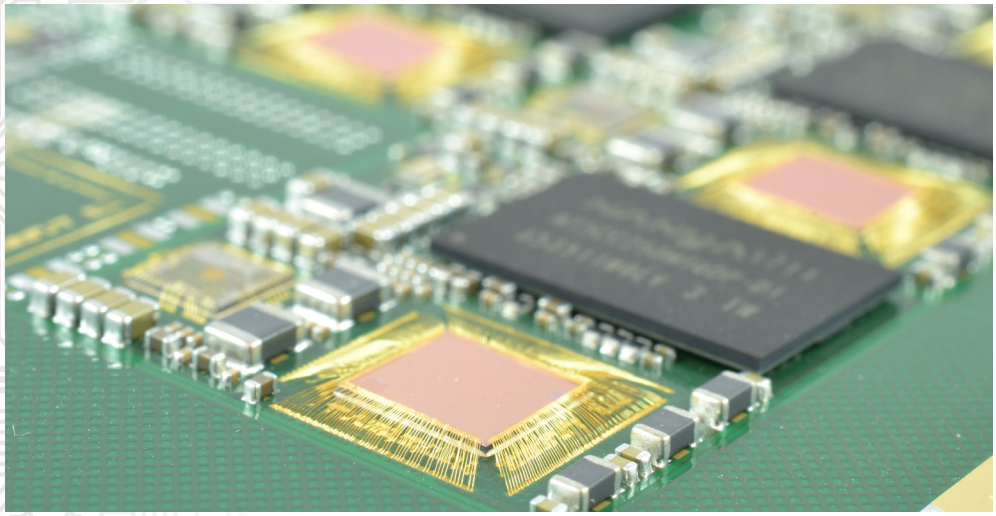
But we're now seeing opportunities in fields such as artificial intelligence (AI), machine learning, image understanding, and cloud computing stretching the limits of contemporary performance. Not only are these applications demanding exponentially more performance, they also want better integration of heterogeneous components such as FPGAs, GPUs, hardware accelerators, and processors for targeted applications. These demands are driving the performance requirements well beyond Moore's law.[5]

At the same time, we're seeing computer systems

shrinking, with the end goal being the concept of "smart dust".[6] To make this possible, the focus changes from driving performance to reducing power dissipation so as to, in the end, power these devices using as little energy as body heat.[7]

During the past 10 years, with the advent of smart devices, the electronics consumer industry has been in a constant state of competition that has driven semiconductor innovation to an unprecedented level. With the design services market segment forecasted to grow with a 7.24% CAGR between 2018 to 2023,[8] there has been a consistent demand for ways consumer electronics companies could reduce/eliminate the effort they have to invest to introduce new products by abstracting the menial tasks of system design.

Finally, the most interesting aspect of the opportunities ahead is the ability to use technology without the need to deeply understand it. Platforms like Arduino,[9] Raspberry Pi,[10] and BeagleBone[11] have made it possible for creative non-engineers to take advantage of the technology to innovate in their areas of passion. As this non-technical creative community begins to create new requirements for semiconductor devices, it's important to make sure those requirements are met in a meaningful way. The goal is to eliminate the increasingly higher barriers of entry that surround electronic design and manufacturing.



3. System-in-package integrates a diverse set of semiconductor components and passives into one package, miniaturizing the hardware while also simplifying design and manufacturing.

The System-in-Package Solution

The key to successfully create any solution is to first find the need to be realized and then find the technology that makes it possible. For the semiconductor industry, this solution needs to enable system designers and product developers to simplify product design while offering them what they need in terms of performance and features, essentially addressing each of the opportunities described earlier. We argue that the solution lies in system-in-package (SiP) *(Fig. 3)*.

There are fundamental requirements that the proposed SiP solution should satisfy, without which its usefulness is limited. The requirements are:

- The integration of diverse active semiconductor components and passive components into one system where the active components could be microprocessors, memories, specialized processing devices, analog circuits, power management, and sensors.
- The miniaturization of the resulting implementation and system footprint.
- Scalability allowing for low-volume opportunities to high-volume opportunities without a cost burden to either end of the scale.
- The ability to provide system-level hardware sub-modules of often-used subsystems. You might call this sub-system-in-package (SSiP).
- Quick, low-cost, prototyping and testing alternatives through flexibilities in design and interconnection methodologies.

4. SiP technology can solve a lot of existing electronics design and manufacturing issues, allowing for faster and easier development of electronics.

This is where the concept of "what is good in the world of semiconductors" complements the concept of "what is good in the world of systems." For example, the concept of fan-out wafer-level packaging (FO-WLP)[12,13,14] has been developed to allow the creation of semiconductor devices that shrink feature size of the IC beyond the physical constraints of a system design. The result is taking semiconductor die that are too small to use as a system-level component and putting them in larger packages, made up of low-cost materials, which are large enough to be used in system designs. The size of these larger packaged components enables them to be used on printed circuit boards (PCBs) to create custom systems.

This currently existing technology is one proposed solution that addresses some of the opportunities that we discussed. Though it's a step in the right direction, it doesn't satisfy all of the requirements of a system component. It partially addresses the complexity of design and manufacturing issues, but doesn't allow for miniaturization or higher level of integration, both of which can be addressed in a SiP solution. As we discuss more about the proposed SiP solution in our series, we will delve into how each of these requirements can be satisfied *(Fig. 4)*.

Finally, it's important to characterize the target areas and markets for SiP technology, as the semiconductor industry is also vastly diverse in its requirements. These requirements may sometimes include specialized functionalities and custom hardware that might not fit within the SiP framework. But, advances and improvements to the existing SiP architecture can help address most use cases. The goal of this article series will be to make a compelling value proposition for system-in-package technology while addressing how it beats the challenges presented by the opportunities introduced in this article.

Looking Ahead

Significant levels of semiconductor integration have already been achieved, and consumers are already benefiting from this through smaller and better performing smartphones and other electronic devices. As we develop new ways of 2.5D and 3D integration that reduce cost and increase manufacturability, it's important to look at the bigger picture in terms of needs and technologies and to connect them in a meaningful way.

The bigger picture for electronic system design would be to have a design flow that's both systems-centric (SiP and PCB) and component-centric (SoC). The system-centric portion of the design flow requires the ability to integrate various semiconductor devices that are each manufactured with its own optimized process, along with hundreds of pas-

sive devices.

Finally, the overall design flow from IC creation to system creation needs to economically scale up or down (both volume and cost) without burdening either end of the design flow. We will see in future articles in the series how system-in-package technology provides a perfect sweet spot to solve many design and manufacturing problems while addressing new opportunities and requirements.

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GENE FRANTZ is one of the founders and the visionary behind Octavo Systems. He currently serves as Chief Technology Officer. He is also a Professor in the Practice at Rice University in the Electrical and Computer Engineering Department. Previously, Gene was the Principal Technology Fellow at Texas Instruments where he built a career finding new opportunities and building new businesses to leverage TI's DSP technology. Through this work he became highly regarded in the industry as a leader in DSP technology. Gene holds 48 patents, has written over 100 papers/articles and presents at conferences around the globe. He has a BSEE from the University of Central Florida, a MSEE from Southern Methodist University, and a MBA from Texas Tech University. He is also a Fellow of the IEEE.

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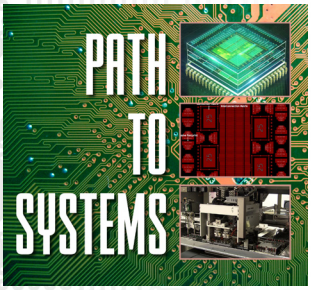
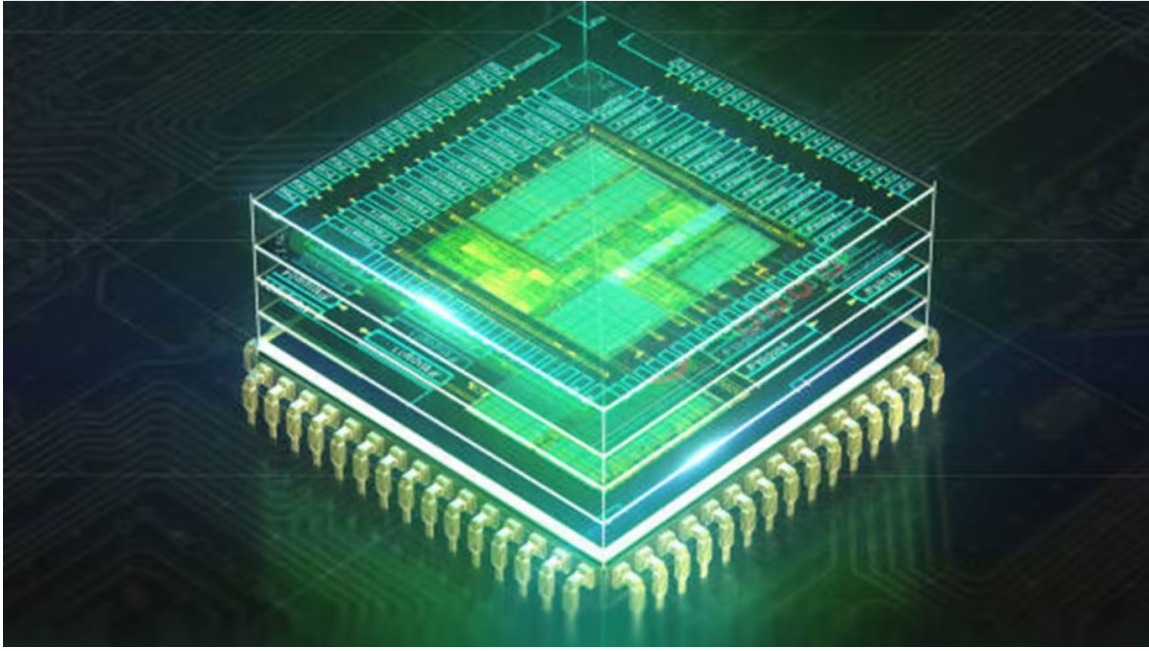




CHAPTER 2:

Why a SiP?

NEERAJ DANTU, Applications and Systems Engineer, MASOOD MURTUZA, Manager Package Engineering, and GENE FRANTZ, Chief Technology Officer, Octavo Systems

This article presents key advantages and challenges ahead for system-in-package (SiP) technology in the grand scheme of semiconductor integration and specifically, embedded systems.

Integration has been the driving function of the semiconductor industry since the transistor was invented. An underlying assumption is that putting more transistors on a piece of silicon was the answer—now, "what was your question?" Many years ago, we used terms like SSI, MSI, and LSI (small-scale integration, medium-scale integration and large-scale integration, respectively). These terms represented a progression of technology and processes for transistor integration.

This progression did not, however, describe the functional integration that came as a result. Consequently, descriptions such as ASIC and SoC (application-specific integrated circuit and system-on-chip) were termed. All of these terms helped to keep in perspective the drive toward more system integration. For example, *Figure 1* shows the difference in functionalities of two DSP SoCs from Texas Instruments (TI) about 10 years apart from each other.

Along with the increased performance at a much smaller technology node, the C6A8168 processor integrates custom cores for graphics processing, video display, and a Cortex A8 ARM core. Along with these cores, the newer processor also integrates several subsystems for connectivity, timing, data storage, and peripherals. The comparison shows how far the industry has come.

As we move forward in this area with integration both at a transistor level and a functional level, new advances in package and circuit board technology have given rise to terms like MCM, SOM, and SiP (multichip module, system-on-module, and system-in-package).

The topic of this paper is this latest descriptor of integration. We will use the term system-in-package (SiP), as it best describes what it is—the next revolution in circuit integration. Let's start with an "under the hood" view of a SiP device.

Under the Hood

The general concept behind the development of a SiP is the unspoken result of pursuing

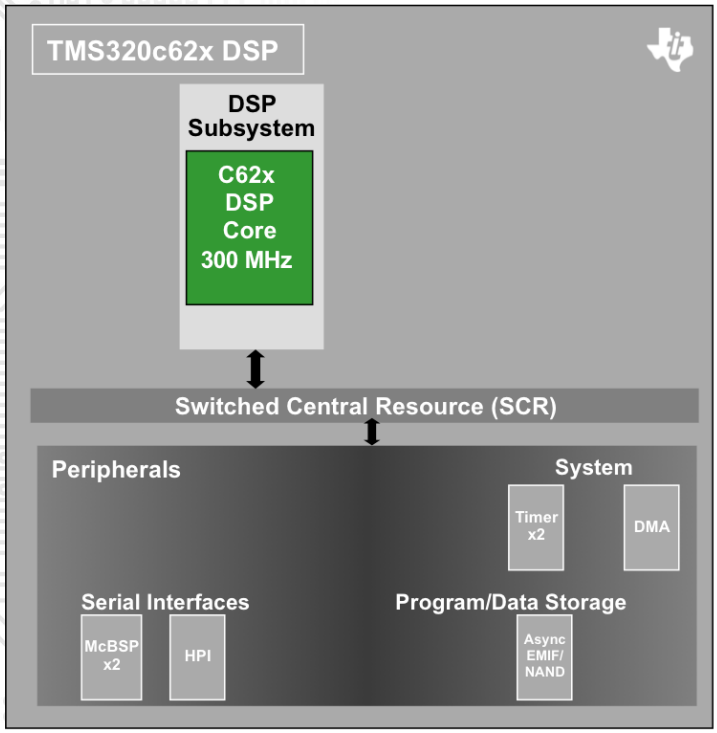
Moore's Law. That is, to keep driving integration, we needed to focus the silicon process development on each of the different kinds of circuits. For example, as the microprocessor needed a different process than that of a memory device, analog circuit, a power-management device, or a sensor device, the obvious answer was to integrate at the system level. This can be termed as the origin for SiP technology.

Despite the relative newness of the term, SiPs have been around for a long time in one form or another. Discretionary wiring[1], MCMs, and Hybrid Integrated Circuits (HIC)[2] have been done in the 1970s. Early adaption of the current form of SiP technology took place in the late '90s with Intel's Pentium Pro[3] integrating processor and cache on separate dies. In contrast to the early days, SiP has transformed into a niche solution with applications in wireless communication and sensors.

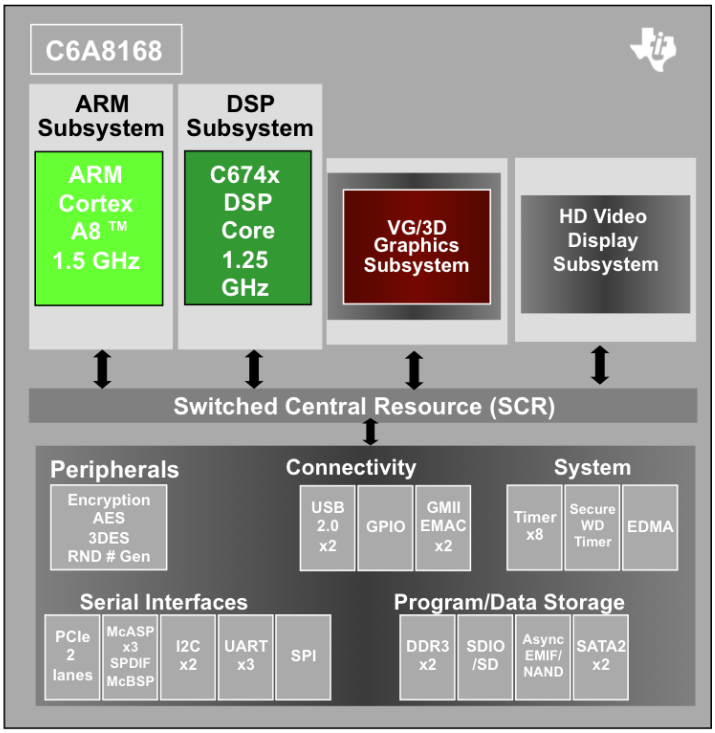
The SiP is a semiconductor device in which systems are integrated. *Figure 2* shows an example of a SiP, the OSD335x-SM. The components of a SiP include die; in this example, it's wire-bonded to a substrate. There can be more than one die oftentimes that's heterogeneous, like power-management ICs, analog PHYs, and memories. The SiP can also integrate packaged parts and other SiP modules. Furthermore, the integration techniques also might vary for example stacked die, flip-chip, through silicon via (TSV), or 3D SiC (3D stacked IC).

Why Use a SiP?

The last few years have not been great for Moore's Law. Moving to the next processing node now requires billions of dollars in investment. As a result, the industry is looking at

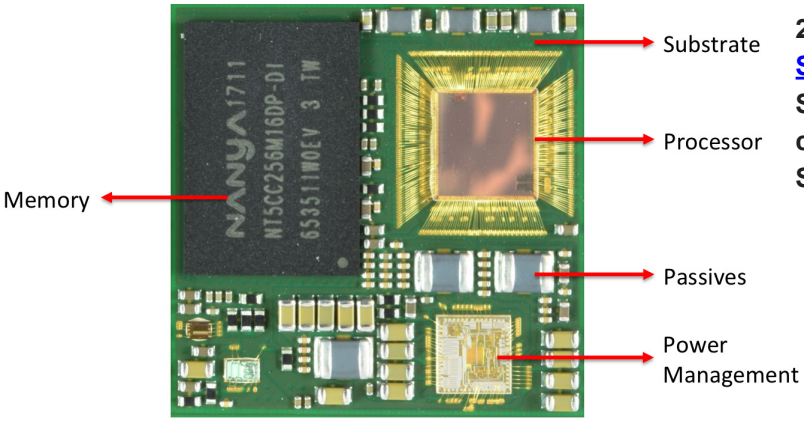


0.18um 1.8V CMOS process
200MHz, 352-pin FCBGA (Flip-Chip)



40-nm 1.0V CMOS Technology
1500 MHz, 1031-Pin BGA Package

1. Comparing the integration of two processors, 10 years apart.

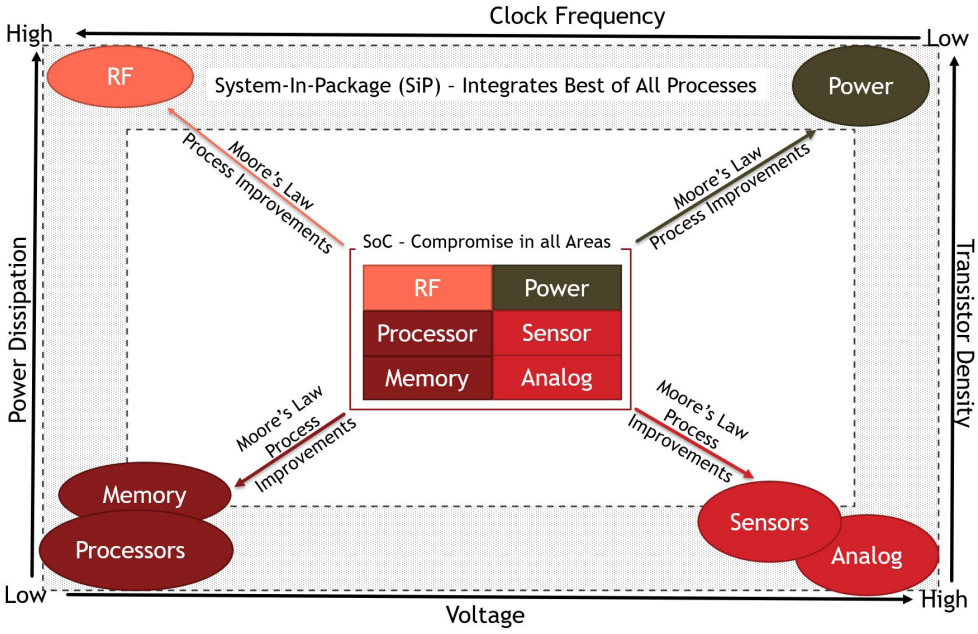


2. Shown is Octavo Systems' OSD335x-SM, revealing the components of a SiP.

optimizing processes and producing efficient semiconductor products while searching for better paths of integration.

The industry is also facing long design cycles. Embedded systems of present day have complex functionalities implemented on high-speed data lanes and protocol specific PHYs. A lot of high-speed interfaces like Ethernet use analog signaling. Many products now also have analog signal conditioning and processing blocks that don't fit into the SoC. MEMs sensors are a good example. Memory is another non-logic component that's now being integrated into most IoT/embedded devices. All of this makes for complex embedded systems, but with striking commonalities.

Even as keeping up with Moore's Law has been difficult for logic, process scaling has been harder on analog and mixed-signal design. As a result, we no longer have just one IC manufacturing process. As seen in *Figure 3*, we have created processes to be optimized for specific needs. There's an optimized process for high-performance microprocessors,



3. Moore's Law has caused semiconductor processes to progress in multiple directions.

memories, high-performance audio power management, and RF circuits.

Due to the components with high-speed interfaces that need to be discretely integrated, the end product is often complex, driving design and manufacturing costs higher. Along with adding design complexity and time to market, this sets fundamental limitations on the new and innovative products with a high barrier of entry for new companies in systems design.

SiP technology addresses all of these problems. Some of the advantages are described below:

Simplification: System designers can integrate SiP components as abstract building blocks that allow them to design faster, enabling a much smaller design cycle. Double-data-rate (DDR) interface design is a prime example for this advantage. DDR layout along with power design and distribution are among the common places that demands a re-spin/redesign. The complexity in the current design environment is resulting in design cycles of 12-24 months.

Depending on what a SiP integrates, the design cycle can be cut in half, often with no need for lots of hardware design experience in the team. Moreover, the system-based approach to integration allows for simplified mill of materials (BOM), eliminating debugging for trivial but important interfaces like DDR. This results in getting to a finished product much faster than otherwise.

Manufacturability and yield: Though manufacturability is a constantly evolving concept when it comes to the semiconductor industry, the less complex the design, i.e. lower-speed interfaces, higher tolerances, and relaxed design rules, the higher the manufacturability of the product. This is an area where SiP expertise comes in very handy. Akin to cooking with the right recipe, given the right approach to SiP design, with substrate selection, mold compound selection, and thermo-mechanical modeling, yield and manufacturability can be extremely positive.

Miniaturization: Another highly valued aspect of semiconductors, especially in this smart gadget IoT era, is minimizing the size of the system. On an average system where only 10% of the components are ICs,[4] miniaturization is a difficult process and sometimes isn't possible without compromise or a higher-cost system. SiP design rules allow for not only much tighter die integration, but also closer passive integration. This reduces the overall size of the system by as much as 65%.[5] So, in a lot of ways, SiP can be viewed as complementary to Moore's Law with a system-level approach to integration.

Cost reduction: Miniaturization is often associated with increased cost. That actually might be not true in the case of system-in-package due to the economics of scale in the semiconductor industry. That's because the cost of manufacturing with a number of integrated components in high volumes reduces the cost for all customers. Cost reduction doesn't stop there. Assembly cost, discrete BOM overhead, and PCB design cost can see big reductions depending on the system. An analysis for the OSD335x SiPs shows up to 20% cost savings.

Reliability: Compared to a PCB system using discrete components (ICs, passive devices), a SiP is equal or better in terms of failure probability. SiPs use the same qualified set of silicon and passive devices as their packaged component version do, thus the intrinsic reliability of these individual components will be the same. The potential improvement comes by way of solder joint reliability. In the case of molded SIPs, such as OSD3358-BSM, the solder joints of constituent packaged IC devices and passive devices are fully

encapsulated in a molding compound. Molding compound protects the solder joints from stresses.

The most common loads that cause failure in soldered components are due to board flexure and bending, shock and vibration, and temperature cycles. In each of these cases, stress is significantly reduced because of the protective molding compound surrounding the components. In addition, SIPs are put through the same intensive qualification tests as semiconductor components; these tests are generally more stringent than commonly used PCB qualification tests. *Figure 4* shows the results of a typical qualification test applied to OSD3358-BSM.

Tests	SS/fail
MSL3	160/0
-40/125 Temp Cycle, 200 cyc	37/0
-55/125 Thermal Shock, 200 cyc	40/0
Unbiased HAST 110C/85% RH, 264 hrs	40/0
HTSL 150C storage, 500 hrs	40/0

4. The results of a typical qualification test applied to OSD3358-BSM.

Next-generation requirements: Continuing the pursuit of monolithic SoC development poses roadblocks on multiple fronts. Design verification and manufacturability become harder as the size of the die increases simply because of the greater chance of impurity/manufacturing faults on a larger die.

Another key issue is intellectual property and the legal issues that arise with design reuse. As new advances such as more efficient communication protocols and modulation techniques are invented, trying to design monolithic dies that keep up is neither economic nor fast. In this context, SiP is a great alternative. On the other side of the spectrum, SiP also eliminates/significantly reduces limitations of current PCB manufacturing technology. SiP reduces the system form factor, significantly increases the chip-to-chip bandwidth, and reduces the power consumption of the system via short and thin electrical traces.

But What Are the Issues?

But disadvantages also need to be addressed: lack of flexibility; inability to customize, and the need to be high volume to be viable in the IC manufacturing process.

Lack of Flexibility

Since SiPs are systems rather than components, they are by their very nature application-dependent and tend to be more application-specific than SoCs. SoCs are designed to be components used in many systems and therefore tend to not be customer-specific, but designed as standard components. Thus, the economies of scale found in high-volume SoCs are lost in the world of SiPs.

Inability to Customize

Systems built with discrete components offer a great deal of flexibility in their design and development; small changes in design are often accommodated without extensive redesign. Such changes aren't practical in SiPs because major components like the substrate or interconnecting systems require major revisions involving a redesign of the substrate. A redesign not only will add cost to the project, but also create a schedule delay of several months. Ideally, one would like to have a SiP with the flexibility of a discrete component system, yet still have the economies of scale of an SoC.

Need for High Volume

The semiconductor industry has been successful due to its drive to lower the cost of

manufacturing. A key component of this drive is high-volume manufacturing methods. That creates a significant issue to a system design which only needs thousands per month rather than millions per month. It's obvious that the need for high volume is key to the success of any IC technology, including SiP technology. The question is how to provide low-volume system components while not altering the high-volume manufacturing flow.

Conclusion

In the previous article of this series, we described the opportunities and challenges ahead for the semiconductor industry. The focus has shifted from component view to system view of design, and the industry demands higher performance with a lower complexity and higher manufacturability. However, the most important aspects of the innovation that has always driven electronics are miniaturization and low barrier for entry. SiP makes both of these goals possible. With the next generation of requirements such as terabit networking, 5G wireless, and 8K video posing tough challenges, having the advantages that SiP brings to the table becomes very important for success. SiP essentially extends the life of Moore's Law. By how much? That's yet to be determined.

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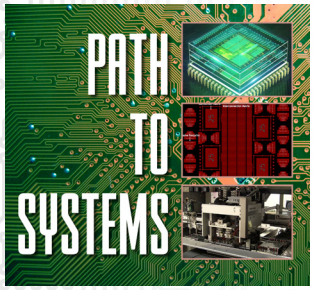
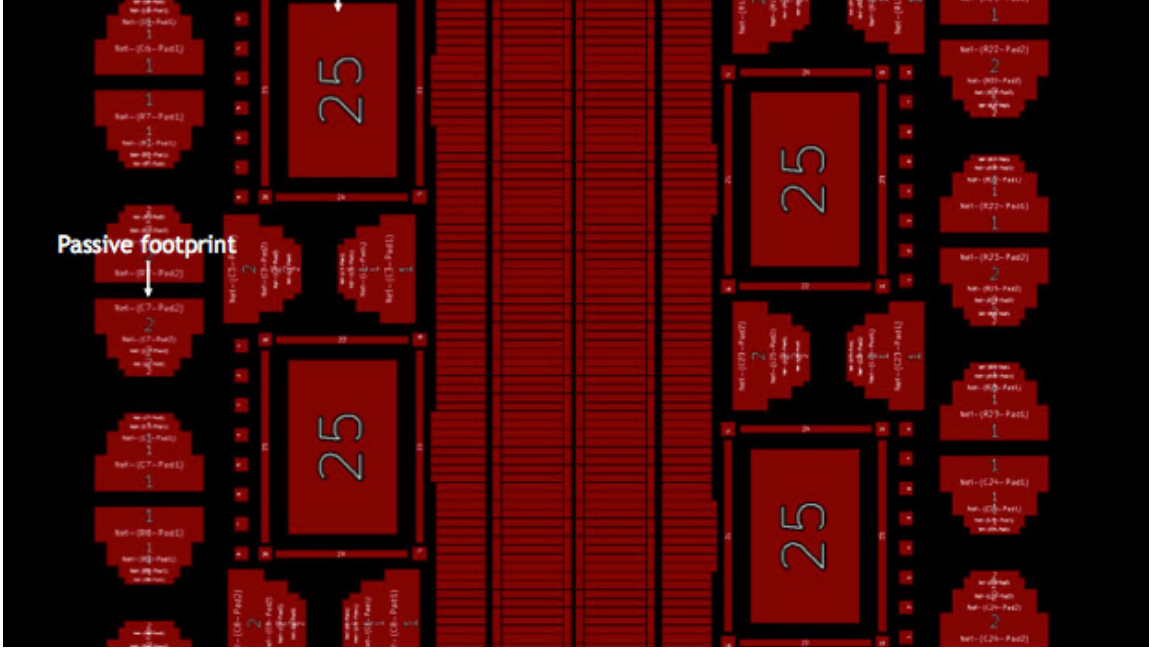




CHAPTER 3:

SiP—Leveraging Mass Production on a Small Scale

NEERAJ DANTU, Applications and Systems Engineer, MASOOD MURTUZA, Manager Package Engineering, and GENE FRANTZ, Chief Technology Officer, Octavo Systems

Part 3 of the series provides insights into how the design and manufacturing process of system-in-package technology will extend Moore's vision, creating Moore's law 2.0.

System-in-package (SiP) technology is at the beginning of its revolution. Some see the SiP in the same way as a system on chip (SoC)—as an IC component with no simple path to further customization. Also, the economics of scale relegate the device to a high-volume manufacturing process in addition to the long design cycle time. Which isn't an issue if you, as a systems engineer, need millions of devices per year. However, new innovators and entrepreneurs are left out.

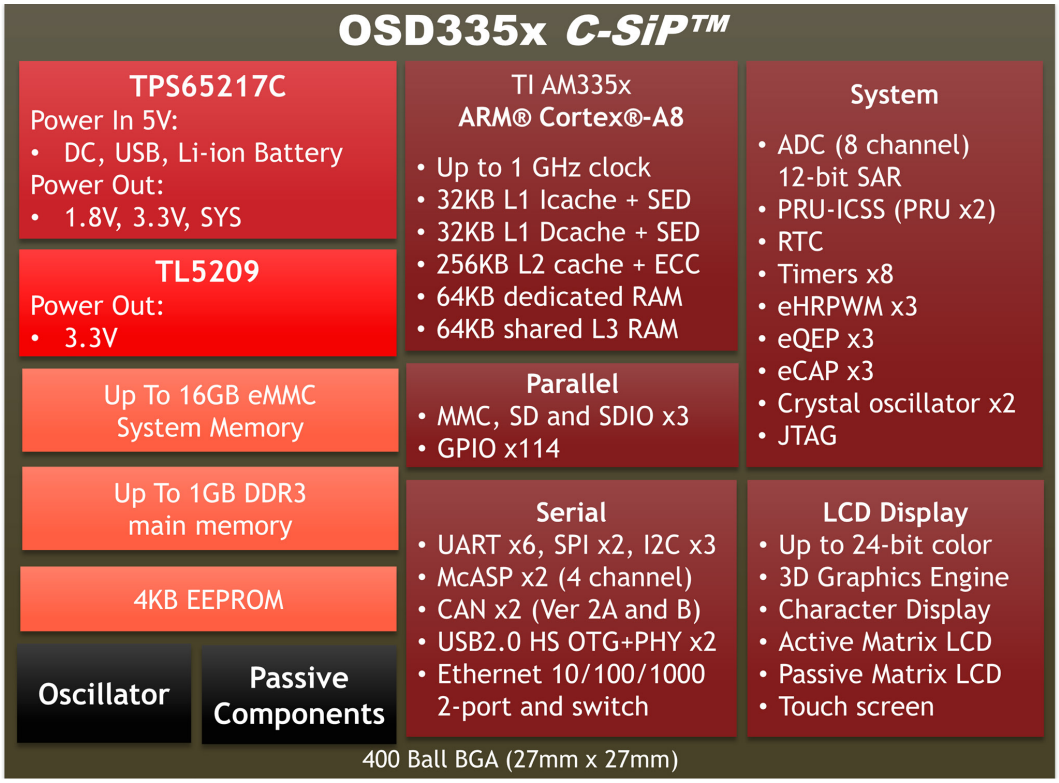
So, is there a way that systems designers can take advantage of the SiP technology to further integrate without the need for a high-volume application? Apparently so, as capabilities loom on the horizon that allow for more integration with less volume using SiP.

SiP Design and Manufacture Today

There are compelling reasons for a SiP to be the solution to systems integration. We detailed several, including simplification, miniaturization, cost reduction, and reliability in Part 2 of this series. In fact, the same requirements that drove the SoC development are likely to drive the SiP roadmap as well. However, SiP capability will be able to bypass many of the limitations presented by SoC without sacrificing much of the system integration achievable through an SoC.

For example, *Figure 1* shows a block diagram of a SiP[1] with a variety of functional blocks. This example is an embedded system that has different IP blocks, with several different semiconductor process nodes. In addition, functional blocks make integration of the SiP into the system easy.

Some of these subsystems, such as the parallel and serial interfaces, are integrated into the SoC, while other subsystems like the DDR memory and power-management IC are



1. OSD335x C-SiP system-in-package block diagram.

independent components integrated into the SiP. This allows the SiP to be a functional system-level block rather than a design challenge, which has become the case with current SoCs.

The *Figure 1* block diagram definition is the result of the initial stages of the SiP's design. An important decision to make here is which components go in the SiP and which do not. Design complexity, functional importance, and package/die size are some of the factors that influence this decision.

Once the device is well-defined in the block diagram stage, computer-aided design (CAD) tools are used to actualize the SiP device. SiP and IC manufacturers often have specific design rules that may not be common or industry standard. So, it's important to work with the manufacturer during the design stage. When the design is complete, the release package is sent to the manufacturer.

An example process flow of SiP manufacturing process is shown in *Figure 2*. Ideally, all active components in the SiP are in die form, but they can also be packaged parts. The manufacturing process might vary based on the integration techniques and the target size/specification to be achieved. The process described in Figure 2 illustrates a simple surface-mount device (SMD) attach process for surface-mount components and wire bonding for die integration.

The SMD components of the SiP are attached to a substrate. This substrate is a printed circuit board built with micron-level design rules that allow for a miniaturized circuit board, tight integration, and better bandwidth and power performance. After the assembly goes through a reflow, it's pre-baked for die attach.

After the die attach has cured, the dies are then attached and wire bonding is performed. This assembly is baked yet again and molded with a preselected mold compound that's suit-

able for the system. Once the mold compound is set, the package goes through solder-ball attach and dry bake. Several quality checkpoints are embedded in the process to enable process specific fault detection.

Overcoming the Challenges of the Current Design and Manufacturing Process

As described in Part 2, this new SiP technology presents new challenges. Some challenges, such as lack of flexibility and inability to customize, are technical. Other challenges, like the need to be high volume to be viable in the IC manufacturing process, are economic. While there's a desire to integrate more functional blocks into the system, doing so compromises system flexibility. The greater the number of functional blocks, the less flexible the SiP becomes, which means lower volume, application specific and higher cost, making integration nonviable.

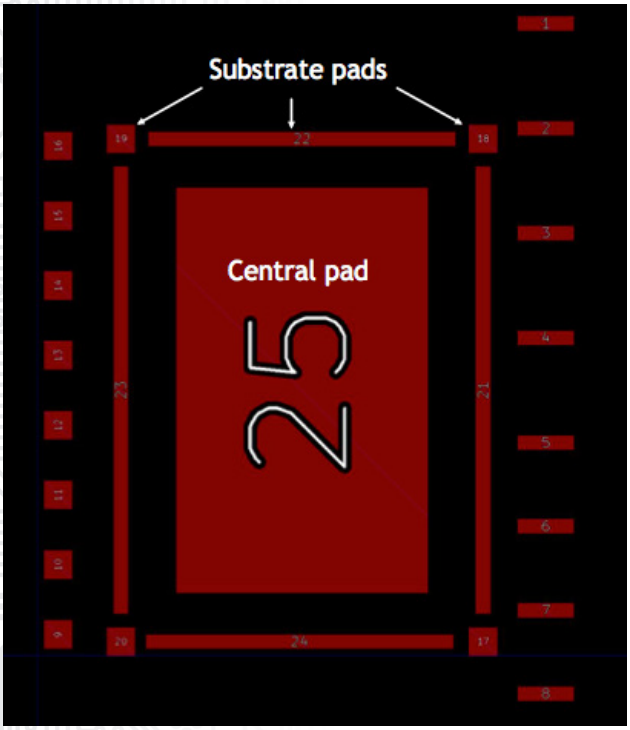
Although not as complex as with an SoC design, making changes to a system component in the SiP still provides a significant hurdle. Moreover, users desire customizability to have better control of their own design as well as make choices of the functionality of the SiP. All of this, while possible, has cost and time burdens associated with it. The good news is, there are solutions that can overcome these challenges with minimum effort spent in time and money.

2. High-level manufacturing flow of a SiP.

Semi-Custom SIP Devices

Semiconductor manufacturers have developed many solutions over the years that enable higher integration and better manufacturability for SiPs. Flip-chip, 3D die stacking, and package on package (PoP) are examples, essentially adding the z-axis to the integration environment. The flexibility of bond-wire placement and specialized mechanical tools have played an important part in these solutions.

These solutions, however, are either highly integrated and don't match a lot of system requirements or remain too risky to be integrated into the production flow to be considered as effective enablersT-he only way to maintain the scalability of the manufacturing process while delivering more integration and functionality is through customizability, which is transparent to the manufacturing process. By making it transparent, the advances in manufacturing processes and adapting the SiP design process to lend itself to



3. Customizable die footprint.

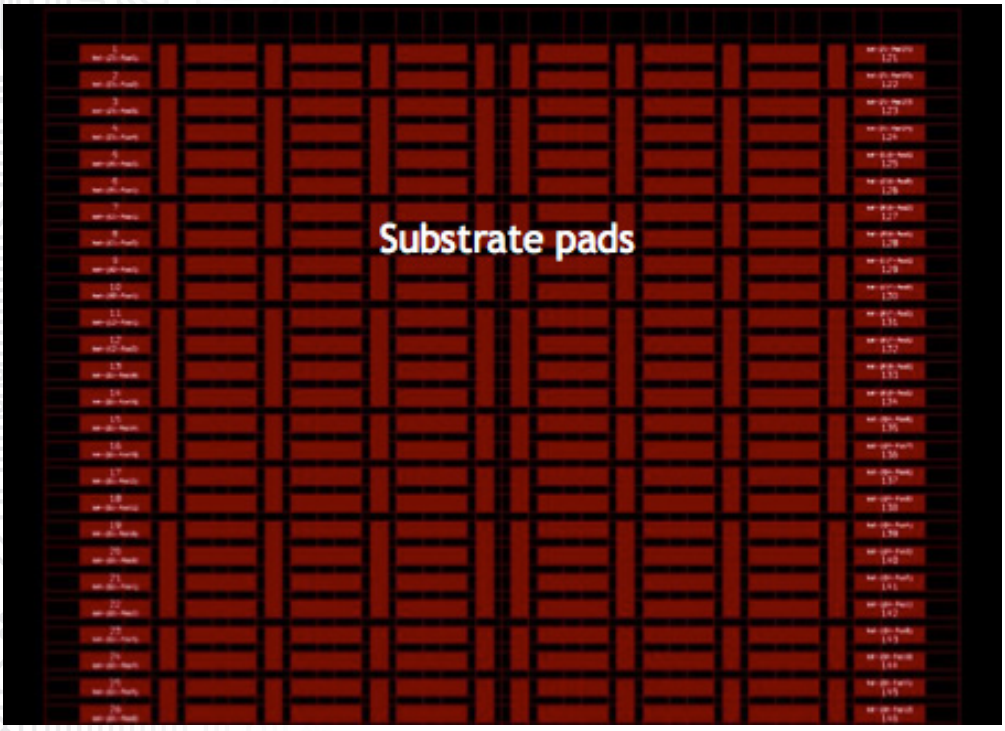
customization can be an ideal solution.

For example, *Figure 3* shows a version of a customizable part (connection matrix) of a substrate.[2] The central pad (25) is where a die would attach to the substrate and bond wires would be used to connect the die pads to appropriate substrate pads as needed. The central pad can accommodate different-sized dies. This layout can be used to make a configurable SiP by programming the pick-and-place machine and the wire-bonding machine appropriately.

This is only one, rather simple, example of how configurable design choices can lead to customizable SiPs. Another example, or rather an extension to this die-attach configuration, is a configurable substrate layout that allows for connecting signals between multiple dies.

Figure 4 shows a customizable interconnection matrix that can be used to create a configurable SiP system. Signals from the die components in Figure 3 as well as other passive/active components can be connected to a connection matrix shown in Figure 4 by signal traces on the substrate. Then they're electrically connected to other signals with bond wires on the connection matrix. In a sense, this makes the connection matrix, when combined with the die-attach pads, a miniature breadboard.

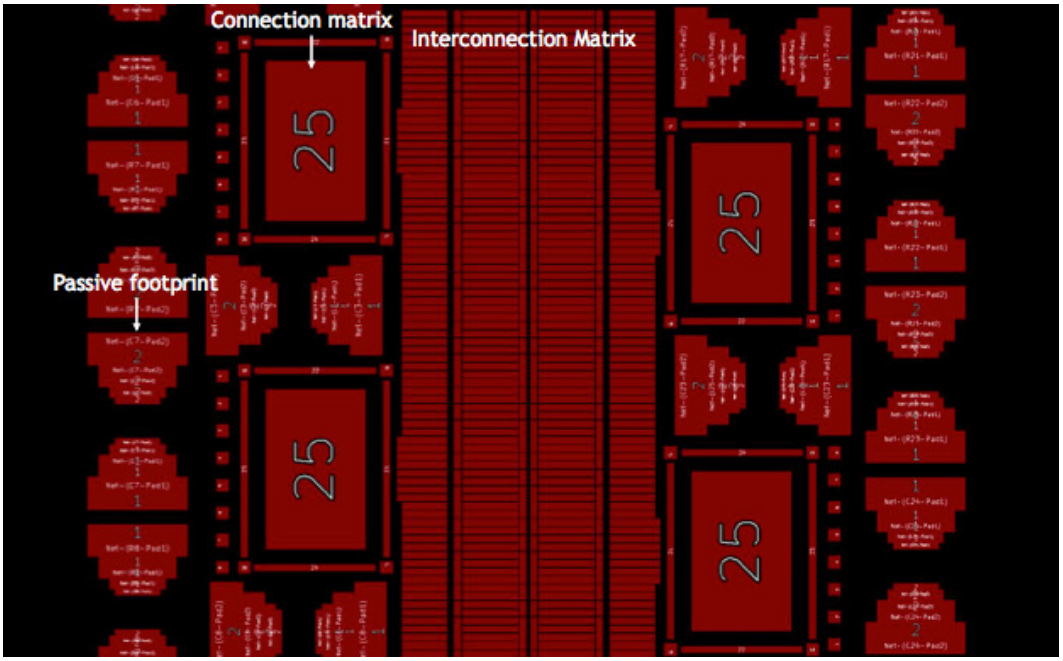
This combination of the central connection matrix and the interconnection matrix has several applications; for example, signal conditioning. The interconnection matrix with a number of connection matrices and passive components connecting into the interconnection matrix placed around it on the substrate *(Fig. 5)* can allow for a large number of op-amp-based signal-conditioning systems.



4. Customizable interconnection matrix.

As mentioned, this is one of many ways to create a customizable substrate. The takeaway here is that customizability is a design methodology that increases flexibility and enables low-volume innovators while providing access to the latest and greatest integration methods.

So, the next question is, "How can the design of a SiP be done to build configurable SiPs?" Based on the application, there are many answers to this question. While the above example is suited for signal conditioning, similar design method-



5. Customizable substrate design.

ology can be implemented for other areas of computing and embedded design.

What Are the Issues?

The configurable SiP creates a new set of challenges. For example, new software tools that enable this design methodology are necessary. Challenges on the manufacturing side include programming the capability in the pick-and-place/bond-wiring machines such that a production line delivers different customizations of a configurable SiP while the line remains the same.

Conclusion

The customizable SiP solution, as it progresses and morphs into new SiP designs, represents a new paradigm in semiconductor manufacturing. The end goal of this technology is to provide a SiP to the system designer who has a need for low-volume run rates with the cost associated with a high-volume run rate.

Is there a system that allows individuals to input their designs while delivering SiP'ed packages without the drawbacks of the low-volume manufacturing cost as well as complex design effort? Such a design methodology reduces time and money spent on the design while providing a path to integration beyond standard components on a PCB. We believe the answer is yes.

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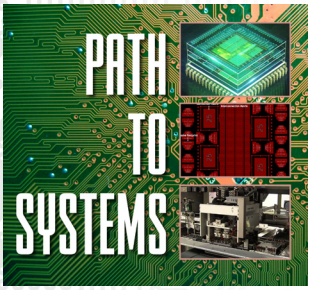
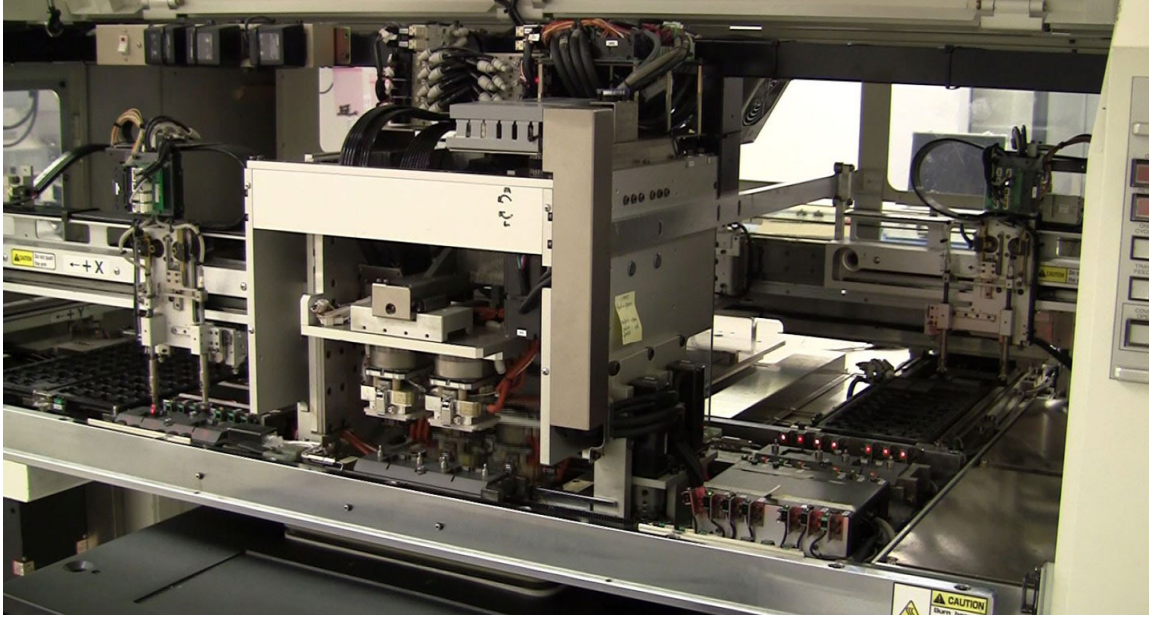




CHAPTER 4:

A SiP of Reliable Advantage—Systems Under Test

NEERAJ DANTU, Applications and Systems Engineer, MASOOD MURTUZA, Manager Package Engineering, and GENE FRANTZ, Chief Technology Officer, Octavo Systems

Part 4 presents how the methodologies of testing and characterization of system-in-package technology enables higher-quality, more-reliable products.

In parts 1, 2, and 3 of the series, we talked about how the fundamental shift of focus toward systems makes system-in-package (SiP) an essential step forward in electronic design. Through SiP, a complete system can be packaged into a standard ball-grid-array (BGA) package the size of a nickel, such as the Octavo Systems' OSD335x in *Figure 1*.

We also discussed the advantages SiP brings to the design and manufacturing of semiconductors and how they can be used to tip the economy of scale toward low-volume opportunities. In this article, we will examine testing methodologies for SiP and how it simplifies testing and characterization of devices. This gives customers of SiP a more-reliable, higher-quality product to put into an end system.

There are several advantages to manufacturing a product or device using a system component (i.e., a SiP) rather than using discrete components. Here, we will focus on the advantages found in the device testing process and methodology. SiP components are uniquely suited to take advantage of the semiconductor manufacturing processes while simultaneously utilizing system-level testing normally reserved for the end product or device.

While Moore's Law has driven ever-increasing transistor densities and device complexity, semiconductor testing has kept pace by focusing on extremely high-volume manufacturing. This necessitates moving quickly through the manufacturing learning curve to reduce the cost of a product as quickly as possible. As a result, the semiconductor test methodology and equipment used during manufacturing have not only made semiconductor component testing extremely cost-effective, but have also resulted in higher quality and more reliable devices.[1]

With this as a backdrop, let's first explore some basic testing concepts of both

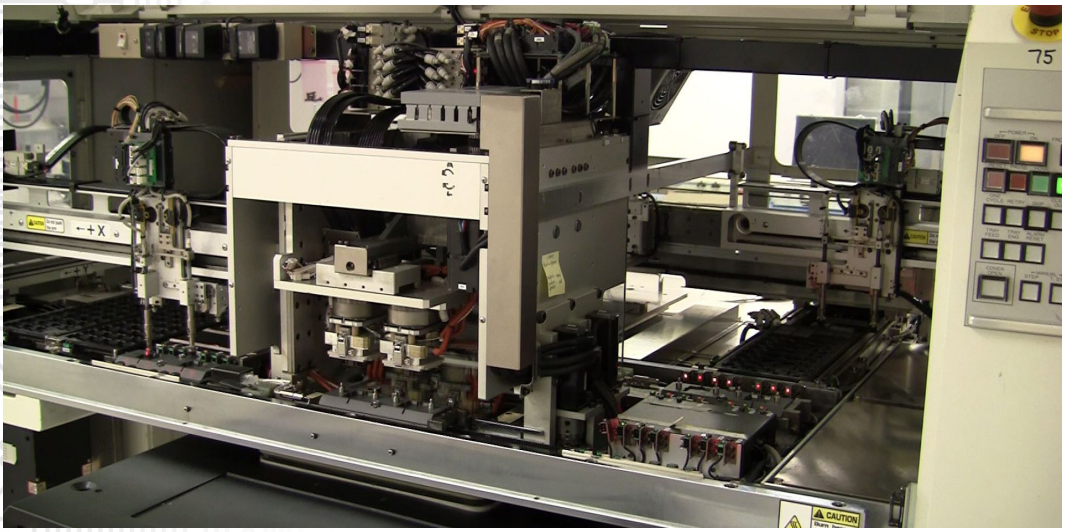
1. The OSD335x is an example of a complete system fitting into a tiny BGA package.

semiconductor devices and systems. That follows with a look at a SiP as a device under test (DUT) and application of these concepts.

Testing Basics

Generally, the further down the manufacturing process an unusable device travels, the more money is lost. It's therefore important to test as much as possible early in the manufacturing process. In addition, as devices become more differentiated, they become more expensive to test as the volume of the devices drops and the process becomes more manual.

For example, the component tests for a generic CPU are much more automated than system-level tests on specialized equipment using that CPU. As such, each subsequent round of testing should focus on aspects that weren't tested or couldn't be tested earlier in the process. This applies to both component-level testing of semiconductor devices as well as system-level testing required for products or devices.



2. A typical automated test equipment (ATE) setup. (Courtesy of Advanced Semiconductor Engineering Inc.)

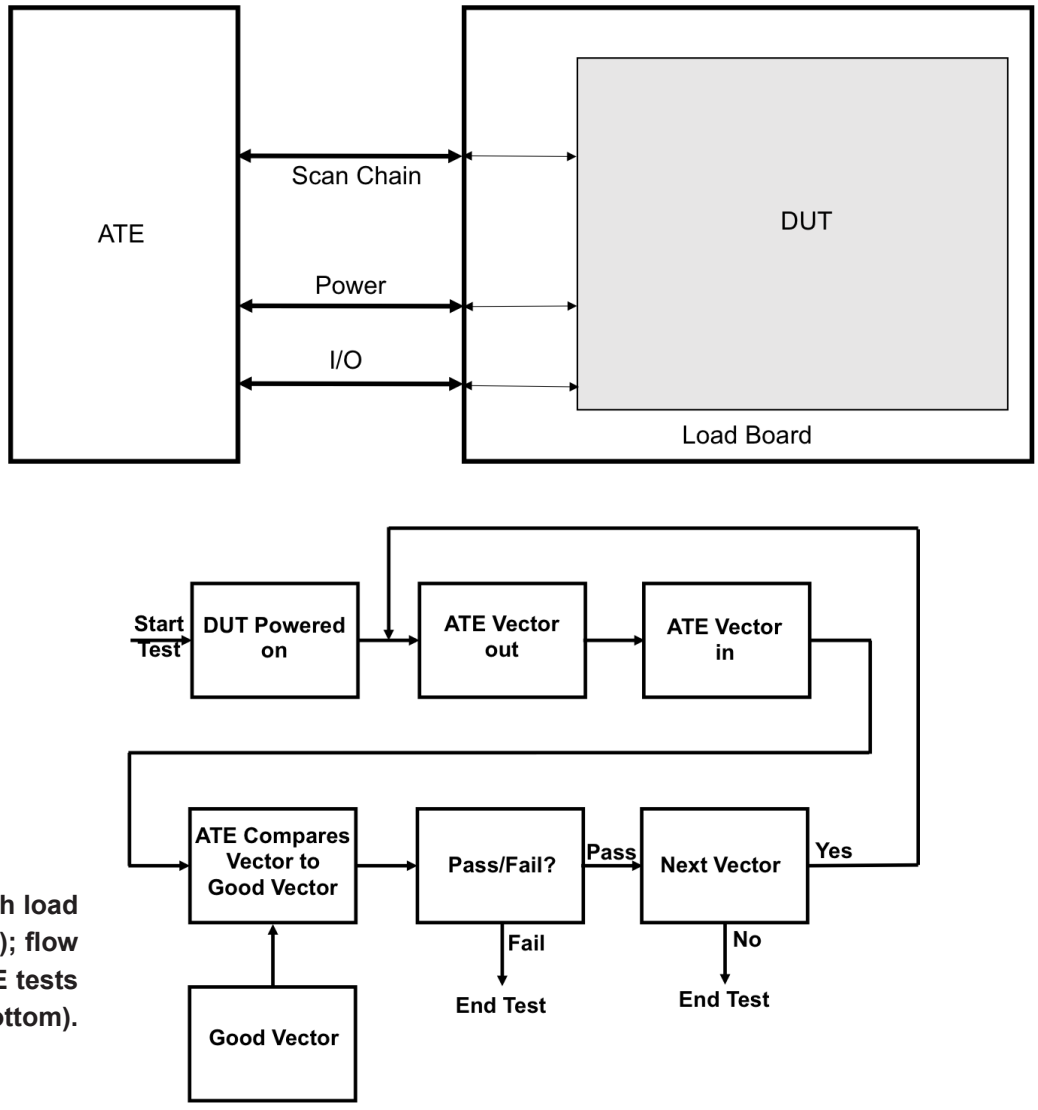
Traditionally, semiconductor testing is focused on components rather than systems since most semiconductor devices are used as discrete components within a larger system. Component testing is primarily divided into two parts: wafer-level testing and packaged-device testing.

In a wafer probe,[2] the equipment will initiate different tests by probing each die in order to determine good die that will be packaged for further testing. Once the

semiconductor die is packaged, the test equipment can perform the next set of tests, which includes external circuits, in order to finalize the component to be sold.

Due to the volume of products manufactured in the semiconductor world, the component-level testing uses automated test equipment (ATE) *(Fig. 2)*. Such ATEs use input vectors, patterns of 1s and 0s, or voltages designed to test for and uncover faults in the DUT. This is done by comparing the actual output vectors of the DUT to the expectations of the design specification, datasheet, and/or statistical characterization of known-good devices. ATEs are designed to use different test fixtures depending on the testing process and device to provide high test throughput and minimize the idle time of the ATE. For example, load boards enable automatic handling of packaged devices.

Figure 3 shows a simple block diagram of an ATE interacting with a packaged DUT via a load board and a flow graph of how it tests the DUT. While the ATE can have access to some or all of the pins of a given device, the primary interaction between the ATE and complex DUTs, such as a processor or system-on-chip (SoC), is generally via a JTAG (Joint Test Action Group) Test Access Port (TAP) and boundary-scan chain infrastructure



3. ATE test setup with load board and DUT (top); flow graph of how the ATE tests the DUT (bottom).

(Fig. 3, top). These elements inside a DUT can be accessed via a JTAG interface, which allows the testing of a device with different methodologies, such as automatic test pattern generation (ATPG) to detect stuck-at faults, built-in self-test (BIST) to detect faults in both memory and logic,[3] or functional tests like IO loopback *(Fig. 3, bottom)*.

Traditionally, when building real-world products or devices, a system-level testing (SLT) methodology[4] is used. Generally, this involves loading production software or firmware on to the system and testing the system-level functionality of each component by covering all of the intended use cases. In many cases, this process is more manual.

An interesting example comes from the early part of Gene Frantz's career on the manufacturing production line in the Texas Instruments calculator division. Instead of an ATE, many times the production tester was a human. The production test on the DUT (in this case, a calculator) consisted of a set of test vectors (an equation) entered into the DUT and the output test vector (resulting answer to the equation) being read by the tester (human) with a determination of pass or fail. Depending on the volume of production, this type of manual testing process is still used today for system-level testing.

System-in-package devices, on the other hand, fall somewhere in between. They incorporate many tested die themselves, as well as other semiconductor components connected together. As such, they can be considered a system, requiring system-level testing. However, the good die may not have been as fully tested as individual packaged devices and, therefore, can't be considered a component, requiring component-level testing in SiP. This leads to the question: How should a SiP be tested?

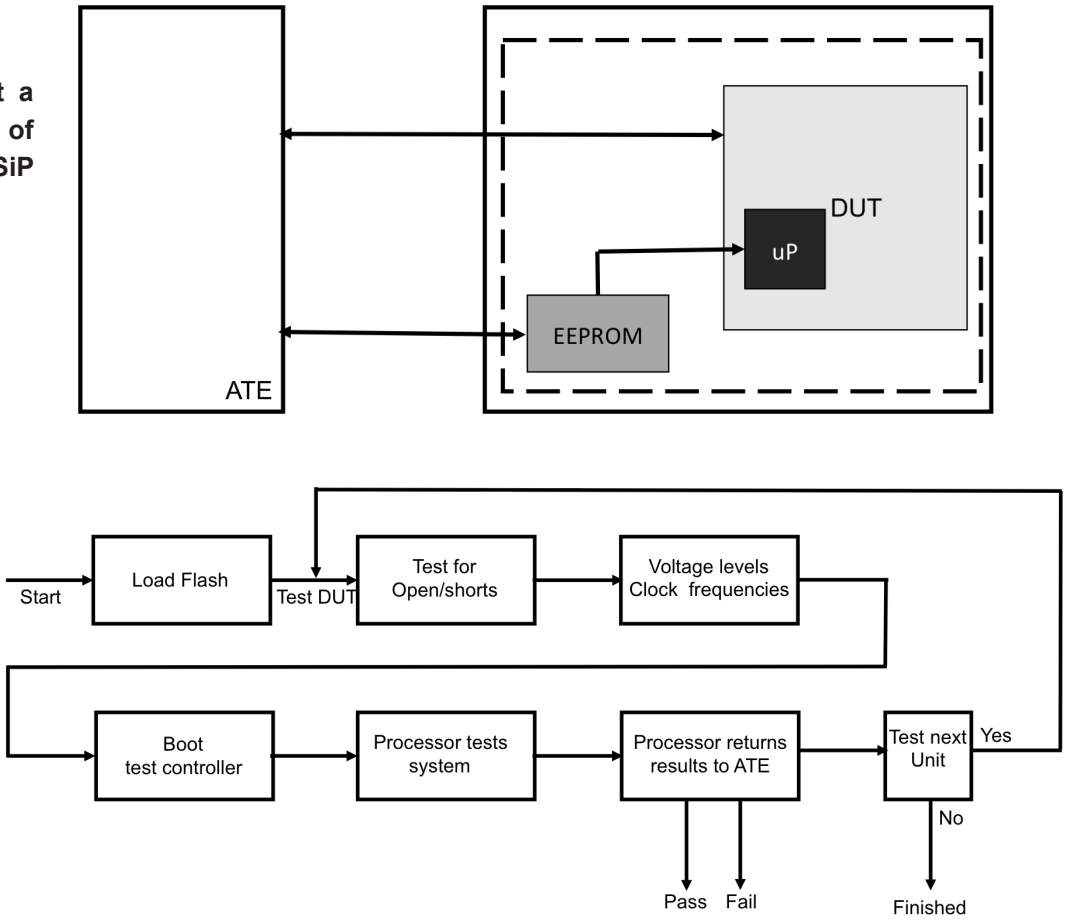
How Should the SiP be Tested?

System-in-package devices can consist of multiple active and passive components. To test every component individually, all of the pins of each component need to be brought out to a pin/ball on the SiP. While this would enable full component-level packaged-device testing, it also drastically reduces the benefits of a SiP. Since manufacturing testing shouldn't reduce the design, cost, and size benefits of a SiP, a hybrid approach is required to verify and validate a SiP.

Component-level testing should be employed for all direct connections between die and the package pins/balls. This will ensure that there are no structural faults and provide a platform for characterization similar to what would be performed on standard packaged components.

On the other hand, system-level testing should be employed to validate and characterize all internal connections. This could include functional-level tests to validate connections between components, such as a processor and DDR memory. It could also involve stress tests to verify proper operation under heavy loads, e.g., confirming that a power-management IC (PMIC) can supply enough current to meet system needs. SiP devices may also use some pins/balls as test points (i.e., pins that should not be used functionally) to provide visibility on internal signals. For example, test points can be employed to monitor voltage rails only used within the SiP.

Using a hybrid testing approach for SiP devices provides several benefits. First, since components are already connected together within the SiP, those intermediate connections no longer have to be tested as rigorously as they would when testing the component individually. For example, if a PMIC provides a voltage rail that's used completely within the SiP, the PMIC output no longer must be fully characterized for all potential output loads



4. ATE setup to test a SiP (top); flow graph of the ATE testing the SiP (bottom).

since the output load is, by design, fixed.

Similarly, the input pins of all components attached to that voltage rail no longer need to be tested over a wide range of input voltages since that, too, is fixed. This allows for a reduction in the component-level tests required, since that connection can now be validated by a single system-level test. In addition, the form factor of a SiP makes it possible to utilize semiconductor ATEs, which can reduce the time needed for handling during many system-level tests and automate what might have otherwise been a manual process.

Testing a SiP as a Semiconductor

Given the SiP form factor, it can be handled as if it were a semiconductor component. Socketed load boards (i.e., load boards that allow an ATE to connect to one or more DUTs) enable the ATE to send test vectors to the DUT and verify the resulting vectors of the test. In addition to validating the test vectors, the ATE can also perform open and short testing as well as voltage-level verification on the DUT. For example, the following diagrams describe how the OSD3358 SiP from Octavo Systems is tested as a semiconductor component rather than as a typical end system, such as a printed circuit board (PCB) or system-on-module (SoM).

As shown in *Figure 4 (top)*, the ATE interfaces with the SiP and non-volatile memory on the load board. The socketed load board provides the ATE with access to all of the SiP device's pins. *Figure 4 (bottom)* shows the flow graph of the test procedure. Open and

short testing is first performed to eliminate DUTs (in this case, SiPs) with manufacturing faults that resulted in unconnected or shorted signals. The ATE then supplies power and verifies the voltage levels of the SiP. Finally, a software program contained in the non-volatile memory, which includes functional tests, is copied into the SiP during boot and is used to examine the rest of the SiP. This program interfaces to the ATE through the test vector input and output interface whereby the ATE can then send the commands to control which tests are executed by the SiP. *Figure 5* shows the OSD335x SiP undergoing test.

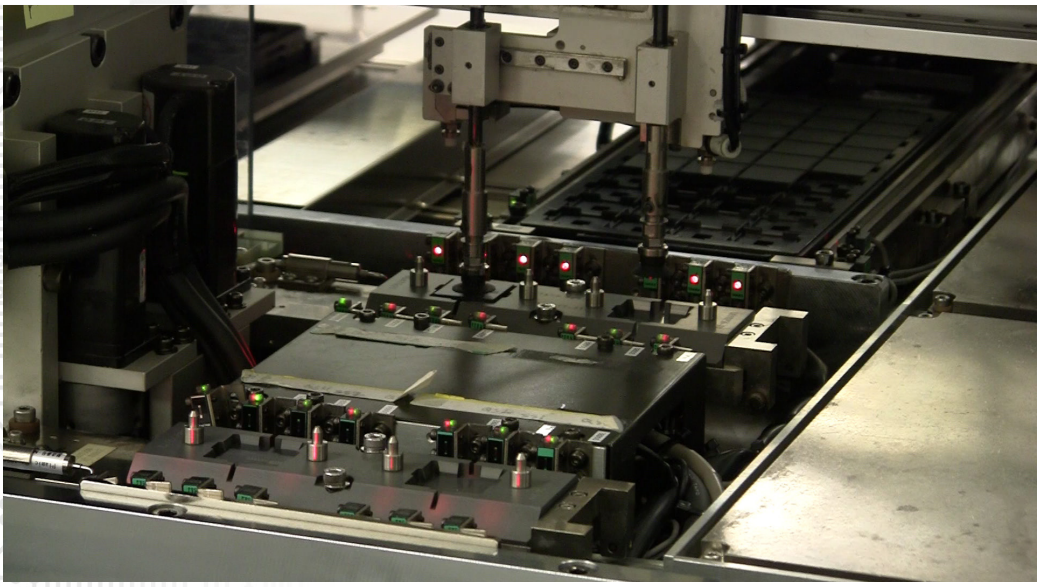
These tests might include verifying the hardware inside the SiP or validating various interfaces. After each test, the SiP can send an output via the vector interface that reflects the outcome of the test. Consequently, that part can be sorted and binned based on whether the device passed or failed the test. In general, the tests should be as short as possible and ordered based on which covers the most common failures, so that "bad" devices can be found as quickly as possible.

There are several advantages to this methodology. It's easy to update the non-volatile memory to add more tests or update existing tests. In addition, the quick feedback loop between the DUT and the ATE means that failures are identified faster and in a completely automated manner. Boot time is minimized since the DUT need only boot and load the tests one time. This can result in shorter test times, which reduces the cost of the device.

Yield

While many testing benefits can be realized with SiP technology, one classical concern often raised is yield. The argument is, given that SiP can contain hundreds of components, each with their own failure rate, the final yield of a SiP is the product of the yields of individual components. For example, if you have five components within a SiP, each with a 95% yield, theoretically the resulting SiP yield is only approximately 77% (0.95 * 0.95 * 0.95 * 0.95 * 0.95 ≈ 0.77). However, this isn't what's actually seen.

In reality, SiP yields are much higher due to a combination of factors. As discussed above, when discrete components are tested, all inputs and outputs must be fully tested. Furthermore, tighter test limits, or guard-banding, are applied to ensure that the component can be used in all extremes of the use conditions called out in the general-purpose specifications.



5. The OSD335x-SM SiP under test. (Courtesy of Advanced Semiconductor Engineering Inc.)

However, within a SIP, the use environment is known and controlled. For internal connections, variation in input voltage, current load, timing, and other variables are minimal. Therefore, devices that might have otherwise failed the normal component testing can be used within a SiP because it meets

the requirements for the given SiP. Hence, SiP yields depend on the system use requirements, more like an end product, rather than just the individual component yields.

As more semiconductor companies look to make their devices "SiP ready," refinements in device testing will occur in wafer-level testing, enabling further improvements in SiP yields. Eventually, wafer-level tests will include any provision to make physical changes in chips, such as resistor trimming or fuse blowing, as well as additional test coverage to avoid complex testing in SiP form.

Conclusion

By using a hybrid of component- and system-level testing methodology, SiP offers benefits to the system manufacturer as well as the end customer of a more robust and cost-effective product. This is achievable if SiP manufacturers perform system tests while utilizing the testing methodologies and infrastructure of semiconductor testing.

We have found this method to yield extremely high rates of pass at next-level system tests. This unique method of testing, in addition to all of the other benefits of using a SiP device discussed in this series, provides strong arguments that a SiP solution like that developed by Octavo Systems may be the best solution for any embedded product design.

ERIK WELSH is the Applications and Systems Manager for Octavo Systems. Erik comes to Octavo after spending three years as the Principal Systems Architect at Mango Communications developing platforms for cutting-edge wireless research targeting the WARP (Wireless Open-Access Research Platform) project. Prior to that, he spent 11 years at Texas instruments in a variety of engineering and customer support roles. He began his career as a system-on-chip (SoC) designer eventually leading SoC Security Architecture development. He later spent time as an Applications Engineer supporting industry-leading customers in the PC industry. Erik earned a Bachelor of Science and Masters in Electrical Engineering from Rice University.

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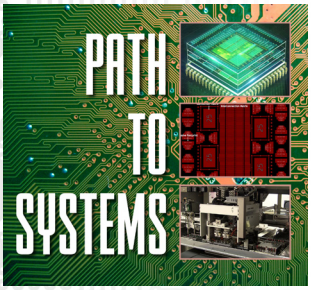
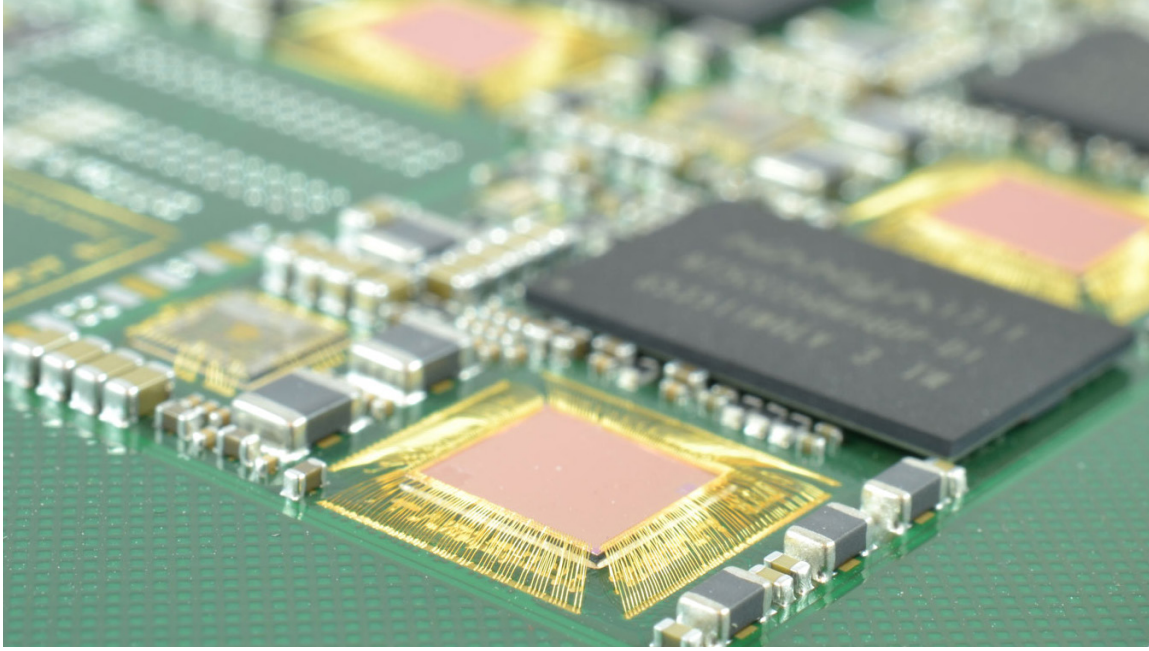




CHAPTER 5:

The Time of System-in-Package Has Arrived

NEERAJ DANTU, Applications and Systems Engineer, MASOOD MURTUZA, Manager Package Engineering, ERIK WELSH, Applications and Systems Manager, and
GENE FRANTZ, Chief Technology Officer, Octavo Systems

Part 5 presents the customizable future of system in package, in which new tools and processes provide customer-selectable sub-modules while maintaining low design and manufacturing costs.

The previous articles of this series have discussed the innovation and evolution of the integrated-circuit industry and how system-in-package (SiP) devices fit into the market. In the first article, Opportunities and Challenges for the Next Generation of Semiconductor Integration, we looked at how the ability to integrate more transistors at a lower cost, increase performance, and lower power dissipation has revolutionized not only the semiconductor industry, but all industries who have been able to take advantage of silicon devices.

In Why a SiP?, we walked through the underlying technology of a SiP, using the Octavo Systems OSD335x-SM as an example and exploring how SiP technology is taking on a role as a complementary capability to further drive industries creating and using semiconductor technology. Then in SiP—Leveraging Mass Production on a Small Scale, we explored issues and opportunities resulting from this emerging technology. We evaluated the design and production flows of SiP technology, delving into the example of the 100-Plus-Component-OSD335x C-SiP, a complete computer in a package.

Finally, because of the advantages a SiP brings to all stages of a system production from design to manufacturing and testing, in A SiP of Reliable Advantage–Systems Under Test we highlighted the importance of creating the tools and processes to allow for the industry to utilize SiP technology.

In this article, we look toward the future of system-in-package, in which new tools and processes provide a system designer with capabilities to customize SiP devices while maintaining low design and manufacturing costs. From customer-selectable sub-modules to SiPs within SiPs, we begin to glimpse the ultimate system-in-package.

Creating a System-Specific SiP

Two major advances need to be made to give the system designer the ability to create system-specific SIP devices:

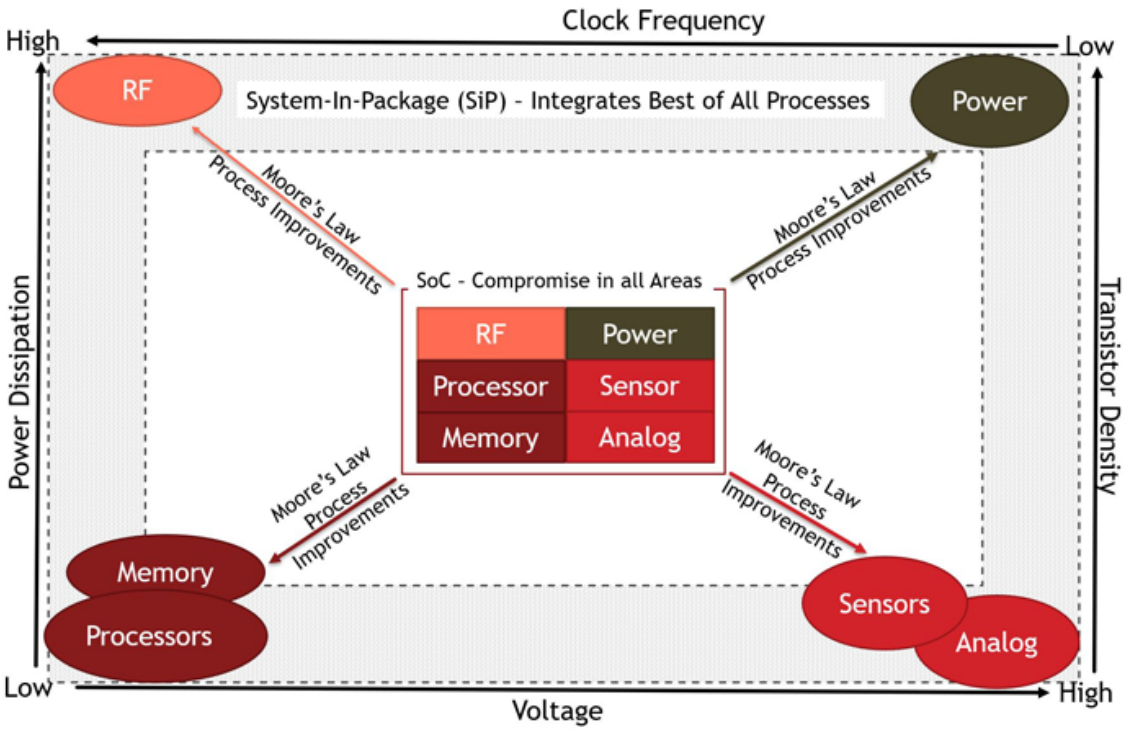
- The creation of a design methodology to allow for semi-custom and custom SiPs.
- The creation of a manufacturing flow that will allow for low-volume manufacturing of SiP devices.

The Design Methodology

The concept of a "system in a package" implies that it's an integration of different components rather than the creation of a single component. While this concept doesn't eliminate the need for new individual components, it changes the role of component design. Given that individual components will be integrated together within the SiP, we need to think about and design "SiP-ready" components rather than just standard components, such as a traditional system-on-chip (SoC).

The design methodology for SiPs borrows from traditional SoC design as well as printed-circuit-board (PCB) design and shifts semiconductor manufacturers' focus from traditional methods of designing single monolithic components to designing systems with several interconnected components. For example, instead of trying to cram as much as possible into a single SoC, it would be better to split components along silicon process lines—analog components in optimized analog processes, digital components in optimized digital processes, RF components in optimized RF processes, and power components in optimized power processes *(Fig. 1)*.

By taking advantage of the process improvements generated by Moore's Law, not only can we use better components, we also reduce "wasted" silicon because we need only integrate the components necessary for the system. In addition, to realize the potential of



1. Moore's Law has caused semiconductor processes to progress in multiple directions.

SiP technology, we will not only need to define the interfaces between "SiP-ready" components, but create tools and processes that will allow us to partition a system so that the best aspects of SiP technology and silicon technology are utilized.

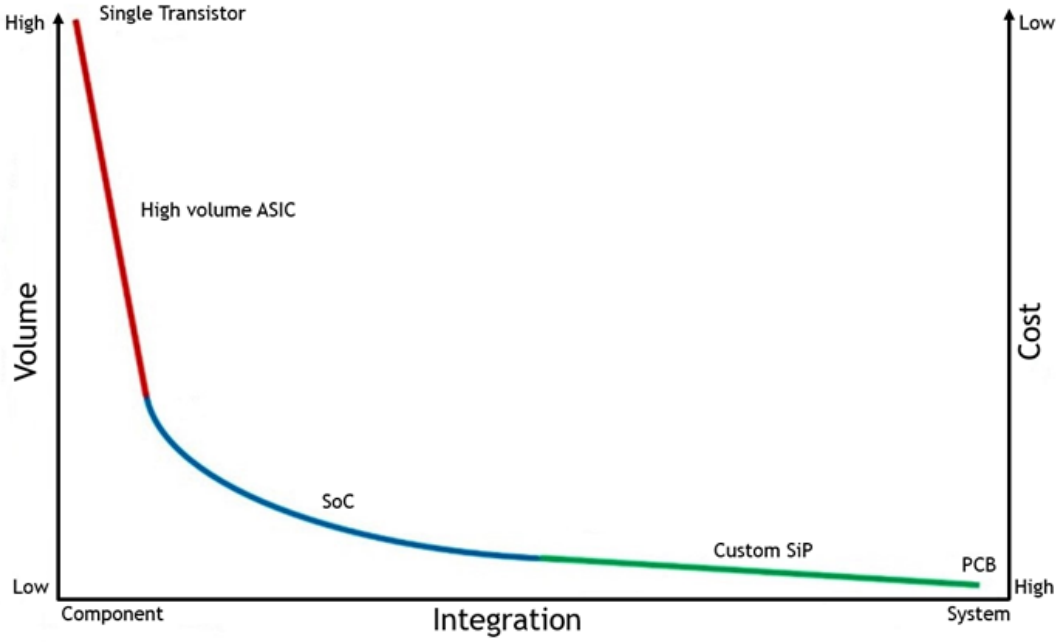
Beyond changes to the design methodology for component manufacturers, customers also must shift their design methodologies to better utilize SiP technology. As SiP devices become more customizable, the ability to generate schematics, layout, and a bill of materials for a custom SiP based on as product specification becomes paramount. Furthermore, the ability to prototype with SiP will need to be understood and integrated into the product design process.

The Manufacturing Flow

Just as the move from monolithic components to integrated systems impacts the design methodology, it will also require adjustments in the manufacturing flow. Today, high-volume SiPs can be manufactured with the same process as a standard semiconductor component. This is both good news and bad news. The good news is that the component manufacturing process has had many decades of optimization to maximize yield, maximize throughput, and minimize manufacturing costs. The bad news is that none of these characteristics (yield, throughput, and cost) lend themselves to the low-volume manufacturing required by a custom SiP.

Figure 2 shows the relationship between integration and volume. At one end, we have extremely high-volume components that are fixed-function and integrate relatively little of the system. At the other end, we have complete systems that integrate all components but have a much lower volume. Given that manufacturing processes have been optimized for high volumes, this means that the cost per unit increases as the volume decreases.

Ideally, we would like to integrate a custom SiP with the low cost of manufacturing of a high-volume component. We believe that this can be achieved with innovation around



2. The number of transistors in a device vs. volume of device

customizable SiPs. Given the programmability of today's manufacturing, assembly, and test machines, we see that it will be possible to reduce the economic manufacturing volume from millions of units to a single unit. Just as stencils are being replaced with programmable solder-paste printers to reduce the cost of small-volume PCB manufacturing today, programmable wire bonders, pick-and-place machines, and testers will usher in an era of increased integration and reduced cost at small volumes.

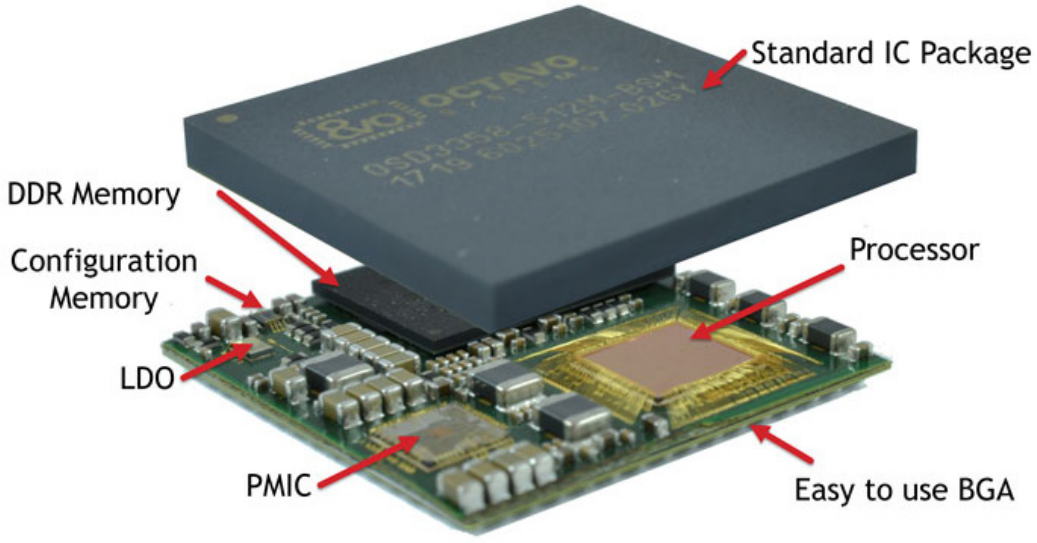
What's Driving SiP Technology Today?

Traditionally, the driving force for SiP technology has been the demand to place more components into a given PCB area to allow for smaller form factors. By utilizing tighter place-and-route rules and unpackaged die, SiPs were able to integrate components of a system much more efficiently than on a PCB. In addition, SiPs were able to even utilize the third dimension using techniques like stacking die or in-substrate passives. However, this demand and ability has been driven by large volumes and require large upfront investments.

Fortunately, thanks to lowering cost for SiP technology, i.e. smaller volume requirements and initial investment, we're seeing system simplification become a driving force behind SiP technology. The desire to simplify a system design by abstracting parts of it away, enabling designers to focus on the key parts of their systems, has become as important, if not more important, than packing components into a given volume.

As design and system complexity grow while design teams shrink, the need for easy-to-use components that integrate the tedious, non-value-added portions of the design becomes critical. For example, in a microprocessor-based system, the connections between the processor, power management, and high-speed memory are the same every time for a given microprocessor. *Figure 3* shows a SiP, which integrates a TI AM3358 microprocessor, DDR3 high-speed memory, and the power management integrated circuit (PMIC), that greatly simplifies the end system design.

As the demand for system-level integration and simplification ramps up, the compo-



3. Shown is a tightly integrated Texas Instruments AM335x-based system-in-package—the OSD335x from Octavo Systems.

nents of today will become "SiP-ready" components while the SiPs of today will become "sub-system in packages (S-SiPs)". S-SiPs and SiP-ready components will be integrated into larger SiPs as system integration drives SiP technology toward the ultimate SiP.

The Ultimate SiP

Given the changes in design and manufacturing required to utilize SiP technology, we should ask ourselves: "What would be the 'Ultimate SiP?'" The simple answer is a component with zero pins. It's a custom component that completely performs the intended function without the need to be physically connected to anything else. It can communicate wirelessly, create or harvest its own energy, and perform its necessary functions autonomously. And it's cheap to manufacture, can operate in harsh conditions, and requires little maintenance.

By integrating all of the system's components into a single package, we rid ourselves of many of the challenges we face today as we struggle to build systems. Instead of focusing on the "how do I make XYZ work?," SiP technology will free you to focus on the "what about …?" as system design transitions from a select few implementers to the many dreamers where creativity begins by first asking the right questions.

Conclusion

Even with the slowdown in the ability to shrink transistors, there appears to be a great future ahead in the world of semiconductor integration. We can see the continuation of Moore's Law as it begins to focus on system integration where we integrate using silicon rather than on silicon. With the capabilities provided by system-in-package, there's no end to the number of transistors we will be able to integrate into an IC package. So, the next time you look to design a system, ask yourself: "Is there a SiP for that?"

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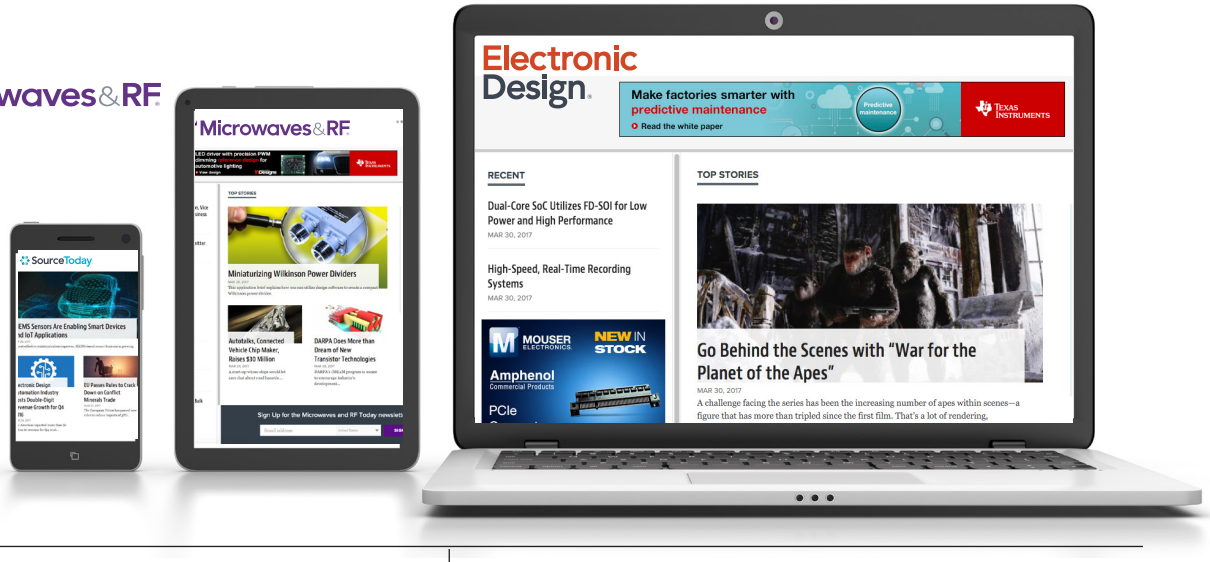

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