

Three Compact Solutions for High Step-Down Voltage Ratios

The article explains why the non-isolated buck converter faces challenges to downconverting high dc input voltage to low output voltage at high output current, and presents three approaches for downconverting such steep voltage ratios.

ystem designers can be faced with the challenge of downconverting high dc input voltages to very low output voltages at high output current (such as 60 V down to 3.3 V at 3.5 A), while maintaining high efficiency, small form factor, and simple design.

Combining high input-to-output voltage difference with high current automatically excludes the linear regulator due to the excessive power dissipation. Consequently, the designer must opt for a switching topology under these conditions. However, even with such topologies, it's still challenging to implement a design that's sufficiently compact for space-restricted applications.

This article will address why the non-isolated dc-dc buck converter (referred to simply as buck converter in this article) is facing serious challenges to downconverting high dc input voltages to very low output voltages at high output current. Three different approaches will be presented for downconverting steep voltage ratios while keeping a small form factor.

Challenges Faced by DC-DC Buck Converters

One candidate for high step-down ratios is the buck converter. It's the topology of choice when having to step down an input voltage to a lower output voltage (such as $V_{IN} = 12$ V down to $V_{OUT} = 3.3 \text{ V}$) in an efficient way, with a significant amount of current, while also using a small footprint.

However, there are conditions under which the buck converter faces serious challenges to keep its output voltage regulated. To understand these challenges, we must remember that the simplified duty cycle (D) of a buck converter operating in continuous conduction mode (CCM) is:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

The duty cycle also relates to the switching frequency (f_{SW}) in the following way, where the on-time (t_{ON}) is the duration over which the control FET stays on during each switching period (T):

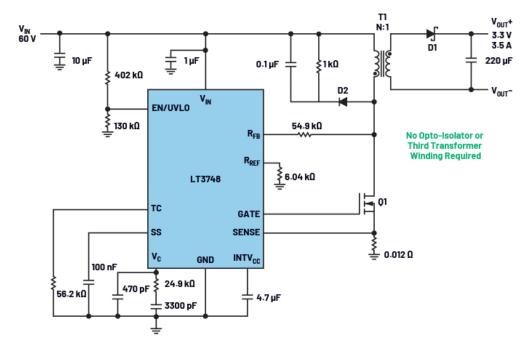
$$D = \frac{t_{ON}}{T} = t_{ON} \times f_{SW} \tag{2}$$

Combining Equation 1 and Equation 2 shows how toon is influenced by the step-down voltage ratio and f_{SW} :

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \tag{3}$$

Equation 3 tells us that the on-time decreases when there's an increase in input-to-output voltage ratio (V_{IN}/V_{OUT}) and/or f_{SW}. This means that the buck converter must be able to operate with very low on-time to regulate the output voltage in CCM under high V_{IN}/V_{OUT} ratio, and it becomes even more challenging with a high f_{SW}.

Let's consider an application with $V_{IN(MAX)} = 60 \text{ V}$, V_{OUT} = 3.3 V at $I_{OUT(MAX)}$ = 3.5 A. When required, we shall use values from the LT8641 datasheet because a solution with the LT8641 will be provided in a later section. The required minimum on-time $(t_{ON(MIN)})$ corresponds to the highest input voltage ($V_{IN(MAX)}$). To assess this $t_{ON(MIN)}$, it's advised to make Equation 3 more accurate. By including V_{SW(BOT)} and V_{SW(TOP)}, the voltage drops for the buck converter's two power MOSFETs, and replacing V_{IN} with V_{IN(MAX)}, we obtain:



1. This circuit solution uses the LT3748 to downconvert 60-V input to 3.3-V output.

$$t_{ON(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{V_{IN(MAX)} - V_{SW(TOP)} + V_{SW(BOT)}} \times \frac{I}{f_{SW}}$$
(4)

Using Equation 4 with $V_{IN(MAX)}$, $f_{SW} = 1$ MHz, we obtain a t_{ON(MIN)} of 61 ns. For V_{SW(BOT)} and V_{SW(TOP)}, we made use of the values provided for R_{DS(ON)(BOT)} and R_{DS(ON)(TOP)} in the LT8641 datasheet, knowing as well that VSW(BOT) = $RDS(ON)(BOT) \times IOUT(MAX)$ and VSW(TOP) = $RDS(ON)(TOP) \times IOUT(MAX)$.

Buck converters can rarely guarantee a t_{ON(MIN)} with the short value of 61 ns obtained above; therefore, the system designer is forced to search for alternative topologies. There are three possible solutions for high step-down voltage ratios.

Three Compact Solutions for $V_{IN(MAX)} = 60 \text{ V}$, $V_{OUT} = 3.3$ V at $I_{OUT(MAX)} = 3.5 A$

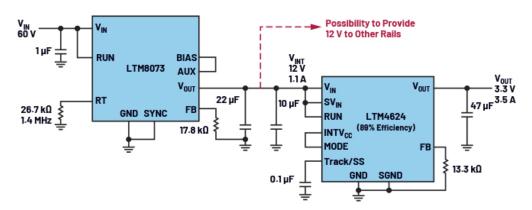
Solution 1: LT3748 Non-opto Flyback

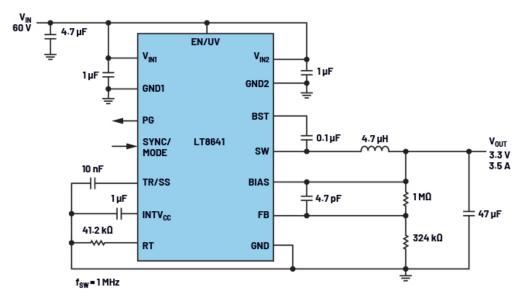
The first option consists of using an isolated topology, where the transformer performs most of the downconversion thanks to its N:1 turns ratio. For that matter, Analog Devices offers flyback controllers such as the LT3748 that don't require a third transformer winding or optoisolator, making the design simpler and compact. The LT3748 solution for our conditions is presented in *Figure 1*.

Even though the LT3748 solution simplifies the design and saves space compared with a standard flyback design, it still requires a transformer. For applications that don't need isolation between input and output sides, it's preferred to avoid this component, which adds complexity and increases the form factor vs. a nonisolated solution.

Solution 2: LTM8073 and LTM4624 µModule Devices

2. In this circuit solution, the LTM8073 and LTM4624 downconvert 60-V input to 3.3-V output.





3. This circuit solution utilizes the LT8641 to downconvert 60-V input to 3.3-V output.

As an alternative, the designer can downconvert in two steps. To achieve a reduced component count of only 10, two µModule devices and eight external components can be used (Fig. 2). Moreover, the two µModule devices already integrate their respective power inductor, sparing the system engineer a design task that's rarely straightforward. The LTM8073 and LTM4624 both come in BGA packages, with respective dimensions of $9 \times 6.25 \times 3.32$ mm and 6.25×6.25 \times 5.01 mm (L \times W \times H), providing a solution with a small form factor.

Since the LTM4624 exhibits an efficiency of 89% under these conditions, the LTM8073 supplies at most 1.1 A to the input of the LTM4624. Given that the LTM8073 can provide up to 3 A of output current, it can be used to supply other circuit rails. With this purpose in mind, we selected 12 V as the intermediary voltage (V_{INT}) in Figure 2.

Despite avoiding the usage of a transformer, some designers might be reluctant to implement a solution that requires two separate buck converters, especially if no intermediary voltage is required to supply other rails.

Solution 3: LT8641 Buck Converter

Consequently, in many cases, using a single buck converter would be preferred because it provides the optimal solution to combine system efficiency, a small footprint, and design simplicity. But did we not just demonstrate that buck converters can't cope with high V_{IN}/V_{OUT} combined with high f_{SW}?

This statement might apply to most buck converters, but not all of them. For instance, buck converters such as ADI's LT8641 is specified with a very short minimum on-time of 35 ns typical (50 ns max) over the full operating temperature range. Those specifications are safely below the required minimum on-time of 61 ns previously calculated, providing us with a third possible compact solution. Figure 3 shows the simplicity possible with the LT8641 circuit.

It's also worth noting that the LT8641 solution can be the most efficient of the three. Indeed, if efficiency must be further optimized compared with Figure 3, we can decrease f_{SW} and select a bigger inductor size.

Although f_{SW} also can be decreased with Solution 2, the integration of the power inductors doesn't offer the flexibility to increase the efficiency beyond a certain point. Moreover, using two consecutive downconversion stages has a small negative impact on efficiency.

In the case of Solution 1, the efficiency will be very high for a flyback design, thanks to its boundary-mode operation and that all components are removed with the no-optical feedback design. However, the efficiency can't be fully optimized because there's a limited number of transformers to select from, as opposed to the array of inductors available for Solution 3.

An Alternative Way to Check Whether LT8641 Fulfills Requirements

In most applications, the only adjustable parameter in Equation 4 is the switching frequency. Consequently, we reformulate Equation 4 to assess the maximum permitted f_{SW} for the LT8641 under given conditions. By doing this, we obtain Equation 5, which also can be found on page 16 of the LT8641 datasheet:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)} \times (V_{IN(MAX)} - V_{SW(TOP)} + V_{SW(BOT)})}$$
(5)

Let's use this equation with the following example: V_{IN} = 48 V, V_{OUT} = 3.3 V, $I_{OUT(MAX)}$ = 1.5 A, f_{SW} = 2 MHz. An input voltage of 48 V is commonly found in automotive and industrial applications. By inserting those conditions in Equation 5, we obtain:

$$f_{SW(MAX)} = \frac{5 \text{ V} + 0.0825 \text{ V}}{50 \text{ ns} \times (48 \text{ V} - 0.1575 \text{ V} + 0.0825 \text{ V})} = 2.12 \text{ MHz} (6)$$

Therefore, under the provided application conditions, the LT8641 would operate safely with f_{SW} set as high as 2.12 MHz.

Conclusion

Three different methods were presented to achieve a compact design under high step-down voltage ratios. The LT3748 flyback solution doesn't require a bulky optoisolator and is recommended for designs where isolation is necessary between input and output sides. The second method, which involves implementing the LTM8073 and LTM4624



µModule devices, is of particular interest when the designer is hesitant to select the optimal inductor for the application and/ or when an additional intermediary rail must be supplied. The third method, a design based on the LT8641 buck converter, offers the most compact and simplest solution when the sole requirement is steep voltage downconversion.

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