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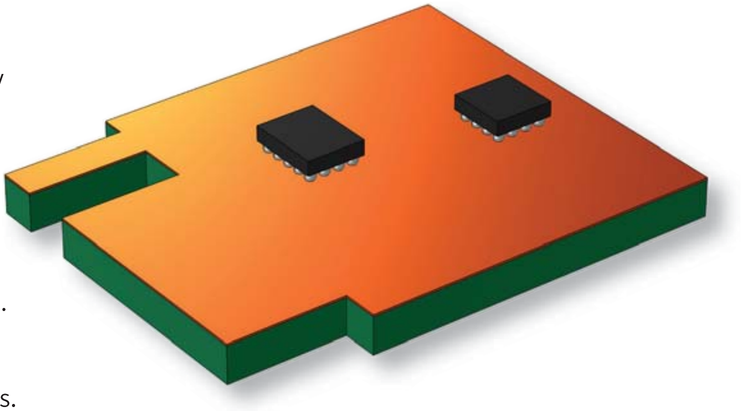
Thermomechanical Fatigue of Electronics Products



Electronic devices are abundant, ranging from cellphones and computers to household appliances and automobiles. Ever-increasing demands on energy efficiency, performance, and prolonged service life present significant challenges to design engineers. In operating these devices, temperatures in the electronic circuitry vary over time, and this cyclic thermal loading produces mechanical stresses and strains that can cause fatigue damage. The product fails when sufficient fatigue damage has accumulated.

Multiphysics simulation software can be used to assess the risk of fatigue failure for electronic products. A multiphysics simulation computes the cyclic thermal loading, including the heat generated by the electronic components. In addition, the simulation include the effects of surrounding airflow and the radiative heat transfer. The simulation uses computed temperatures to calculate stress and strains in the component. The simulation then calculates the fatigue damage produced by this thermomechanical loading.

In this presentation, guest speakers Kyle Koppenhoefer and Joshua Thomas from AltaSim Technologies will discuss the development of a thermomechanical fatigue model for electronic devices subjected to a complex thermal environment. The webinar will also include a live demonstration using the COMSOL Multiphysics® software and a Q&A session.

SPEAKER: Kyle Koppenhoefer, Altasim Technologies

Kyle Koppenhoefer is the president of AltaSim Technologies. He and his business partner founded AltaSim 20 years ago. He works with customers to identify how computational analysis can be used to provide solutions to their products and manufacturing processes. Prior to cofounding AltaSim, Kyle worked for the Department of Defense and the Edison Welding Institute. He holds a PhD in civil engineering from the University of Illinois.

SPEAKER: Joshua Thomas, Altasim Technologies

Josh Thomas is a senior engineer at AltaSim Technologies. He has provided consulting and training support in COMSOL Multiphysics® over the last 10 years. He is a lead instructor in many of AltaSim's classes and has worked extensively with structural mechanics problems and multiphysics problems involving thermal and structural analysis. Josh received his bachelor's degree in aerospace engineering and master's degree in mechanical engineering from The Ohio State University.

SPEAKER: Akhilesh Sasankan, COMSOL

Akhilesh Sasankan is a technical sales engineer at COMSOL. Before starting at COMSOL, he received master's in mechanical engineering from Arizona State University. Akhilesh's areas of interests include CFD and high-performance computing.

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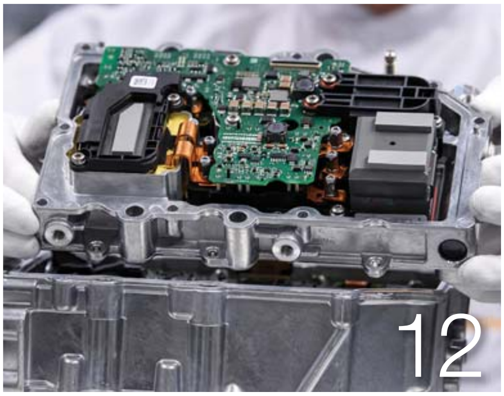

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ElectronicDesign 70 YEARS

Editorial

WILLIAM WONG | Senior Content Director

70 Years and Still Going Strong

It’s our 70th anniversary and we’re celebrating by rolling out new features in print and online throughout 2022.

A LOT HAS happened in the world over the past 70 years, which *Electronic Design* has been covering from an engineering and technology perspective. Our sister publication, *Microwaves & RF*, celebrated its 60th anniversary last year.

Things are much different than when we started with massive print issues and a host of editors dedicated to specific technology beats. These days, our editors and contributors are as apt to deliver our content as videos. We’re still in print, of course, but the bulk of our content is online with a focus on engineers who are likely viewing this on a PC or smartphone.

I’ve had the pleasure of celebrating *Electronic Design’s* 50th and 60th anniversary as an editor. Our publication is just a few years older than the transistor, and the vacuum tube was a technology that we covered at the start.

Nowadays, a single smartphone packs more storage and compute power with a higher-resolution screen than any portable PC of a couple decades ago. We have self-driving car races and satellite-based internet communication. Deep neural networks turned artificial intelligence (AI) and machine learning (ML) into a must-have technology. The cloud and windows render new meanings.

You may have noticed some of the changes at *Electronic Design* online, such as our digital issues in the Top Stories of the Week or the regular galleries in Products of the Week. New products have been important to engineers and developers, although these days availability can be a challenge given supply-chain issues. While AI/ML may garner the spotlight, we know that the fundamental technologies like communication, analog, power, and test rank up there in importance based on our annual salary survey.

We’re also presenting multipart article series in the *Electronic Design* library, and collecting together articles and multimedia content in our topic-oriented TechXchanges, covering areas like RISC-V, Chiplets, ROS – The Robot Operating System, and Power Supply Design. This includes our TechXchange Talks videos. Also check out Kit Close Up, which comprises quick video views of development kits that have become very important to engineers, programmers, and designers.

So, here’s to the next 70 years. Here at *Electronic Design*, we plan to continue to cover the new technologies and breaking issues impacting our industry. ed

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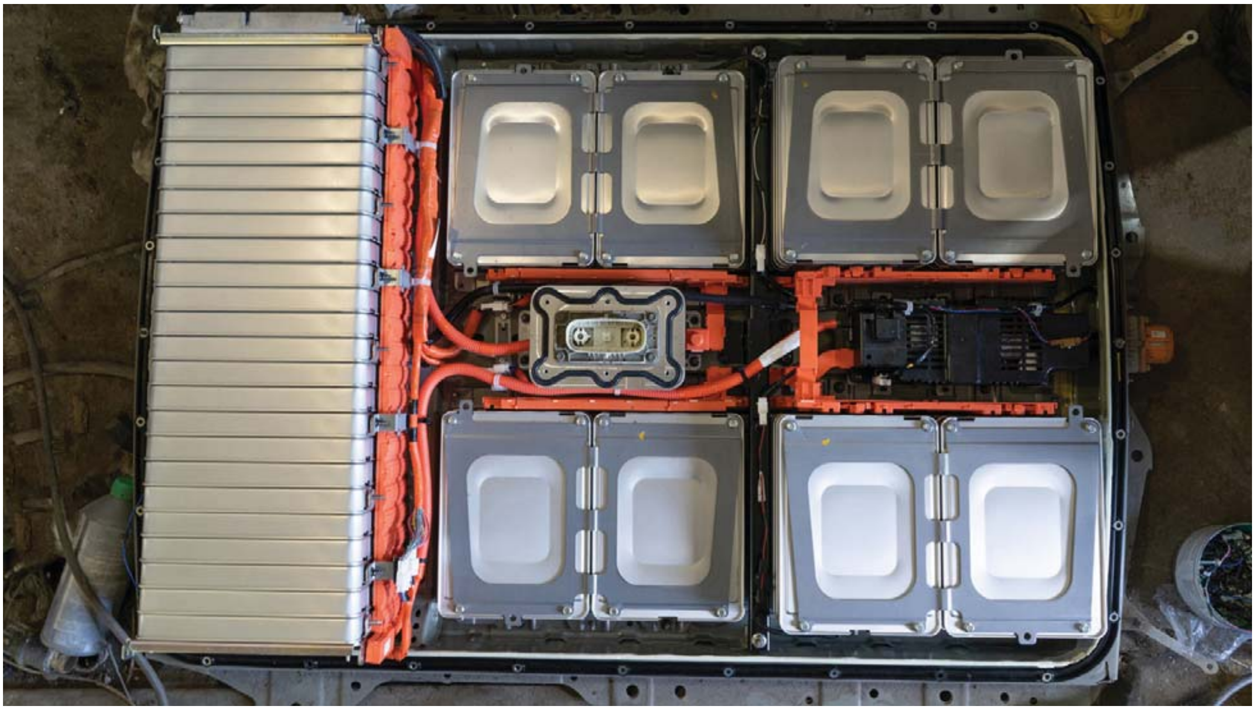
Engineering Essentials

STEVE TARANOVICH | Contributing Editor

How to Boost Power Density in Automotive Systems

More vehicle weight leads to lower miles per gallon in fossil fuels and more frequent charging in electric vehicles. Thus, power density of power supplies and batteries is a crucial factor in optimizing automotive performance.



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The latest design architectures, especially in automotive power electronic systems, are critical in the success of any new hybrid electric vehicle (HEV) or electric vehicle (EV). A high-voltage vehicle power network is necessary with voltages of 60 V and higher, along with a traditional 14-V power network.

High-voltage vehicle power network architectures contain an electrical energy-storage system and a traction drive inverter. Some HEV and EV system architectures also may contain high-voltage power electronic systems using dc-dc converters to power a low-voltage network. Examples include electrical air-conditioning compressors, cooling water pumps, oil pumps, traction bus voltage stabilization, and ac-dc converters for unidirectional or bidirectional interfaces to vehicle grids.

Let's take a look at various power systems and components in the vehicle that contribute to an overall higher-power-density architecture.

V2X power

Vehicle system power-rail architectures for vehicle-to-everything (V2X, "X" equates to grid, home, or load) power can have a 5-V bus generated, via the vehicle battery voltage, with the use of an off-battery buck converter. This type of design architecture is able to power all point-of-load (PoL) devices at a 2-MHz+ switching rate. Efficiencies of over 90% can be achieved. Such high switching rates, along with high efficiency, will greatly improve automobile power density.

GaN FETs in automotive

Using gallium-nitride (GaN) FETs in automotive power designs will enable high power density due to fast switching coupled with 600-V and higher capability in those designs. When an integrated driver is part of the solution, designers will be able to deliver as much as 2X power density, with 99+% efficiency, plus the bonus of reducing the size of power magnetics. Employing GaN-on-silicon substrates will enable a lower cost, along with a supply-chain advantage, as compared with silicon-carbide (SiC) devices.

Lightweight and compact power systems are key, especially in EV automotive systems. Engineers can now achieve extended battery range and higher system reliability—GaN enables this performance enhancement. On-board chargers and dc-dc converter sizes can be shrunk by as much as 50% with GaN vs. silicon or SiC solutions as well.

Again, here, high-frequency switching rates and high efficiency lead to excellent power density in the vehicle.

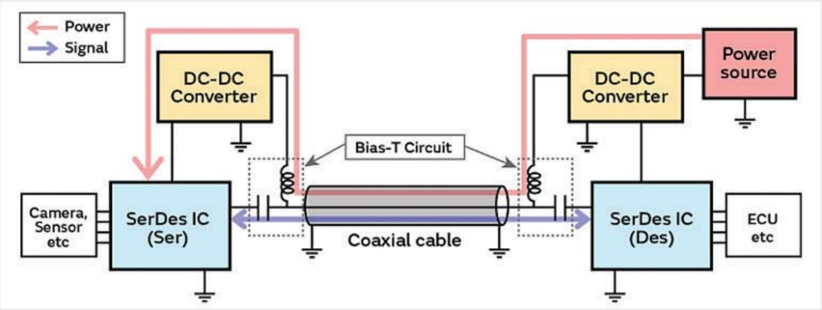
Automotive-grade current-sense resistors and shunts

Automotive power density also can be improved via the proper design usage of current-sense resistors. These resistors will have very low resistance values, good pulse performance, low temperature coefficient of resistance (TCR), low inductance, along with low noise.

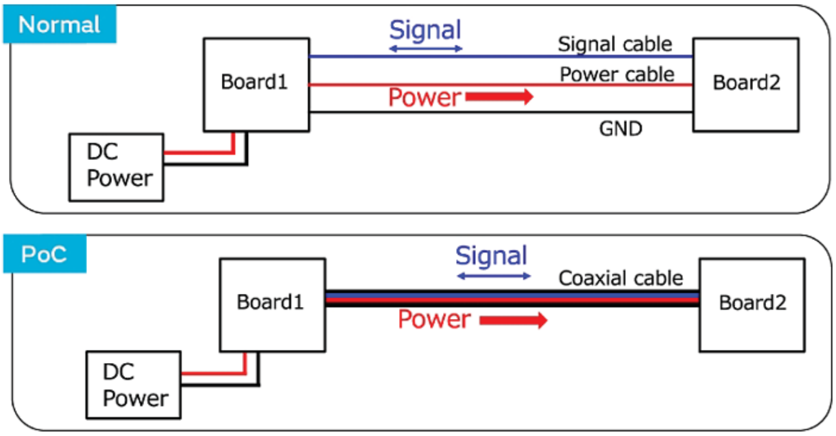
A good current-sense resistor will be able to provide exceptional pulse performance, while absorbing more electrical energy, before reaching the device temperature limit. The resistor element also must be quite robust to be able to handle higher temperatures. Laser trimming will help reduce harmonic distortion and circuit ringing, too.

When a material undergoes temperature variations, the dimensions either slightly increase or decrease as it expands or contracts. During duty-cycled or pulsed applications, power is switched off and on, which will cause repetitive heating or cooling expansion/contraction cycles.

Such thermal cycling may cause long-term reliability problems for solder joints of surface-mount components when there's a large difference in the rates of geometric expansion/contraction. These different rates are usually known as coefficient of thermal emission (CTE) mismatch. Choosing a resistor with a CTE value, close to the CTE of a circuit board's FR-4 material, will minimize this effect with better long-term solder-joint performance and lower failure rates.



1. The Bias-T circuit separates the power-supply line from the signal line. *(Image from Reference 4)*



2. The PoC system uses thin-film metal inductors on a single coaxial cable for improved power density. *(Image from Reference 4)*

Using automotive current-sense resistors can boost the power density in the automotive architecture, since the power rating increases as the resistor size decreases. In addition, designers should choose resistors that have multiple series, so that they can change series with the same size. In addition, designers can progress to higher power ratings. An all-metal construction is a positive feature in such resistors.

Designers, of course, will need to choose a resistor series that's AEC-Q200-qualified for automotive use.

Automotive-grade high-power-density inductors for LED lighting

Advanced LED driver designs are being developed using electronic components that can deliver higher luminescence and improved energy efficiency, all at lower cost. Suppliers now provide higher-power LED headlight clusters that perform well at elevated current in a smaller footprint.

Today's technologically advanced inductors used in LED lighting are able to handle higher temperatures (up to +155°C) and higher power density. Furthermore, footprint can be decreased by as much as half with the latest inductors. In the past, a popular inductor used to have a fairly large footprint of 12.5 × 12.5 mm on the printed circuit board. Today, manufacturers have decreased this size to 8 × 8.5 mm, maintaining the equivalent performance of several years ago. Pricing also has reached levels that are competitive in car manufacturing.

Automotive applications are becoming more sophisticated as they trend well beyond two or three LED drivers per automobile. Smaller inductors built with the latest advanced technology like thin-film metal lead to improved power density in the automobile. Bias-T and power-over-coaxial (PoC) circuits also use inductors that have high-impedance characteristics and lead to improved power density *(Figs. 1 and 2)*.

High-Power-Density Design for EVs

The GaN active-clamp phase-shifted full-bridge (PSFB) architecture has zero-voltage switching across the entire load and voltage range. It enables a 1.5-kW, 400- to 12-V dc-dc converter for automotive application with a wide voltage and power range. The small leakage inductance coupled with the ability to realize soft-switching, even under low load conditions, leads to a significant increase of the switching frequency up to 500 kHz.

This dc-dc converter architecture is able to transfer energy from a 400-V vehicle traction battery, in an electric or hybrid vehicle, to the 12-V electrical system. It also ensures galvanic isolation for safety.

The power density of the converter simplifies integration into an automotive vehicle. Magnetic components dominate the volume of the power electronics. Power density can be increased by raising the switching frequency. By using SiC or GaN transistors, very low conduction and low switching energies are achieved—far better than with silicon devices. The circuit topology can be seen in *Figure 3*.

Soft-switching, combined with GaN transistors and the active clamping, boosts switching frequency up to 500 kHz. This design architecture also increases power density significantly while maintaining high efficiencies—a prototype achieved greater than 95% efficiency as well as a power density of 12.5 kW/L.

Thermal Management for Automotive High Power Density

Many new electronic devices are making their way into the modern automotive system, leading to an increase in heat generated within the vehicle. There's also a trend to replace hydraulic and mechanical devices with smart electronic devices. Energy efficiency is on the rise due to this new effort, but designers now need to manage these added heat loads. The quantity of heat sources continues to climb; thus, they need to be spread out over most of the vehicle's limited volume.

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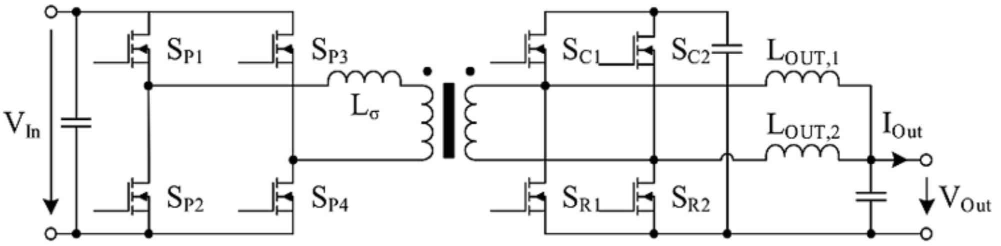

3. Shown is the circuit topology of the GaN active-clamp phase-shifted full bridge. *(Image from Reference 2)*

Cooling techniques will significantly improve power density. Some key areas within the vehicle have various levels of cooling:

- Level 1 applies to heat spreading in the semiconductor package, where today's technologies use copper, copper/tungsten, and copper/moly heat spreaders.
- Level 2 applies to heat transfer/spreading from the device package to the chassis. Modern technologies use copper and aluminum heat spreaders.
- Level 3 applies the transporting of heat from the chassis to the system heat exchanger. This method uses forced air flow as well as pumped liquid loops.
- Level 4 applies to heat dissipation through the system heat exchanger. Modern technologies enable air-cooled heatsinks and radiators.

The "level of cooling" method in an automobile typically uses a heat spreader, temperature control, and heat transport. These advanced thermal-management methods, such as HiK plates and VCHPs, have passed laboratory development stages and are being deployed in mission-critical military and space systems.

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JAMES MORRA | Senior Editor

How Much Longer Will It Take to Fix the Chip Shortage?

The global chip shortage is entering its second year, and there are a lot of variables complicating the recovery.

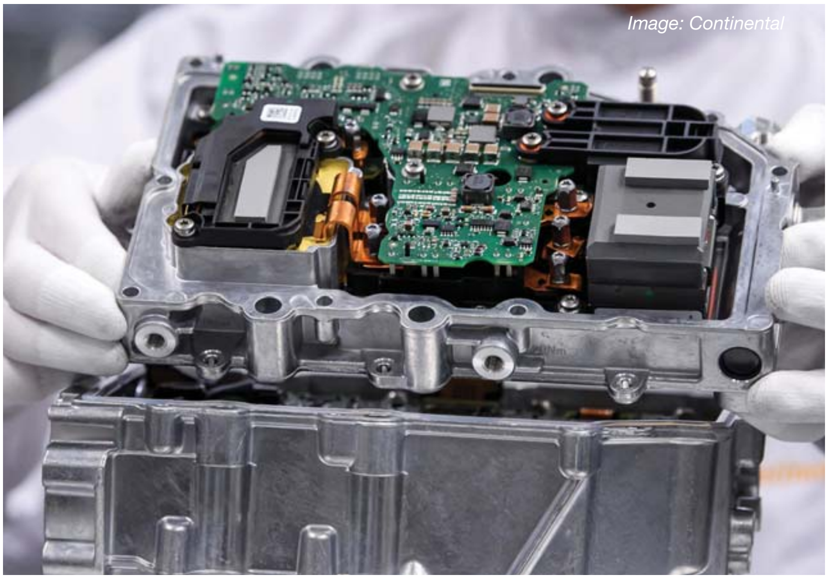


Image: Continental

The global chip shortage, now dragging into its second year, has shaken the electronics industry to its core, crimping the world's ability to build everything from cars to consumer goods and raising prices.

Even companies that produce chips are being hit—at least indirectly—by sourcing problems, adding to the upheaval facing the semiconductor industry as it attempts to solve the chip shortage.

Applied Materials, which makes the high-end machinery used to manufacture chips, said late last year it has been unable to get its hands on some of the chips used in its products due to snags in its supply chain. Demand for the analog, power, and logic chips it uses is outstripping supply. This exposes the company to some of the same supply-chain issues affecting other areas, such as autos.

"That is the definition of a vicious cycle," said Chris Richard, supply-chain expert and principal analyst at Deloitte, where he covers the semiconductor market. "You can't make more equipment to put in factories because you don't have a chip that gets made in the same factory."

The chip shortage is complicated even more by the fact that electronic devices use a very wide range of components that have varying levels of availability, said Richard. It only takes a single part on a bill of materials (BOM) being out of stock or on allocation to halt production. At Applied Materials, executives said that out of the thousands of components used in its tools only 10 were giving its suppliers trouble.

Part of the problem is that semiconductor equipment makers are fighting over the same finite supply of chips as companies in other sectors. The reality is that no one is getting their hands on ample supplies.

Where Do Things Stand?

The chip industry is cyclical, driven by fluctuating demand for chips used in consumer goods and other sectors that follows the ebb and flow of the economy, with the market swinging from gluts to shortages. But the pandemic sent a shock through every part of the semiconductor ecosystem when it hit in 2020.

The virus shut down factories where chips are made, packaged, and tested. It also took a toll on other parts of the supply chain, such as sourcing silicon wafers, substrates, and other raw materials, straining supplies. The complex logistics that companies use to move chips around the globe and ship finished stock to customers was also hit, leading to tighter inventories that companies are at pains to replenish.

"We aren't even close to being out of the woods," U.S. Commerce Secretary Gina Raimondo said in January. "The semiconductor supply chain is very fragile and it's going to remain that way until we can increase chip manufacturing."

In January, the U.S. Department of Commerce published a report using a survey of over 150 companies, including nearly every major chip maker as well as automotive, industrial, and medical companies that have been hit hard. The report noted that median inventory levels of key chips at these companies fell from 40 days in 2019 to five days in 2021, leaving them exposed to even the slightest extra setback.

"The current global chip shortage rivals only a few of the past imbalanced markets," said Graham Scott, head of global procurement at Jabil, in a blog. "However, it's unique in the breadth of product families."

Widespread shortages are holding companies back from rebuilding inventories, he said. Companies tend to place chip orders several months ahead of time, but fulfillment is taking longer than usual. Electronics companies are wrestling with lead times of more than 28 weeks for virtually every type of chip, said Scott.

Many microcontrollers and logic chips are in worse shape, on allocation or with lead times of 52 weeks.

What Is Taking So Long?

The semiconductor industry continues to dig out of the deep hole created by booming demand for chips.

Global sales of semiconductors soared to a record $556 billion in 2021, up more than 26% year over year, according to the Semiconductor Industry Association (SIA).

Companies have been ordering more chips than they actually need to shore up stocks, squeezing capacity and driving up prices, said Masatsune Yamaji, semiconductor analyst at Gartner.

To discourage double-ordering, many chip makers are requiring customers to lock themselves into long-term, non-cancelable orders. Even those vendors have their hands full, though. Broadcom has said that it is fully booked through the end of 2022 and into early 2023.

Semiconductor firms are shifting chip factories into higher gear in response to the supply constraints. Most companies run chip fabs at around 80% of their maximum capacity, leaving time to shut down parts of the plant for maintenance and upgrades. But robust demand for chips is keeping capacity utilized at a high rate: an average level of between 90% and 95% for more than a year at this point.

But as supply chains remain in turmoil, the world is piling the pressure on the semiconductor industry. Chip firms are, in turn, moving to beef up capacity at fabs and develop new technologies.

But adding production capacity for chips that the world is lacking is difficult or impossible in the short term. Expanding the capacity of a fab takes up to a year and a half to install, test, and then qualify the equipment.

According to Deloitte's Richard, companies plan to add production capacity throughout this year. But he warned that the chip shortage will likely continue to fall short of demand despite the production build-up.

Jan-Philipp Gehrmann, head of global marketing for the advanced analog business at NXP, said the auto industry has been affected by component sourcing issues more than any other sector, and it learned too late that it is impossible to fix it with the flip of a switch.

"What auto makers were unfamiliar with was the process of how chips are made and the complexity behind that," said Gehrmann. While it usually only takes a single day to manufacture a vehicle from start to finish, the average chip has a front-end production cycle of 12 to 24 weeks. Additionally, it takes 4 to 8 weeks on the back-end to package and test it before the finished chip is finally shipped to the customer.

"The fact that producing a single chip can take six months was hard to understand," said Gehrmann.

When Will It Finally End?

Unless there is a sudden drop in demand, the chip shortage will not be over anytime soon, analysts said.

Most industry executives warn the shortage will likely not ease before the second half of 2022, with some products continuing to be delayed by a deficiency of chips in 2023.

"Demand remains robust across most system markets, but inventory levels by the middle of the year and slower economic activity in the second half could be what ultimately eases the constraints," said Mario Morales, VP of semiconductor research at IDC, in a January report.

Although the chip shortages are broad-based, the companies feeling the pain most acutely are those trying to buy chips based on long-lasting legacy nodes, specifically microcontrollers used in cars as well as a wide range of analog and power management ICs.

The industry is warning these constraints will not be resolved for some time. GlobalFoundries, the largest U.S.-based contract chip maker, said that wafer capacity for its more mature nodes is sold out through 2023 even as it plans to boost its production capacity by 50% in the same span.

Varying levels of availability also mean different industries and even companies in the same industry will regain access to components at different rates, said Glenn O'Donnell, VP of research at consulting firm Forrester, in a 2021 report. He noted widespread shortages could soften for some sectors, such as PCs and consumer electronics, in 2022, while weighing on others, such as cars.

The route out of the global chip shortage is complicated by the supply chain's vastness, which leaves it exposed to unpredictable events, according to Avnet VP of global supplier development Peggy Carrieres.

The components in an average chip, from the intellectual property used to design it to the blank wafers used to build it, can travel 25,000 miles and cross over 70 international borders before a customer gets its hands on the final chip, as stated in a report released by the Global Semiconductor Alliance in 2020.

A disruption at any point in the supply chain—caused by a once-in-a-century pandemic, a massive fire at a fab, or sanctions imposed as part of a trade war—can snag production, straining supply and hiking prices.

What's Being Done About It?

Once the world falls into a chip shortage, little can be done to address it in the short term, at least on the part of the semiconductor industry. Besides boosting production rates, chip makers have started hiking prices and adjusting their order books.

The last time the world went through such a supply shock was more than a decade ago in the wake of the global financial crisis, said Richard. If what happened then is any model for the future, he sees today's shortage lasting at least another year.

But what stands out about the shortage of 2020 and 2021 is that companies are responding by building in more excess capacity to get ahead of future demand, he said. Every company fears overreacting to a shortage. The risk is by the time fabs come online, the demand that spurred companies to build them in the first place will be over, leaving them with some of the most expensive unused capacity in the world.

But the semiconductor industry is loading up its bets that underlying demand for chips has permanently increased. "There is definitely more—and substantial—capacity coming online," said Richard.

Many of the world's largest semiconductor companies are racing ahead with ambitious plans to build U.S. plants. Intel, Samsung, and TSMC have announced projects in Ohio, Arizona, and Texas, in recent years, with a minimum total investment of $69 billion. Intel said investment at its manufacturing site in Ohio could grow to $100 billion over the next 10 years. But the plan hinges on it getting government aid.

TI announced plans to invest up to $30 billion in a new manufacturing site in Texas by 2025.

Companies are being lured to the U.S. by the prospect of massive subsidies. The U.S. has proposed $52 billion in funding to boost the country's self-sufficiency in chips, as part of the America COMPETES Act.

But none of these investments will alleviate today's chip shortage, as most of the fabs are still years out. For now, though, customers are going to take what they can get.

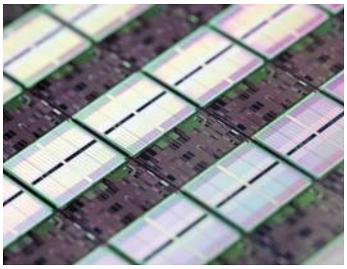
ElectronicDesign 70 YEARS

Special Report

JAMES MORRA | Senior Editor

U.S. Warns Chip Shortage to Last Into Late 2022 as Inventories Dip

The Commerce Department said an industry survey showed mature nodes of microcontrollers, optoelectronics, and analog chips reeling from acute supply shortages.



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U.S. manufacturers are not out of the woods when it comes to a global chip shortage that has snagged the production of everything from cars to medical devices, the Commerce Department said in a report.

A summary of the report released in January indicated there is still "a major supply and demand mismatch" for semiconductors. The report, based on survey results compiled from about 150 companies in the supply chain, said demand remains very high, running up to 20% above pre-pandemic levels, and chip suppliers are struggling to keep up.

U.S. manufacturers are now down to less than a week of inventory for key chips, which are defined as 160 components that companies identified as being the most challenging to buy, the report cautioned.

In 2019, companies typically had 40 days of inventory on hand for key chips, said the Commerce Department. Now, inventory levels for the same chips have dipped to a median of fewer than five days, the report warned. Inventories are even more depleted in critical sectors such as automotive and medical devices.

The agency said it is also looking into allegations of price gouging, specifically "the unusually high prices" for chips sold by electronics distributors that act as intermediaries between chipmakers and consumers.

"Fragile" Supply Chain

U.S. companies don't see the shortage being solved in the next six months—at least.

Commerce Secretary Gina Raimondo said the report highlighted the need for the U.S. to pass federal subsidies to help rebuild its manufacturing base for semiconductors and address the country's over-dependence on chip imports.

"It is both an economic and national security imperative to solve this crisis," she said in a summary of the survey results. "It is essential that Congress move swiftly to pass the President's proposed $52 billion in chips funding as soon as possible."

The chip drought has gripped the electronics segment for more than a year now, brought on by booming demand for electronic goods such as personal computers and game consoles. Snags in the supply chain are adding to delays. Automakers are unable to procure parts for otherwise idle factories, while the scarcity of components has also tangled production of medical devices and consumer goods.

The dearth of chips has forced companies to fight over the production capacity at chip foundries, largely located outside the U.S., which are overloaded with orders, and in some cases sold out for the foreseeable future.

The chip industry depends on a sprawling global supply chain that can be upended by even short delays or disruptions in one region, leaving holes in the supply chain other regions are generally not equipped to fill. Most U.S. chip firms are completely, or for the most part, fabless, outsourcing production overseas. The U.S. only accounts for approximately 10% of global chip output, a drop from more than 35% in 1990.

Most industry executives have warned that the shortage will not ease until the second half of this year. Some products may continue to be delayed by a scarcity of components into 2023 and 2024.

Procurement challenges with a single part—even one that costs less than a dollar—can leave consumer goods such as cars and game consoles sitting unfinished until it becomes available. Any disturbance in overseas production, like a coronavirus outbreak, a natural disaster, a fire at a fab, or even political instability, could lead to shutdowns in key U.S. industries, putting American jobs at risk, according to the report.

"The semiconductor supply chain remains fragile," the report said.

Supply Bottlenecks

The report is the result of a request for information (RFI) put out by the Commerce Department last year. The agency asked chip companies to share details on their products and customers to help get a better handle on how the pandemic has affected the chip supply chain and identify bottlenecks.

Raimondo said the Commerce Department heard back from almost every major semiconductor vendor and from buyers in a wide range of sectors, both inside and outside the U.S., including major car makers.

The primary bottleneck is wafer production capacity, which she said has no obvious short-term solution.

The vast majority of fabs are running at a rate between 90% and 95% of their maximum production capacity, up from levels of between 85% and 90% before the pandemic. Such a rapid rate of production is unusual because modern chip-making tools need regular upkeep that takes them out of commission. Chip makers also periodically shut down part of their factories to upgrade equipment.

A summary of the report highlighted the chips experiencing the most acute supply shortages. The worst deficiencies are in microcontrollers widely used in cars and other areas such as medical devices. These chips depend on mature nodes, e.g., 40 nm, that are generations behind the state-of-the-art in chips.

A diverse range of analog chips, including power-management ICs, radio-frequency ICs, display-driver ICs, and image sensors are also scarce due to a dearth of production capacity at 90 nm and 130 nm, among other nodes. Optoelectronics are another weak spot in the supply chain, said the Commerce Department.

Even though these special-purpose chips are key components in cars and other goods, companies are reluctant to invest in production capacity at mature nodes because they are closer to obsolescence.

The Commerce Department said substrates that connect a die to a circuit board have also become a key chokepoint in the supply chain. Electronics companies trying to procure capacitors, diodes, and other tiny components used to assemble their devices are still hitting obstacles, too.

Raw materials ranging from blank silicon wafers that serve as the fundamental building blocks of chips to plastic resins used in packages that house finished chips are also suffering supply woes.

Moreover, there are widespread delays in testing and packaging chips before they're ready to ship out.

Private and/or Public

The Biden administration hoped to take a more active role in addressing the chip shortage, including better transparency in the supply chain. But the new report released by the Commerce Department highlighted a lack of short-term solutions to the crisis. The broader goal is to boost domestic production.

The report concluded that private companies are "best positioned" to resolve the chip supply crisis in the short term by increasing production and redesigning products in a way that favors readily available ICs.

Ford, GM, and other auto makers are taking steps to untangle their globe-spanning supply chains and forging more direct relationships with foundries to secure component supplies for the long term.

Unprecedented demand for chips has pushed companies to invest aggressively in fabs, both in the U.S. and other locations around the world. While some companies plan to ramp up new production later this year, many other fabs are years out, offering no short-term relief to electronics companies lacking chips.

Intel announced a new $20 billion manufacturing site outside Columbus, Ohio, that it hopes to build into the world's largest chip manufacturing site. The first two factories are expected to come online in 2025.

Samsung and TSMC also announced U.S. expansion plans that are years from making a difference in the supply chain. Plus, most of these capital investments are in state-of-the-art microprocessors that are not in short supply.

While Intel and other chip-making giants focus on building fabs, Raimondo said she wants to encourage chip producers and buyers to share more information to reduce the risk of supply-demand mismatches. ed

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THIS ARTICLE IS PART OF Tech-Xchange: Chip Shortages and Counterfeits. *www.electronicdesign.com/magazine/50421*

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ABHILASHA KAWLE | Senior Analog Design Engineer, Analog Devices
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CTSD Precision ADCs (Part 1): Improving Signal-Chain Design Time

CTSD ADCs bring out architectural benefits and simplify signal-chain design to reduce solution size and help achieve faster time to market. This article series explains the benefits of CTSD ADCs and how to adapt them to precision medium-bandwidth apps.

In many digital processing applications and algorithms, the demand to have better resolution and precision for all converter technologies has increased over the last two decades. The limited resolution/precision of analog-to-digital converters (ADCs) was enhanced by using an external digital controller that would extract and deliver more precise results using software techniques such as averaging and optimized filtering schemes.

To reduce extensive postprocessing at the digital microcontroller or DSP, designers could use a high-performance precision ADC. This would reduce optimization time at the digital side, and a lower-cost microcontroller or DSP also could be considered. The applications and markets for precision ADCs are widespread:

- **Industrial instrumentation:** vibration analysis, temperature/pressure/strain/flow measurements, dynamic signal analysis, acoustic analysis
- **Medical instrumentation:** electrophysiology, blood analysis, electrocardiogram (EKG/ECG)
- **Defense applications:** sonar, telemetry
- **Test and measurement:** audio test, hardware-in-loop, power quality analysis

The analog input signal to be processed by an ADC could be a sensor signal with voltage, current output, or a feedback control-loop signal with bandwidth ranging from dc to a few hundred kilohertz. The ADC digital output format and rate depend on the application and postprocessing required by the following digital controller.

In general, signal-chain designers follow the Nyquist sampling theorem and program the ADC's output data rate (ODR) for the digital controller to be at least twice the input frequency. Most ADCs provide the flexibility to tune the ODR based on the signal frequency band of interest.

For currently available ADCs, several signal-conditioning stages are involved before the ADC can interact with the input signal. Signal-conditioning circuits with stringent requirements need to be designed and tailored around specific and individual ADC technologies to ensure that ADC datasheet performance can be achieved.

A signal-chain designer's job doesn't stop after the selection of the ADC. Considerable time and effort are often required to design and fine-tune this surrounding periphery. Analog Devices provides a high level of technical support in the form of design simulation tools and models to overcome most of these inherent design challenges.

A New Approach: Easing the Design Journey with CTSD Architecture

Continuous-time sigma-delta (CTSD) architecture, which has been predominantly used in audio and high-speed ADCs, is being tailored for precision applications to achieve the highest precision while leveraging its unique signal-chain simplification properties. The advantages of this architecture remove the burdens involved with designing the periphery.

To illustrate the simplification that CTSD ADC technology brings to the signal chain, this article highlights some of the key challenges involved in incumbent signal-chain design for general applications. It also shows how CTSD ADCs ease these challenges.

So, let's start with a few design steps involved in incumbent signal chains, with the very first task being the selection of the right ADC to best fit the targeted application.

Step 1: Selecting the ADC

When selecting from the wide range of available ADCs, important considerations are resolution and accuracy, signal bandwidth, ODR, signal type, and the range to be processed. Generally, in most of the applications, digital controllers require their algorithms to process amplitude, phase, or frequency on the input signal.

To accurately measure any of the previous factors, the errors added in the process of digitization need to be minimal. The major errors and their corresponding measurement terminology are detailed in the *table* and explained in further detail in ADI's Essential Guide to Data Conversion.

The performance metrics in the *table* are related to signal amplitude and frequency, and they're generally termed as ac performance parameters.

For dc or near dc applications, such as power metering, that deal with 50- to 60-Hz input signals, ADC errors like offset, gain, INL, and flicker noise would have to be considered. These dc performance parameters also require a certain level of temperature stability relating to an application's intended use.

ADI has a wide range of high-performance ADCs to meet system requirements of several applications, be they precision-based, speed-based, or based on a restricted power budget. Just comparing one set of ADC specifications to another isn't the way to choose an ADC. The overall system performance and design challenges must be considered, and that's where the choice of ADC technology or architecture comes into play.

Two broad classifications of ADC architectures are traditionally preferred. The most popular is the successive-approximation-register (SAR) ADC, which follows the simple Nyquist theorem. It states that a signal can be reconstructed if sampled at twice its frequency. The advantages of SAR ADCs are excellent dc performance and small form factors with low latency and power consumption scaling with ODR.

ADC Errors and Performance Metrics

ADC Error		Associated Measurements in Datasheets
1	Thermal and quantization noise	Signal-to-noise ratio (SNR), dynamic range (DR)
2	Distortion	Total harmonic distortion (THD), intermodulation distortion (IMD)
3	Interference	Crosstalk, alias rejection, power-supply rejection ratio (PSRR), common-mode rejection ratio (CMRR)
4	Magnitude and phase error	Gain error, magnitude, and phase droop at frequency of interest
5	Delay from ADC input to final digital output	Latency, settling time

The second technology choice is a discrete-time sigma-delta (DTSD) ADC, which works on the principle that the greater the number of samples, lesser is the information lost. So, the sampling frequency is much higher than the stated Nyquist frequency, a scheme referred to as oversampling. Another advantage from this architecture is that the errors added due to sampling are minimized in the frequency band of interest. Because of this, DTSD ADCs have both excellent dc and ac performance but a higher latency.

Figure 1 shows an illustration of the typical analog input bandwidths of both SAR and DTSD ADCs, with some popular product choices at various speeds and resolution. The Precision Quick Search

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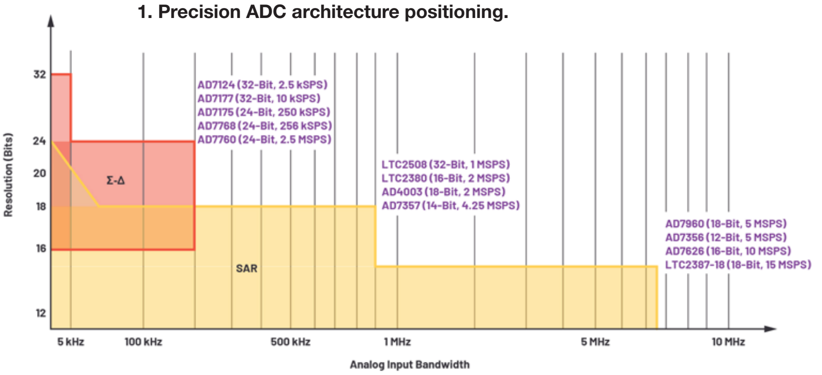


feature also can be referenced to help in your choice of ADC.

In addition, a new class of precision ADCs are now available. Based on CTSD ADCs, they're on par with the performance of DTSD ADCs but are unique with regard to simplifying the entire signal-chain design process. The challenges highlighted in the next few design steps of an incumbent signal chain can be addressed by this new ADC family.

Step 2: Interfacing the Input to the ADC

Sensors whose outputs are to be processed by the ADC may have very high sensitivity. Designers must have a good understanding of the ADC input structure to which the sensor will be interfaced to ensure ADC errors don't mask or distort the actual sensor signal.

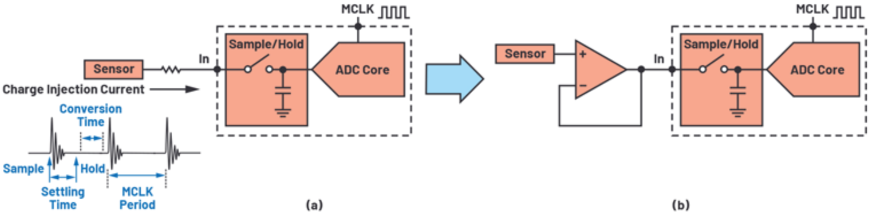
In conventional SAR, DTSD ADCs, the input structure is known as the switched capacitor sample-and-hold circuit *(Fig. 2).* At every sampling clock edge, when the sample switch changes its ON/OFF state, finite current demand needs to be supported to charge or discharge the hold capacitor to a new sampled input value. This current demand must be supplied by the input source, which, in our case of discussion, is the sensor.

In addition, the switch itself has some on-chip parasitic capacitors that inject some charge back onto the source, which is called charge injection kickback. This added error source also needs to be absorbed by the sensor to avoid corruption of the sensor signal.

Most of the sensors are incapable of providing such a magnitude of currents, indicating that they fall short of driving switching circuitry directly. In a different scenario, say even if a sensor can support these current demands, the sensor's finite impedance would add an error at the ADC input.

The charge injection current is a function of input; this current causes an input dependent voltage drop across the sensor impedance. As shown in *Figure 2a,* the input of the ADC is then in error. One solution to solve these issues is to place a driving amplifier between the sensor and ADC *(Fig. 2b).*

Now we need to set the criteria for this amplifier. First and foremost, the amplifier should support the charging current and absorb the charge injection kickback. Next, this amplifier's output needs to be fully



2. Switched capacitor charge injection kickback into the sensor (a) and isolating the kickback effect with an input buffer (b).

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settled at the end of the sampling edge so that the ADC samples input without added errors. This means the amplifier should have the capability to provide instantaneous current steps that map to having a high slew rate. Further, it should provide a fast settling response to these transient events, which maps to having high bandwidth. As the sampling frequency and resolution of the ADC increases, meeting these requirements becomes critical.

The big challenge for designers, especially those who work with medium-bandwidth applications, is to identify the right amplifier for the ADC. As indicated earlier, ADI provides a set of simulation models and precision ADC driver tools to ease this step, but for a designer, it's an added design step to achieve the datasheet performance of the ADC.

Some of the new age SAR and DTSD ADCs have mitigated this challenge by using novel sampling techniques to completely reduce the transient current demand, or by having an integrated amplifier. But either solution limits the range of signal bandwidth or penalizes ADC performance.

The CTSD ADC advantage: CTSD ADCs address this challenge by providing an easy-to-drive resistive input instead of a switched capacitor input. This shows that there are no hard requirements of high-bandwidth, large-slew-rate amplifiers. If sensors can directly drive this resistive load, they can be directly interfaced to a CTSD ADC. Otherwise, any low-bandwidth, low-noise amplifier could be interfaced between a sensor and a CTSD ADC.

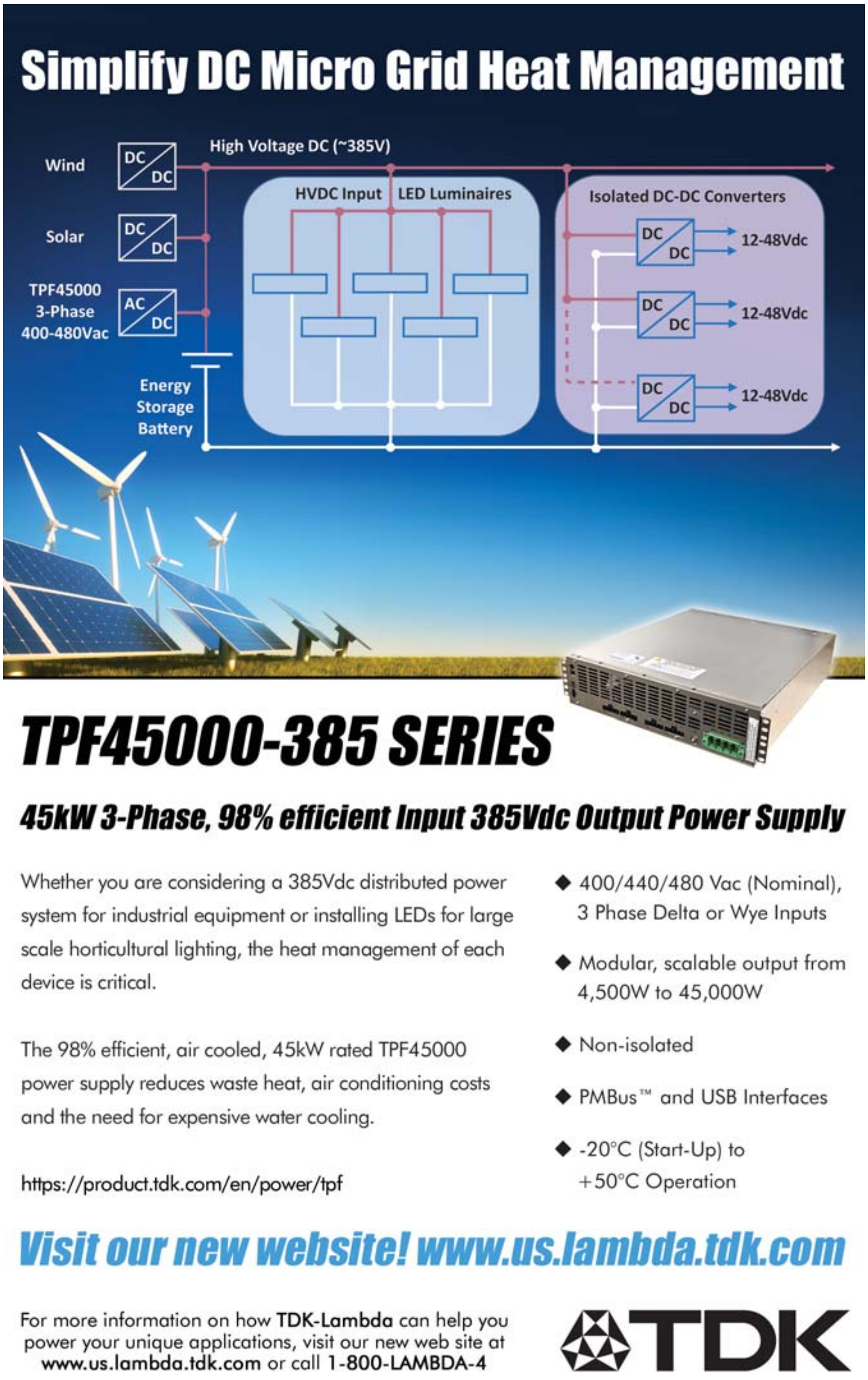
Step 3: Interfacing the Reference to the ADC

The challenge involved with interfacing to a reference is similar to input interfacing. The reference input for conventional ADCs also is a switched capacitor. At every sampling clock edge, the reference source needs to charge the internal capacitors, thus demanding large switching current with good settling time.

The reference ICs available can't support large switching current demand and have limited bandwidth. The second interfacing challenge is that noise from these references is large in comparison to an ADC's noise. To filter this noise, a first-order RC circuit is used.

On one hand, we're band-limiting the reference for noise, while on the other hand, we're demanding fast settling time. These are two opposing requirements to satisfy. For this reason, a low-noise buffer is used to drive the ADC reference pin *(Fig. 3b)*. Based on the sampling frequency and resolution of an ADC, the slew rate and bandwidth of this buffer is decided.

Again, like with our precision input driver tools, ADI has tools to simulate



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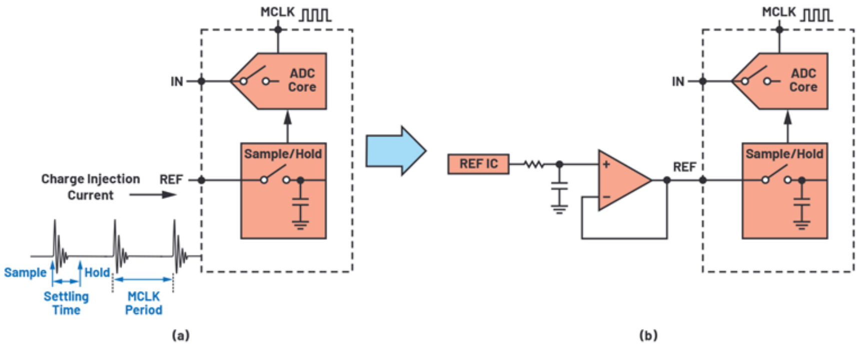
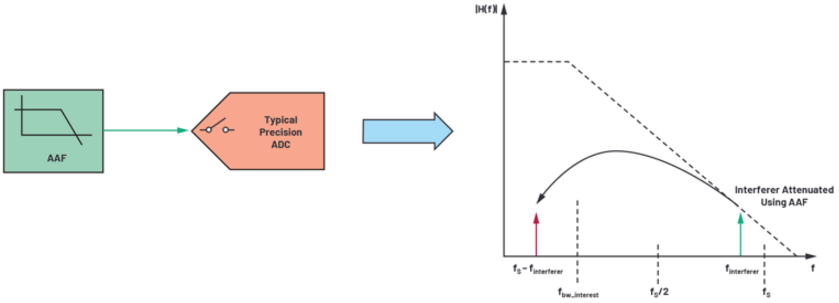
TDK



3. Switched capacitor charge injection kickback into the reference IC (a) and isolating the kickback effect with a reference buffer (b).



4. Use of an antialiasing filter to mitigate the effect of aliasing on in-band performance.

and select the correct reference buffers for an ADC. And similar to input, some of the new age SAR and DTSD ADCs also have the option of an integrated reference buffer, but they come with performance and bandwidth limitations.

The CTSD ADC advantage: This design step can be completely skipped by using a CTSD ADC. It provides a new, easy option for driving a resistive load that doesn't require such a high-bandwidth, large-slew-rate buffer. The reference IC with low-pass filter can be directly interfaced to the reference pin.

Step 4: Making a Signal Chain Immune to Interference

Sampling and digitizing a continuous signal causes loss of information, which is termed as quantization noise. The sampling frequency and number of bits set the performance limit for an ADC architecture.

After addressing the performance and interfacing challenges for the reference and input, the next struggle is to address the issue of high-frequency (HF) interferers/noise folding into the low-frequency bandwidth of interest. This is termed aliasing or folding back. These reflected images of the HF or out-of-band interferers into the bandwidth of interest cause signal-to-noise ratio (SNR) degradation.

To mitigate the effect of foldback, one solution is to use a type of low-pass filter known as an antialiasing filter (AAF). It attenuates the unwanted interferer's magnitude such that when this attenuated interferer folds back in-band, the desired SNR is maintained. This low-pass filter is generally incorporated with a driver amplifier *(Fig. 4)*.

When designing this amplifier, the biggest challenge is finding a balance between faster settling and the low-pass filtering requirements. An added challenge is that this solution must be fine-tuned for each application requirement, which limits the adoption of single platform design across various applications. ADI has many antialiasing filter tool designs to help designers overcome this challenge.

The CTSD ADC advantage: This immunity to interference is addressed by the inherent alias rejection property of the CTSD ADC itself, a feature that's unique only to CTSD ADCs. The AAF isn't required for ADCs with this technology. Therefore, we would be one step nearer to directly interfacing a CTSD ADC to a sensor without much effort.

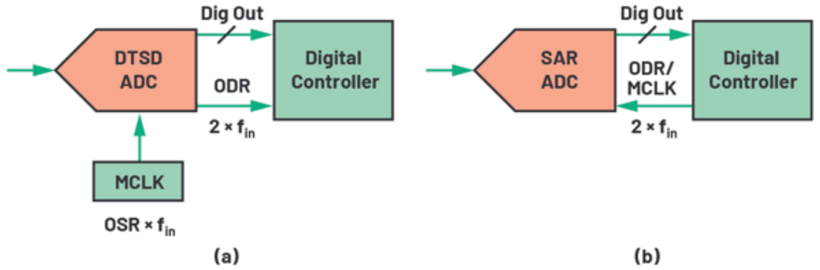
Step 5: Selecting the ADC Clock Frequency and the Output Data Rate

Next, let's discuss the clock requirements for the two classes of traditional ADCs covered earlier *(Fig. 5)*. The DTSD is an oversampled ADC, which means that the ADC is sampled at a higher-than-Nyquist sampling rate. But giving ADC oversampled data directly to the external digital controller implies we're overloading it with lots of redundant information. In an oversampled system, the core ADC output is decimated using on-chip digital filters that enable the final ADC digital output at a lower data rate, which is usually twice the signal frequency.

For DTSD ADCs, the designer needs to plan for the provision of the high-frequency sampling clock for the core ADC and program the desired output data rate. The ADC will give a final digital output at this desired ODR and the ODR clock. A digital controller uses this ODR clock to clock in the data.

Next, we address the clock requirements of SAR ADCs, which usually follow the Nyquist theorem. Here, the sampling clock of the ADC is provided by a digital controller; the clock also acts as an ODR. But there's less flexibility in the timing of this clock—the sample-and-hold timing needs to be well-controlled to get optimum performance from the ADC, which also indicates that the timing of the digital output needs to be well-aligned with these requirements.

In understanding the clock requirements of both architectures, we see that the ODR is coupled to the sampling clock of the ADC. This is a limitation in many systems where ODR can drift or change dynamically, or needs to be tuned to the analog input signal frequency.



5. Clocking requirements in a DTSD ADC (a) and SAR ADC (b).

The CTSD ADC advantage: The CTSD ADC couples with a novel asynchronous-sample-rate converter (ASRC) that resamples the core ADC data at any desired ODR. The ASRC also enables designers to granularly set the ODR at any frequency and go beyond the age-old restriction of limiting ODR to a multiple of sampling frequency. The frequency and timing requirements of ODR are now purely a function of the digital interface and completely decoupled from the ADC sampling frequency. This feature eases digital isolation design for signal-chain designers.

Step 6: Interfacing with the External Digital Controller

Traditionally, there are two types of data interface modes for ADCs to communicate with the digital controller. One involves the ADC acting as a host, providing the digital/ODR clock, and deciding on the clock's edges for the digital controller to clock-in the ADC data. The other type is hosted mode (receiver mode), in which the digital controller is the host, provides the ODR clock, and decides the clock edges at which the ADC data will be clocked in.

Continuing from Step 5, if a designer selects a DTSD ADC, the ADC acts as host for the following digital controller since the ADC provides the ODR clock. If a SAR ADC is selected, the digital controller needs to provide the ODR clock, implying SAR ADCs are always configured as hosted peripherals. So, the obvious limitation is that, once an ADC architecture is chosen, the digital interface is restricted to being in host mode or hosted mode. Currently, there's no flexibility in choosing the interface regardless of ADC architecture.

The CTSD ADC advantage: The novel ASRC that's been coupled with a CTSD ADC enables designers to independently configure the ADC data interface mode. This opens up a whole new opportunity for applications where high-performing ADCs can be configured in any mode suitable for the digital controller of the application irrespective of ADC architecture.

Putting It All Together

The building blocks of a traditional signal chain with an analog front end (AFE) comprising an ADC input driver, an alias rejection filter, and a reference buffer that can be drastically simplified by a CTSD ADC *(see Fig. 9 of online article at https://electronicdesign.com/21214650)*. One example of a signal chain with a DTSD ADC requires significant design effort to fine-tune and derive the datasheet performance of the ADC *(see Fig. 10a of online article at link above)*. To ease the customer journey, ADI has reference designs that can be reused or retweaked for various applications for these ADCs.

A signal chain with a CTSD ADC and its simplified AFE is easier to design because its ADC core doesn't have a switch capacitor sampler at the input and reference *(see Fig. 10b of online article at link above)*. The switch sampler is moved to a later stage of the ADC core, making the signal input and reference input purely resistive. This results in an almost nonsampling ADC, making it a class of its own.

Also, the signal transfer function of this class of ADCs mimics the antialiasing filter response, which means it inherently attenuates noise interferers. With CTSD technology, the ADC is reduced to an easy plug-and-play component.

In summary, CTSD ADCs simplify signal-chain design while achieving a system solution with the same performance level as a traditional ADC signal chain, along with offering the following advantages:

- Provides alias-free, low-latency signal chain with excellent channel-to-channel phase matching.
- Simplifies the analog front end with no added step of selection and fine-tuning of high bandwidth input and reference driver buffers, enabling higher channel density.
- Breaks barrier of ODR being a function of the sampling clock.
- Gives independent control of interface to external digital controller.
- Improves the signal-chain reliability rating, which is a direct result of periphery component reduction.
- Shrinks size and has a 68% reduction in BOM, leading to faster time to market for customers.

Parts 2, 3, and 4 of this series explain the concepts of CTSD ADCs and ASRCs in greater detail, highlight the signal-chain advantages, and Part 5 will conclude with leveraging the features of the new AD7134 *(visit https://electronicdesign.com/21216291)*.

TO READ this article in its entirety, go to https://electronicdesign.com/21214650.

THE AUTHORS would like to thank product applications engineer Ren Naiqian and product marketing engineer Mark Murphy for their useful insights in writing this article.

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ElectronicDesign 70 YEARS

Design Feature

JAMES MORRA | Senior Editor

Staying a Step Ahead of the Global Chip Shortage

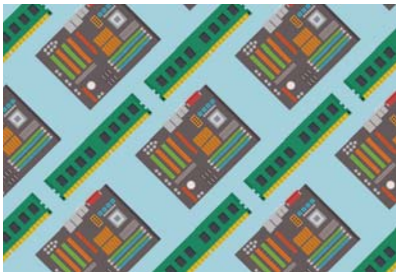

Image: ShowVector, Dreamstime

Engineering teams can take steps before and during the development process to ensure they're in the best position to navigate a new era of supply-chain issues.

An out-of-stock component can be the bane of even the best electronic design. As the global chip shortage drags on into its second year, access to electronic components has become a huge challenge for engineers. More challenges are likely ahead as everyone competes over a finite supply of chips.

But engineering teams can take steps before and during the development process to make sure they are in the best position possible to navigate a new era of supply-chain issues, according to industry experts.

They said the path to solving component sourcing issues means working closely with both internal and external sourcing and manufacturing teams. When engineers select components and suppliers without input from procurement and sourcing departments, they can overlook more realistic options or end up scrambling for parts or rushing to onboard suppliers, which can add to costs or lead to product delays.

"Uncertainty and complexity are constants in business today. But global manufacturers have more control of managing their electronics sourcing risk than they may realize," said Steve Flagg, CEO of Supplyframe, in a 2020 report. "Eighty percent of the lifetime risk and cost of a typical hardware product is decided during that product's initial design," he said. "That's where the disconnect often exists."

Engineering teams also need to build more flexibility into their designs, industry experts said, making it easy to swap out scarce components with secondary sets of chips without sacrificing product quality.

Pain Points

Supply-chain issues are already heaping more pressure on engineers, as companies rely on them to review bills of materials (BOM) for availability as well as to validate, specify, and qualify replacement parts. Electronics makers are working with a wider range of vendors, including spot brokers, to try to respond more quickly to supply issues, with engineers being enlisted to help vet secondary suppliers.

But the chip shortage influences more than just where engineers seek parts for their designs. It also impacts how they design products, according to a report by U.S.-based electronics distributor Avnet, citing a survey of more than 500 engineers. As lead times worsen and prices rise, over 60% of engineers said that they are building products based more on the availability of components than their preference.

Most engineers faced with out-of-stock components or those with long lead times are swapping them out with pin-to-pin replacements that have different specs (53%) or, if possible, drop-in replacements (49%).

Others (55%) have been forced to redesign products around new sets of components.

Co-op Mode

For years, engineers have been encouraged to build products using a "design for manufacturing" (DFM) strategy, designing a product specifically for ease of manufacturing, with the goal of keeping costs low.

But design for manufacturing depends on being able to procure all of the necessary components. In an age of widespread chip shortages, industry experts say engineering teams need to take things to the next level. Ted Pawela, chief ecosystem officer at Altium, a leading vendor of electronic design software for circuit boards (PCBs), urged engineers to use more of a "design with manufacturing" approach.

"What it means is that rather than completing a design and only then receiving manufacturing feedback, you get that feedback as your design progresses," he said, reducing the risk of re-designs.

Altium last month rolled out a software tool called Altimade to assist companies trying to take the next step. Available on its Altium 365 cloud platform and connected to MacroFab's manufacturing platform, Altimade promises to speed up the prototyping process by uniting design, manufacturing, and sourcing data and experts all in the same dashboard. That opens the door for them to work together on designs.

Using Altimade, customers get access to continuously updated component and manufacturing prices and lead times. The insights help them understand the implications of design decisions and react to unplanned events such as natural disasters. Altium said Altimade also allows its customers to order a PCB without leaving the design environment. Orders are filled by MacroFab's network of manufacturers.

TO READ THE ARTICLE in its entirety, please go to https://electronicdesign.com/21235575.

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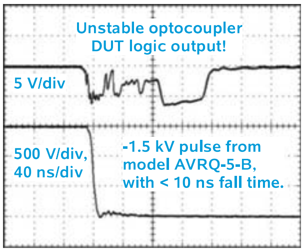

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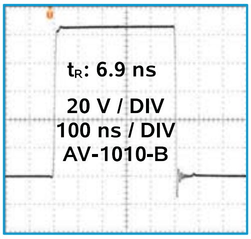

AV-1015-B:	±50V, 10 MHz, 20 ns - 10 ms, 10 ns rise
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AV-1011B1-B:	±100V, 100 kHz, 100 ns - 1 ms, 2 ns rise
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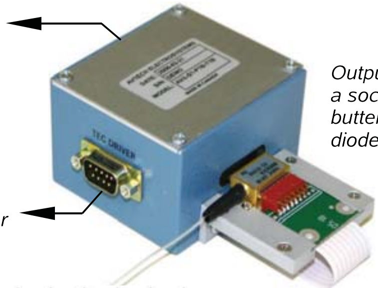
Nanosecond Laser Diode Drivers With Butterfly Diode Sockets



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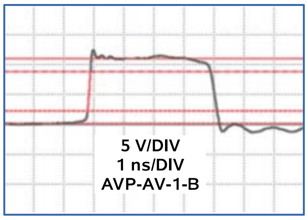

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20 V	200 ps	10 MHz	AVMR-2D-B
40 V	150 ps	1 MHz	AVP-AV-HV3-B
50 V	500 ps	1 MHz	AVR-E5-B
100 V	500 ps	100 kHz	AVR-E3-B
100 V	300 ps	20 kHz	AVI-V-HV2A-B
200 V	1 ns	50 kHz	AVIR-1-B
200 V	2 ns	20 kHz	AVIR-4D-B
400 V	2.5 ns	2 kHz	AVL-5-B-TR

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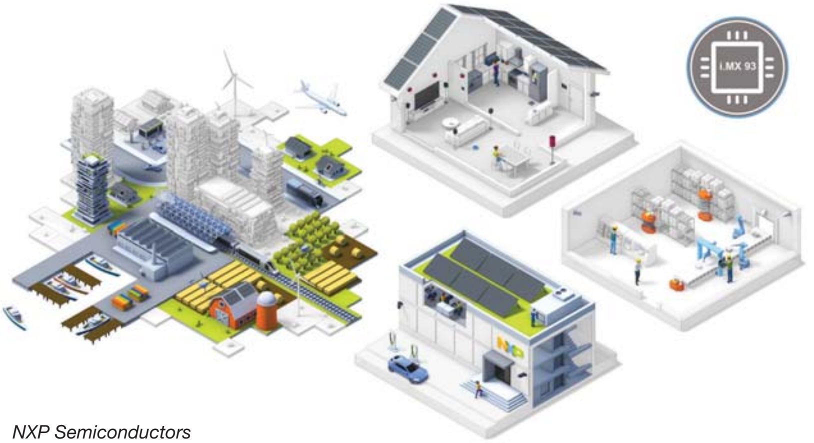
ElectronicDesign 70 YEARS
Embedded Revolution

WILLIAM G. WONG | Senior Content Director

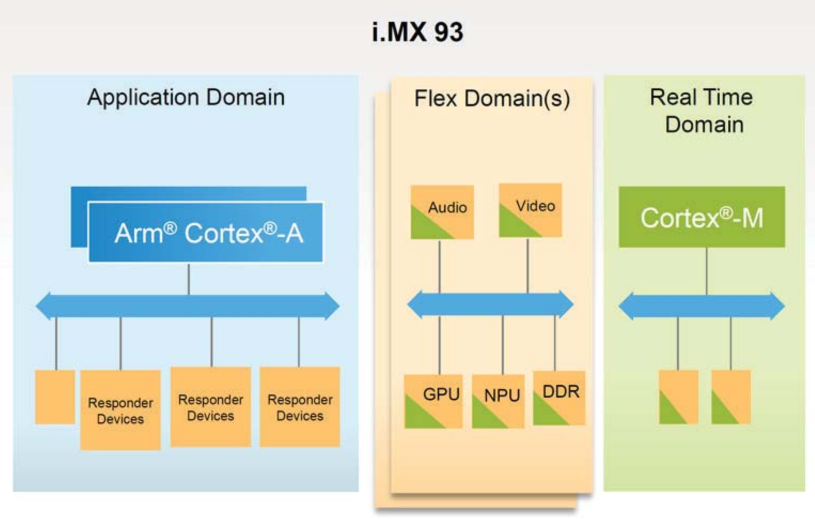
This is Where Embedded SoCs are Headed

NXP's i.MX 93 incorporates Arm's Ethos-U65 machine-learning accelerator.

In one sense, NXP Semiconductors' i.MX 93 system-on-chip (SoC) was not unexpected. It includes Arm's latest complement of application processors, a microcontroller, and the Ethos-U65 neural processing unit (NPU), along with the usual complement of peripherals from serial ports to GPUs *(Fig. 1)*. Combining Cortex-A and Cortex-M processors in an SoC is common these days; the Ethos architecture was announced by Arm years ago.



NXP Semiconductors



1. NXP divides its i.MX 93 into two processor blocks and a Flex Domain that includes the Ethos-U65 neural processing unit (NPU).

Still, being first out of the gate with cutting-edge hardware has its advantages. Developers have been chomping at the bit for good, low-power, low-cost, integrated machine-learning solutions to make the Internet of Things a bit smarter.

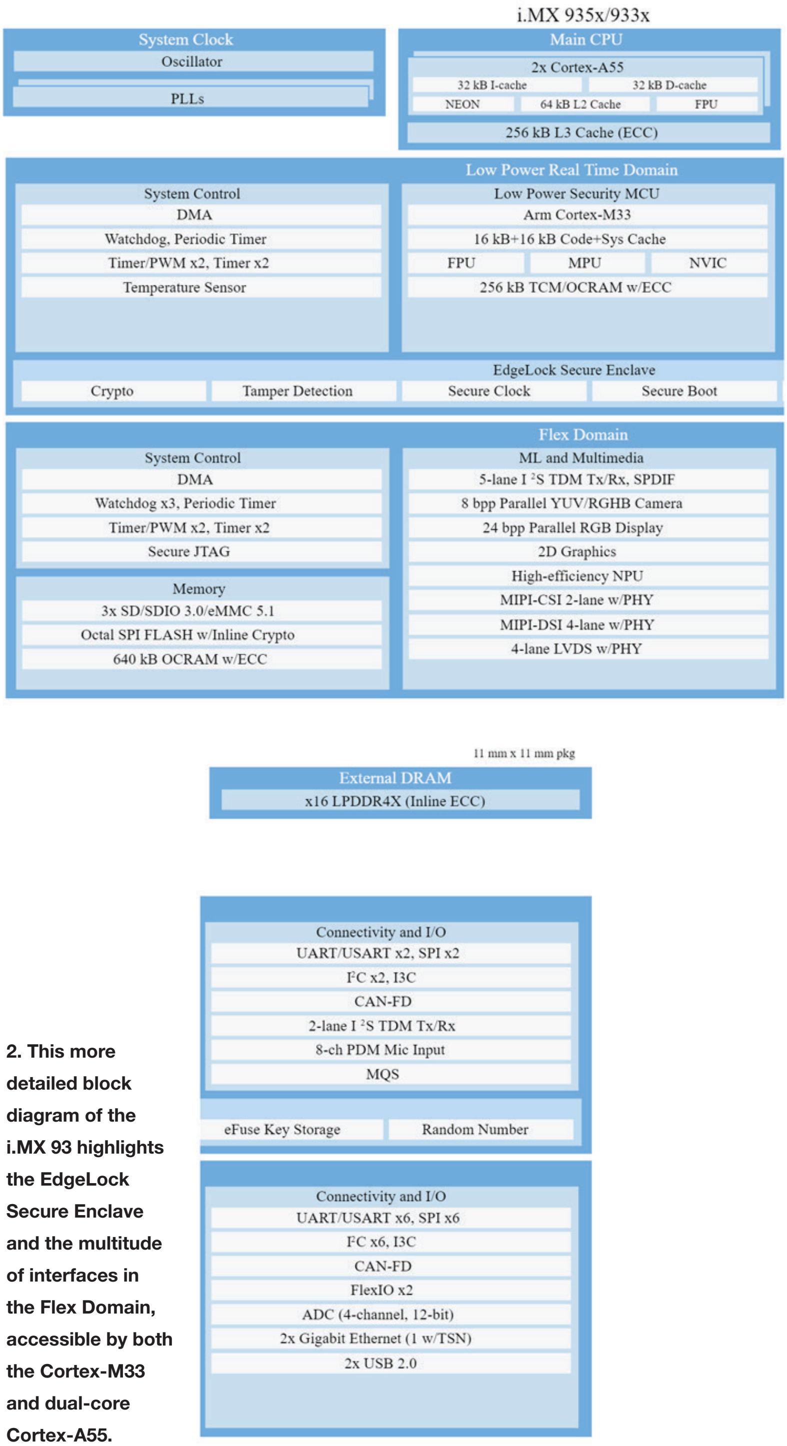
The NPU is grouped together within the Flex Domain that essentially includes most of the peripherals accessible by the microcontroller and application processor *(Fig. 2)*. The Cortex-M33 has additional peripherals, so its domain can operate independent of the application processor, providing a low-power operating environment.

The EdgeLock Secure Enclave maintains its own processor and crypto support and storage. It has secure-boot and TrustZone support, as well as features like attestation. In addition, the system supports Microsoft Azure Sphere, providing secure communication and updates. The i.MX 93-CS is specifically designed for this environment. The i.MX 93 will work with other cloud solutions, too.

"We're making it easier for developers to create, connect, and maintain innovative IoT devices by providing a comprehensive platform actively supported by the scale and expertise of Microsoft software, cloud, and security experts," said Halina McMaster, Partner Group Program Manager, Microsoft Azure Sphere.

"Together with NXP, we are delivering a variety of Microsoft Azure Sphere-certified edge processors that provide a secured environment for customer applications, critical over-the-air update infrastructure, and more than 10 years of ongoing security improvements for every Azure Sphere chip," continued McMaster. "The i.MX 93-CS chips will unlock opportunities across industries for performance optimization, sustainability, and safety through new classes of secured IoT devices."

In essence, the i.MX 93 is designed to provide a secure application environment with real-time and low-power support via the Cortex-M33, and the ability to efficiently handle machine-learning applications in real-time without needing to go to the cloud for assistance. This allows data and decisions to be handled locally, as well as minimizes the amount of data to be exchanged with the cloud since the data can be massaged locally instead of sending raw data.



2. This more detailed block diagram of the i.MX 93 highlights the EdgeLock Secure Enclave and the multitude of interfaces in the Flex Domain, accessible by both the Cortex-M33 and dual-core Cortex-A55.

The Ethos-U65 can manage multiple machine-learning models simultaneously. The number and speed at which these models are handled will be application-specific, but it can easily deal with many multimedia chores as well as analyze data like motor-control information to provide preventative maintenance information. It provides more ML processing power than the dual-core Cortex-A55 and consumes less power, allowing it to operate under the auspices of the Cortex-M33 in low-power mode while the application processor is asleep.

The Cortex-M33 has its own 256 kB of RAM with ECC support. This allows the chip to run without keeping any off-board LPDDR4 running.

The Ethos-U65 is supported by NXP's eIQ ML software development kit. This includes the eIQ Toolkit workflow tools, the GUI-based eIQ Portal development environment, and eIQ inference engine options. The software can target NXP's array of machine-learning platforms, including the Cortex-A55 and Cortex-M33. Of course, the Ethos-U65 is more efficient, but this allows developers to distribute ML chores as needed.

The Cortex-A55 processors can run operating systems like Linux while the Cortex-M33 tends to run bare-metal applications or RTOS. A number of RTOS platforms with cloud connectivity are available.

The other part of the puzzle is NXP's Product Longevity Program, which includes the i.MX 93. It promises at least 10 years of support for the products, and often exceeds 15 years. This is important for applications that aren't churning out new revisions every six months. ed

Industrial Revolution

JAMES MORRA | Senior Editor

Intel Launches $1 Billion Fund to Build Foundry Ecosystem, Backs RISC-V


Intel

Intel is boosting efforts to become a top contract chip maker with a new wave of ecosystem investments. The Santa Clara, California-based company launched a $1 billion fund to invest in companies and startups building technologies to speed up the chip development cycle for its foundry customers. Intel said the fund will invest in areas such as software tools, equipment, materials, architectures, IP, and advanced packaging.

Intel is also partnering with electronic design automation (EDA) firms such as Ansys, Cadence, Siemens, and Synopsys, and IP vendors such as Arm and SiFive to fine-tune their software and IP for Intel's process technology.

"Innovation thrives in open and collaborative environments," said Randhir Thakur, head of Intel Foundry Services (IFS), which is working with Intel Capital, the company's venture arm, to allocate the funding. He said the fund "will marshal the full resources of Intel to drive innovation in the foundry ecosystem."

Intel is trying to recover from years of disarray after it fell behind rivals in designing the most advanced chips and building them, shaking its dominance for the first time in years. CEO Pat Gelsinger is trying to revive Intel's fortunes and transform it into an even more sprawling company that builds chips for other firms—and even rivals—based on their blueprints and using its leading-edge process technologies.

As part of his IDM 2.0 strategy, Intel is investing tens of billions of dollars to boost its production capacity, including at the new $20 billion manufacturing site in Ohio that it announced last month.

Part of the strategy is to support a wide range of IP tuned for Intel's process technologies. Intel touted its ability to support IP based on the industry's leading instruction set architectures (ISAs). Intel is opening its trove of x86 CPUs and other IP cores to its foundry customers, and it will support competing instruction sets Arm and RISC-V, even in processors that contain IP blocks based on all three architectures.

Intel also announced plans to build an "open chiplet platform" and open die-to-die interconnect standard to help its customers in the shift from a system-on-chip (SoC) to a system-in-package (SiP) design approach.

Backing RISC-V

In addition, Intel said it will use the $1 billion fund to invest in companies and offerings that will strengthen the ecosystem around the open-source RISC-V architecture and encourage more of the industry to adopt it.

Intel will use the fund to help companies in the RISC-V market innovate faster, working with them to adapt IP for its process technologies and put them on the priority line in its chip fabs for prototyping runs. The company will also support them with design resources and build development boards and software tools. An ISA is the fundamental code used by software to communicate with the hardware underlying a CPU.

The firm is partnering with several key players in the RISC-V ecosystem, such as Andes Technology, Esperanto Technology, SiFive, and server CPU startup Ventana Micro Systems. The company will work with them to optimize and enhance their RISC-V CPU cores and chiplets for its process and packaging technologies.

Intel said partnering up will allow its foundry business to build chips with a wider range of RISC-V cores inside, from embedded to high performance, for data centers, autos, networking, 5G, and other markets.

A range of startups, corporations, and even governments are placing a bet on RISC-V as an alternative to Arm and the x86 architecture used by AMD and Intel. One of its advantages is that it's open source, giving any company the ability to adapt the CPU cores to their specific needs without the costs or restrictions of other instruction sets. Furthermore, it doesn't depend on companies such as Intel or Arm to drive research and development.

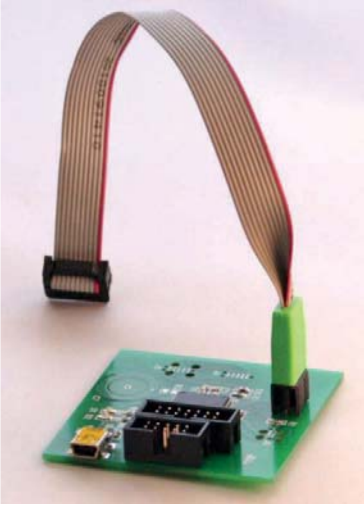
Open instruction sets are relatively new to the semiconductor landscape. Nonetheless, they are gaining ground fast, particularly in China, and companies are trying to convince foundries to support more RISC-V IP offerings.

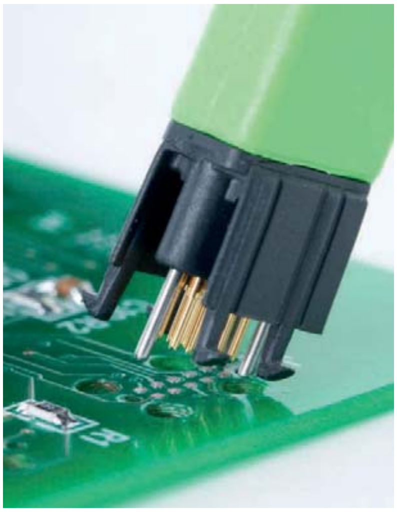
The RISC-V architecture is further behind rivals in terms of having a rich open-source software ecosystem, which is as important to its growth as hardware. To address that, Intel said it is funding an open software-development platform that will give engineers across the ecosystem more freedom to experiment with it.

"As the leading open-source ISA, RISC-V is a great fit for our open ecosystem vision, which is why we are making investments and building partnerships that will empower the ecosystem," Thakur said in a blog post.

Intel also is joining RISC-V International, which oversees the design of the instruction set alternative and extensions. ed

Tag-Connect





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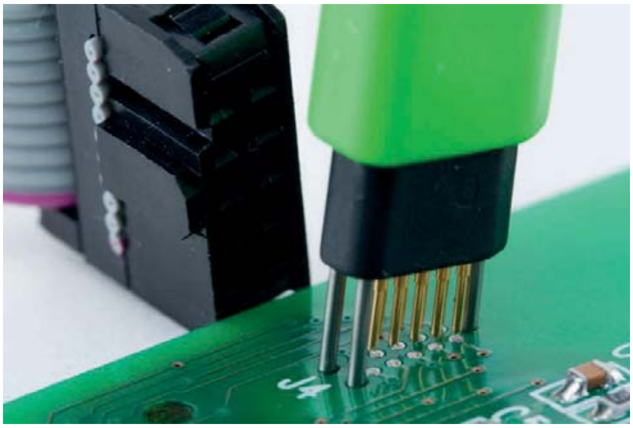

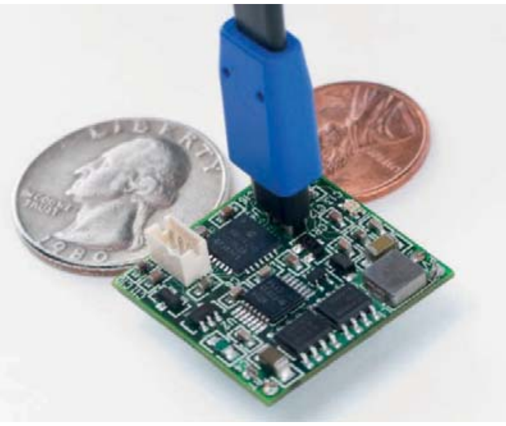

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Then and Now

WILLIAM G. WONG | Senior Content Director

A Quick Stroll Through 70 Years of Communications

1. PC motherboards often had multiple socket types to handle different interfaces. *Image: Dreamstime | xxl_678492*

2. Coax is still used for cable modems, but was used to support Ethernet at its inception. *Image: Dreamstime | xxl_1598388*

3. Fiber links provide high-speed connections with no crosstalk issues. *Image: Dreamstime | xxl_50204661*

Processors and memory have changed radically over the past 70 years, but the variability of those areas doesn't hold a candle to communications technology. I obviously can't do it justice in such a short article, but I did want to highlight some of the major changes in wired and wireless communication.

Wired

On-board serial and parallel buses have been around for ages, and they've progressed significantly in terms of throughput. One of the most basic items—serial asynchronous communication—is a generation old yet still one of the most used interfaces on microcontrollers and motherboards.

Standards like RS-232 and CAN allow for cabling to be longer and more robust, and variations like multidrop solutions continue to be used regularly. Other serial interfaces like I^{2}C and SPI have been pulling double duty as peripheral and memory interfaces. There are variations like Hyperbus, OneWire and I3C, too.

Parallel buses for motherboards *(Fig. 1)*, such as the venerable Industry Standard Architecture (ISA) bus that ran at 8.3 MHz, morphed into the Extended Industry Standard Architecture (EISA). These were eventually replaced with Peripheral Component Interconnect (PCI). Versa Module Europa (VME) found a home in rugged environments, but all were superseded by high-speed serial interfaces.

PCI Express (PCIe) is the primary bus interface. Currently in its fifth generation, it runs at 32 Gtransfers/s with support for up to 32 lanes. This version also supports standards like CXL and CCIX that provide cache coherence on top of the PCIe peripheral support.

Local area networks have moved from 2.5-Mbit/s Arcnet and 10-Mbit/s Ethernet running over coax cables *(Fig. 2)* to twisted-pair and fiber-optic Ethernet, which now dominates the network space with speeds up to 400 Gbits/s being used on a regular basis. Fiber optics are no longer a specialty item *(Fig. 3)*.

Modems used over voice lines have given way to cable modems using Data Over Cable Service Interface Specification (DOCSIS) as well as other standards including fiber connections.

Wireless

Wireless communication has changed the way we look at networking. Recently, the migration from any form of analog communication to digital is evident in the ubiquitous 5G cellular solutions being deployed. Voice and video still go over the airwaves; however, in a digital format that's more conducive to the underlying communication infrastructure. AM/FM radio still endures, but television is now all digital and even AM/FM radio has a digital counterpart.

Wi-Fi has turned networking into something that was impossible with wired connections. It provides mobility and eliminates wiring so that networking can be deployed in existing spaces without major site modifications. Though still slower than the fastest wired connection even with multiple-input, multiple output (MIMO) support, it's more than fast enough for most applications, including video streaming.

The rise of low-power, wide-area networks (LPWANs) and other low-power network technologies such as Bluetooth, ZWave, Zigbee, and LoRaWAN, and cellular support like Narrowband IoT (NB-IoT), have been relatively recent enhancements looking over the past 70 years. The limiting factors continue to be speed, distance, and power where you can only minimize any two. Likewise, bandwidth allocation and regulation affect availability and performance.

This short ride through old and new communication systems leaves a lot out. Much of it is still in use even as newer, faster, and more secure solutions continue to emerge. What's remarkable is the level of compatibility with the plethora of existing standards. It's what has made these communication solutions workable. ed

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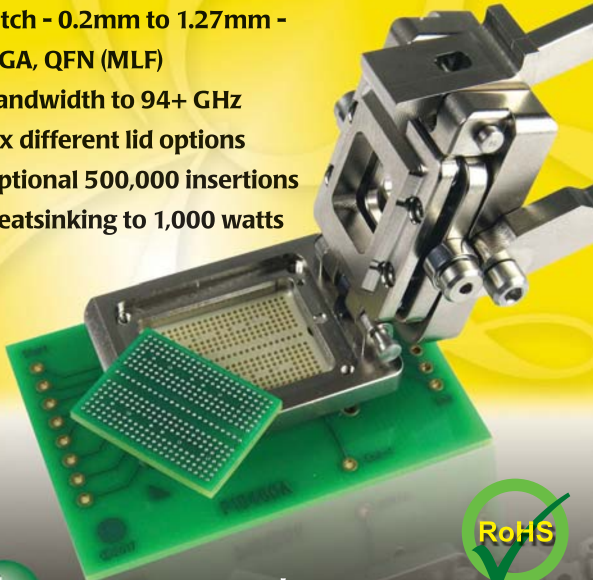

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Lab Bench

WILLIAM G. WONG | Senior Content Director

Reading Rust for C Programmers

Here's a very short intro to the syntax for Rust, the up-and-coming programming language in the embedded space.

Rust is the rising darling in the safe and secure programming arena. The challenge these days is that it's changing as we speak, which will create havoc on embedded applications—especially those that require long-term support. It will likely join Ada, C, and C++ in the future as it continues to be refined. That's why it's good idea to get to know Rust's features, such as its memory management and approach to object-oriented programming.

Those are both major topics that I will push off to later articles. Their details are a bit more complex than what I want to do here, which is talk about some basic syntax that makes reading Rust code easier for the Rust novice.

Below is a short, runnable Rust program to generate Fibonaci numbers. It highlights some interesting aspects of Rust that tend to be skipped when presenting Rust for the first time:

```
fn print_fib_1(n: usize) {
    println!("Fibonacci 1");
    let mut x = (1, 1);
    for i in 0..n {
        println!("{}: {}", i, x.0);
        x = (x.1, x.0 + x.1)
    }
}

fn print_fib_2( arr: &mut [i32]) {
    println!("Fibonacci 2");
    arr[0] = 1;
    arr[1] = 1;
    let n = arr.len();

    for i in 2..n {
        arr[i] = arr[i-1] + arr[i-2];
    }

    for i in 0..n {
        println!("{}: {}", i, arr[i]);
    }
}

fn main() {
    const NUMBER: usize = 5;
    println!("Hello, Fibonacci!");
    print_fib_1(NUMBER);

    let mut x:[i32; NUMBER] = [0; NUMBER];
    print_fib_2(&mut x);
}
```

The **fn** keyword introduces a function or procedure. There's additional syntax for function return values, but that's for another time. The argument, **n**, is of type **usize**.

Now for the interesting part. The **println!** for printing is actually a macro named **println**. The exclamation point indicates that a macro is being invoked. Also, macros can have a variable number of arguments, while a function has a fixed number. The brackets in the format string, {}, are placeholders.

Rust supports tuples, i.e. **(1, 1)**, that contain heterogenous elements, while arrays have homogenous elements. Both are fixed-length items; it's possible to get the length, i.e., **arr.len()**. The range, i.e., **0..n**, in the for loop are a syntax common to other languages. The array element access looks like **arr[i]**, while the tuple elements are **x.1**.

The **let** statement binds a value to a variable. The **mut** keyword indicates that the variable is mutable, which is the default for Ada, C, and C++. Note: Non-mutable and constant are different. A non-mutable is one that the program can't change at this point.

I should also talk about this function argument: **arr: &mut [i32]**. The ampersand indicates a reference that in this case is to an array of type **i32** that changed. On the other hand, **const** is used to define a constant that must be written as an uppercase name like **NUMBER**.

Finally, we have something that looks like this:

```
let mut x:[i32; NUMBER] = [0; NUMBER];
```

This defines an array **x** that has **NUMBER** of elements of type **i32**. The assigned value is an array of 0s. Of course, the code that's generated will allocate the array in the stack and fill it with zeros before proceeding.

There are a lot of new ideas in Rust, or ones that look different than in other languages.

There are a lot of new ideas in Rust, or ones that look different than in other languages. Knowing what you're looking at will help garner a better understanding of Rust when you start coding. I hope this helps. ed

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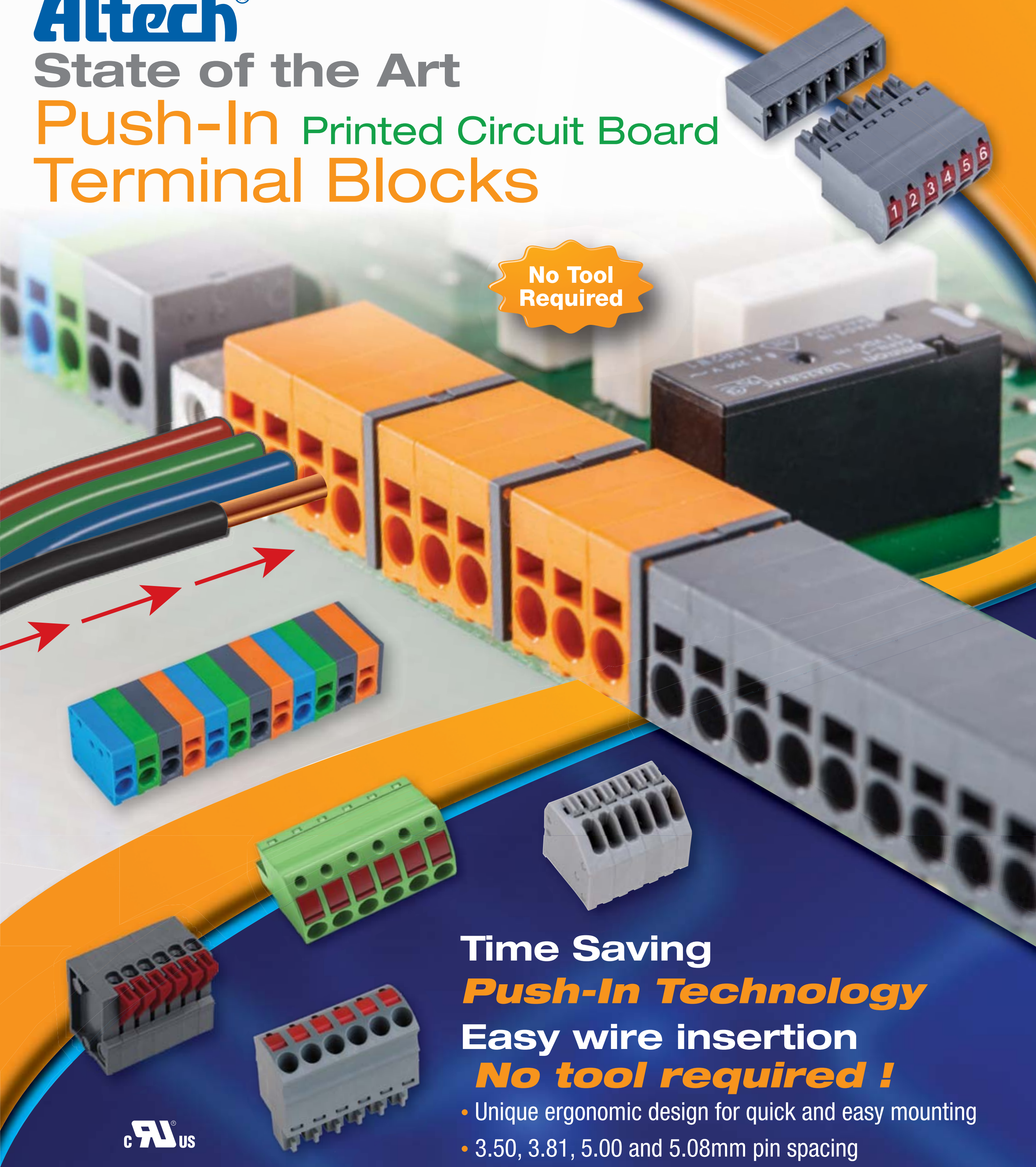

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