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CTSD Precision ADCs (Part 2): CTSD Architecture Explained

This article will delve into CTSD ADCs using a less traditional approach, enabling signal-chain designers to envision a new class of easy-to-use precision ADC technology that interconnects a few well-known components.

n Part 1, we highlighted the key challenges of incumbent signal-chain designs that can be simplified significantly with a precision continuous-time sigma-delta (CTSD) ADC, as it maintains continuous-time signal integrity while achieving the highest precision. Now, the question is what's behind the CTSD architecture that enables it to achieve these advantages?

The traditional approach of explaining the concept of CTSD technology is to first gain an understanding of the basics of a discrete-time sigma-delta (DTSD) modulator loop and then substituting the discrete-time loop elements with equivalent continuous-time elements. While this method provides in-depth insight of sigma-delta functionality, we aim to provide a more intuitive understanding behind the inherent advantages of precision CTSD ADCs.

To begin, we will outline a step-by-step approach to building a CTSD modulator loop starting with the widely known, closed-loop inverting amplifier configuration and combining it with an ADC and a DAC. Then we'll evaluate the basic sigma-delta functionality from the circuit we build.

Step 1: Revisiting the Closed-Loop Inverting-Amplifier Configuration

One of the key advantages of the CTSD ADC is that it offers an easy-to-drive continuous resistive input rather than a traditional switched capacitor sampler upfront. One of the circuits that has a similar input impedance concept is the inverting amplifier, which we will use as a starting block toward
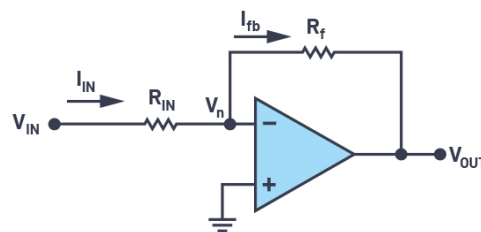
1. A closed-loop op amp in an inverting amplifier configuration.

building a CTSD modulator loop.

A closed-loop op-amp configuration has always been the go-to option for replicating an analog input with high fidelity. *Figure 1* shows one of the most popular op-amp configurations, which is called an inverting amplifier configuration.[1] One of the measures of the fidelity is the output to input gain, also known as—in sigma-delta nomenclature—the signal transfer function (STF). Determining the parameters that affect the STF requires analyzing the circuit.

To refresh our mathematical skills, let's revisit the derivation of the famous V_{OUT}/V_{IN}. In the first step, the open-loop gain of op amp A is assumed to be infinite. This assumption directly leads to making the op amp's input negative (V_n) at potential ground. The application of Kirchhoff's laws at this node gives:

$$I_{IN} = \frac{V_{IN}}{R_{IN}} , \ I_{fb} = -\frac{V_{OUT}}{R_f} \tag{1}$$

Mapping this to V_{OUT} and V_{IN}, we get the gain or STF as:

$$STF = \frac{V_{OUT}}{V_{IN}} = -\frac{R_f}{R_{IN}} \tag{2}$$

Next, let's go beyond the impractical assumption of infinite gain and rederive the STF with the finite gain of A for the op amp. The STF now looks like:

Clock Edge Samples

	V_{IN}	$V_{OUT} = V_{OUTDAC}$	$V_n = (V_{OUT} + V_{IN})/2$	$V_{OUT\_INT} = -A \times (V_n)$	D_{OUTADC}
First sample edge	1	0	0.5	−50	−50
Second sample edge	1	−50	~ −25	~2500	2500
Third sample edge	1	2500	~1250	~−12,500	−12,500
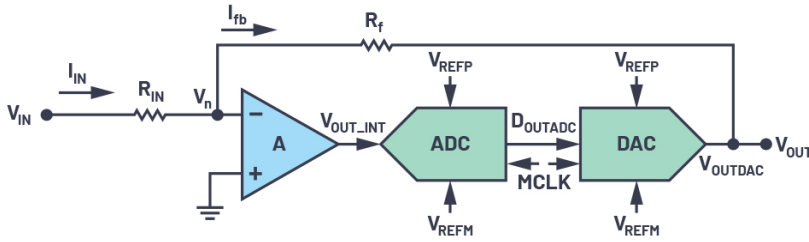
2. Introducing an ADC and DAC in an inverting amplifier configuration.

$$STF = -\frac{R_f}{R_{IN}} \times \left(\frac{A}{\left(1 + \frac{R_f}{R_{IN}} \right) + A} \right) \qquad (3)$$

From here, textbooks generally describe the sensitivity toward the R_{IN}, R_f, and A parameters. For our case, lets proceed toward building the CTSD loop.

Step 2: Introducing Discretization into the Amplifier

The requirement for our ADC signal chain is a digitized version of V_{IN}. In our next step, we introduce the digitization in this circuit. Rather than use the traditional way of putting a sampling ADC directly at the input signal, we'll try a different approach and put a representative ADC that follows the amplifier output to obtain the digitized data. But the output of the ADC can't be used as feedback directly—it's required to be an analog voltage. So, then, we need to follow up the ADC with a voltage digital-to-analog converter (DAC) *(Fig. 2)*.

Because of the ADC and DAC, V_{OUT} is still a representation of V_{IN}, but with quantization error due to the added digitization. Therefore, nothing has changed in the signal flow from V_{IN} to V_{OUT}. One point of note here: Keep the functionality of the loop symmetric to about 0 V; easing our mathematical derivation, the references of ADC and DAC are chosen to be:

$V_{REFP} = V_{REF}/2$, and $V_{REFM} = -V_{REF}/2$

Step 3: Introducing the Analog Accumulator—the Integrator

Is the closed-loop configuration in *Figure 2* stable? Both the ADC and DAC are discretization elements working on a sampling clock (MCLK). It's been an unachievable dream of converter specialists to design a delay-free ADC or DAC. Since these loop elements are clocked, the input is generally sampled

on one edge and processed on the other clock edge. Thus, the output of the ADC and DAC combination V_{OUT}, which is the feedback in *Figure 2*, is available only after one clockcycle delay.

Does this delay in feedback have any implication on stability? Let's trace how V_{IN} transfers along. For simplification, let's assume $V_{IN} = 1$, $R_{IN} = 1$, $R_f = 1$, and the gain of op amp A is 100. At the first clock cycle, the input voltage is 1 and the DAC output feedback, V_{OUT} or V_{OUTDAC}, is 0 and not available until the next clock edge *(see table)*.

As we trace the error between the input and feedback to the output of the amplifier and ADC, we can see the output keeps growing exponentially. This is technically termed as the runaway problem.

This happened because the ADC input works on instantaneous error gained up by the amplifier, i.e., the ADC decides even before the feedback is available, which wasn't required. If the ADC works on an accumulated, averaged error data so that the error due to one clock delay of feedback is averaged out, then the output of system would be bounded.

The integrator is one such analog equivalent of an averaging accumulator. The gain of the loop is still high but only

(a)

(b)
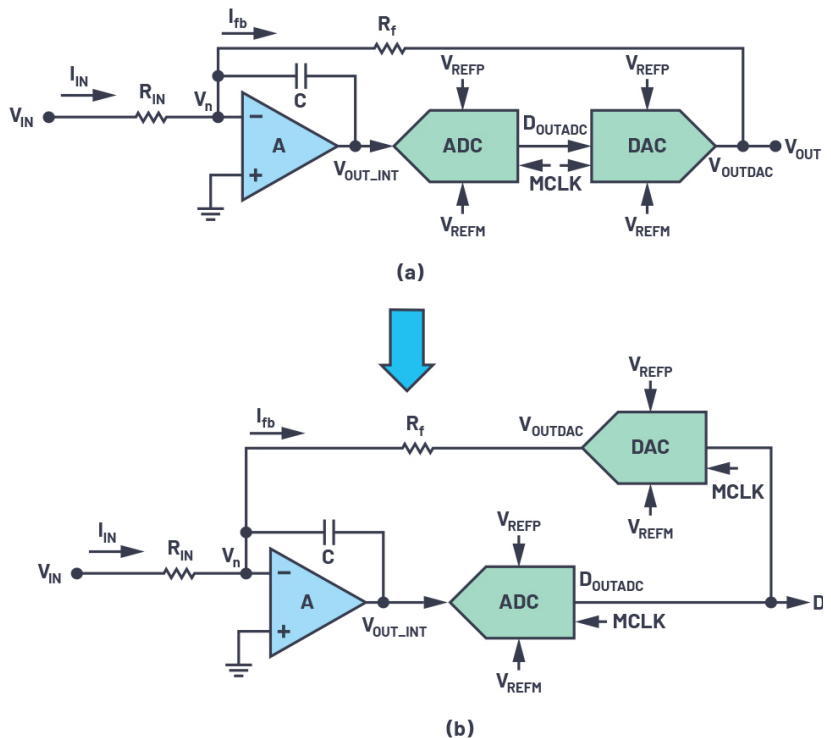
3. Introducing the integrator into the loop (a). Rearranging the loop to highlight D_{OUTADC} as the output (b).

at low frequencies, or, in other words, in the frequency bandwidth of interest. This ensures that the ADC isn't presented with any instantaneous errors that can lead to a runaway situation. So, the loop is now amplifier modified as an integrator followed by the ADC and DAC *(Fig. 3a)*.

## Step 4: Simplifying the Feedback Resistor

Our element of interest is D_{OUTADC}, so let's rearrange the loop elements to highlight D_{OUTADC} as the output of the system *(Fig. 3b)*. Next, let's visit the simplification of the DAC and R_f path, and for that let's dig into the DAC's details.

The purpose of the DAC is to convert a digital code (D_{IN}) to an equivalent analog current or voltage in proportion to the reference. To further extend the advantages of continuity to reference, what we've considered here is a general DAC architecture based on a resistor ladder that has no switching load on reference.

Let's review a thermometric resistor DAC,[2] which converts D_{IN} to the DAC current, with relation to Equation 5:

$$I_{DAC} = \frac{V_{REF}}{R_f} \times \frac{D_{IN}}{2^N} \tag{5}$$

where $V_{REF} = V_{REFP} - V_{REFM}$, the total reference voltage
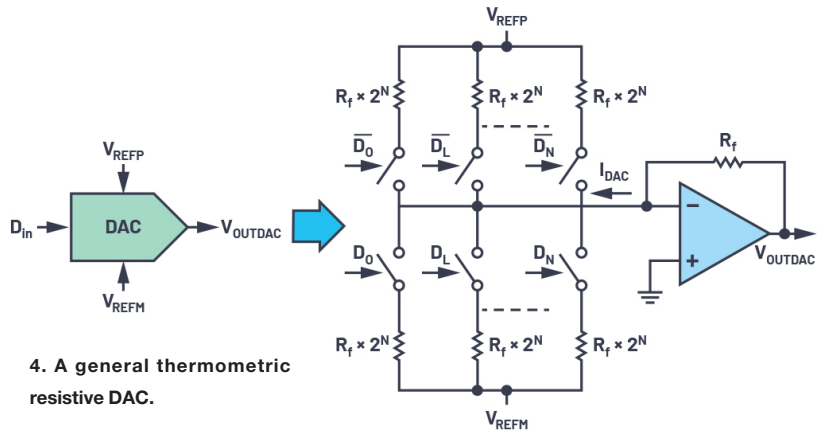
4. A general thermometric resistive DAC.

across the DAC.

- D_{IN} = Digital input in the thermometric code
- R_f = Feedback resistor; split as each unit element
- N = Number of bits

To get the voltage output, an I to V conversion follows by using an op amp in a transimpedance configuration,[3] as shown in *Figure 4*. So:

$$V_{OUTDAC} = I_{DAC} \times R_f \tag{6}$$

Going back to our discretized loop of *Figure 3b*, this V_{OUTDAC} is again converted back to current, I_{fb}, through the feedback resistor of the inverting amplifier, implying the signal flow is $I_{DAC} \rightarrow V_{OUTDAC} \rightarrow I_{fb}$. Mathematically:

$$I_{fb} = \frac{V_{OUTDAC}}{R_f} = I_{DAC} \tag{7}$$
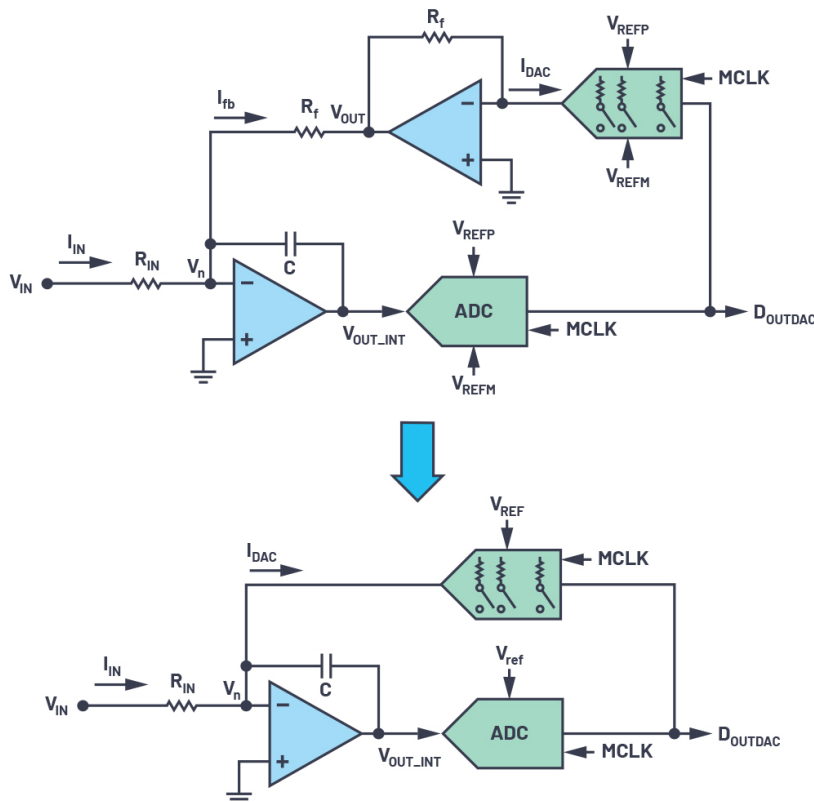
From the above signal flow and formula, we see that converting V_{OUTDAC} to I_{fb} is a redundant step that can be bypassed. Removing the redundant elements and, for simplicity, representing ($V_{REFP} - V_{REFM}$) as V_{REF}, let's redraw our loop *(Fig. 5)*.

And voilà! We've built a first-order sigma-delta loop! And all by stitching together well-known elements—an inverting amplifier, an ADC, and a DAC.

## Step 5: Understanding Oversampling

Up to now, we've grasped the construction of a CTSD loop, but not yet appreciated the particularities offered by this fanciful loop. The first step toward that is understanding oversampling. ADC data is useful only if there are enough sampled and digitized data points to extract or interpret the analog signal information.

The Nyquist theorem advises that, for

5. Removing redundant I to V and the feedback resistor.
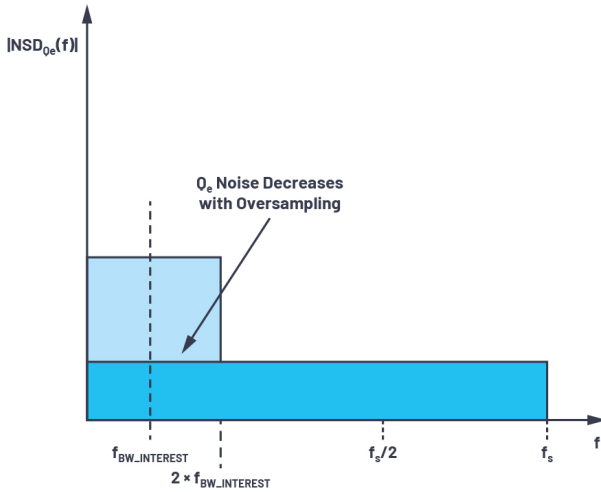
6. A noise spectral density comparison between Nyquist sampling and oversampling.
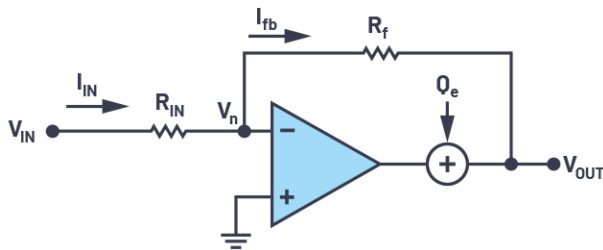
7. The introduction of an error in an inverting amplifier configuration.

8. The introduction of quantization error Q_e in a sigma-delta loop.

9. Integrator transfer function.

faithful reconstruction of an input signal, the sampling frequency of the ADC should be at least twice the frequency of the signal. If we keep adding more data points over this minimum requirement, it would further reduce the error in interpretation.

Following that line of thought, in sigma-delta, the sampling frequency is selected to be much higher than the suggested Nyquist frequency. This is known as oversampling. Oversampling[4] helps reduce the quantization noise in the frequency band of interest by spreading the total noise over much higher frequency *(Fig. 6)*.

Step 6: Understanding Noise Shaping

Signal-chain designers shouldn't feel lost when sigma-delta experts use terms like noise transfer function (NTF) or noise shaping.[4] Our next step will help them get an intuitive understanding of these terms, as they're unique to sigma-delta converter nomenclature. Let's revisit our simple inverting amplifier configuration and introduce the error Q_e at the output of the amplifier *(Fig. 7)*.

The contribution of this error at the output is quantified as:

$$V_{OUT} = \frac{Q_e}{\left(1 + \cfrac{A}{\left(1 + \cfrac{R_f}{R_{IN}}\right)}\right)} \tag{8}$$

The mathematical formula translates that the error Q_e is attenuated by the open-loop gain of the amplifier, which is just reiterating the advantage of a closed loop.

This understanding of the closed-loop advantage can be extended to quantization error Q_e of the ADC in the CTSD loop. This is the error introduced due to digitization of the continuous signal at the output of the integrator *(Fig. 8)*.

We can now intuitively conclude that this Q_e would be attenuated by the integrator. The integrator TF is $|H_{INTEG}(f)|$ $= 1/|s \times RC| = 1/2\pi fRC$, and its corresponding frequency domain representation is shown in *Figure 9*. Its profile is equivalent to a low-pass filter profile with high gain at low frequencies, and the gain reduces linearly as frequency increases. Correspondingly, the attenuation for Q_e would then look like a high-pass filter.
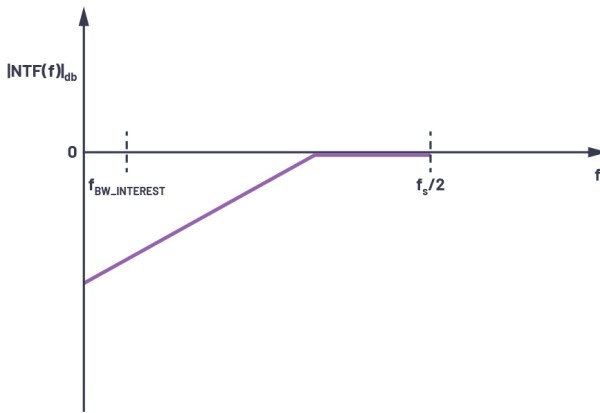
The mathematical representation of this attenuation factor is the noise transfer function. For an interim, let's ignore
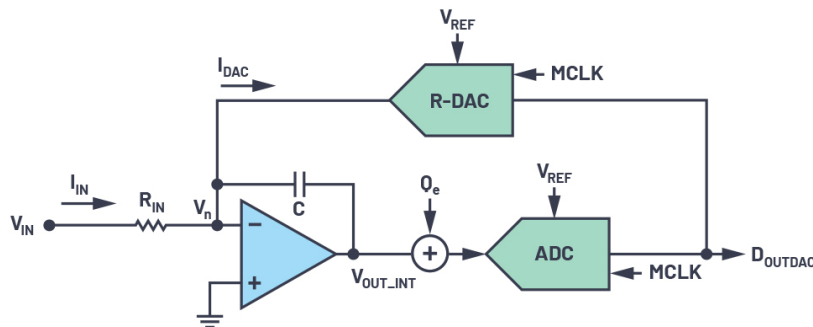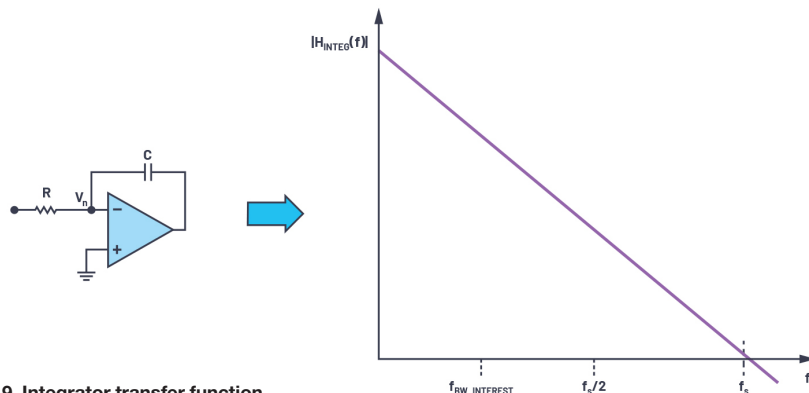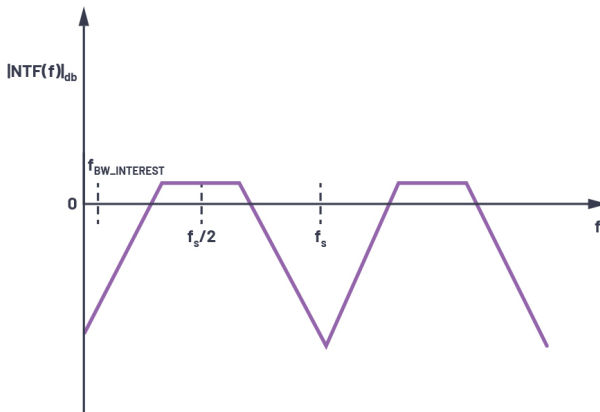
10. Noise transfer function without the sampler. It has a high-pass filter profile.

11. The noise transfer function of a CTSD ADC.

12. A block diagram of a CTSD ADC modulator loop from an analog input to a digital output (a). A frequency spectrum representation of an input signal at the output of a modulator and the output of a digital filter (b).
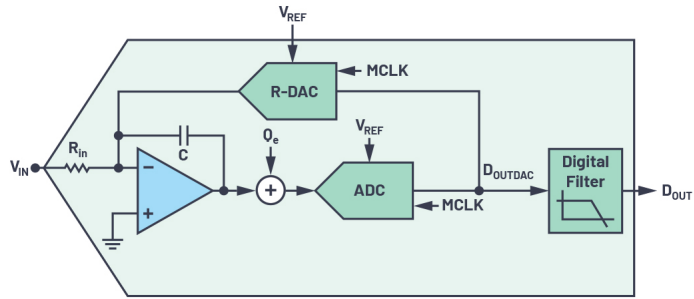
the sampler in the ADC and the switches in the DAC. The NTF, V_{OUTADC}/Q_e, can be evaluated by following the same exercise as we did for the inverting amplifier configuration, which in the frequency domain looks like a high-pass filter profile *(Fig. 10)*:

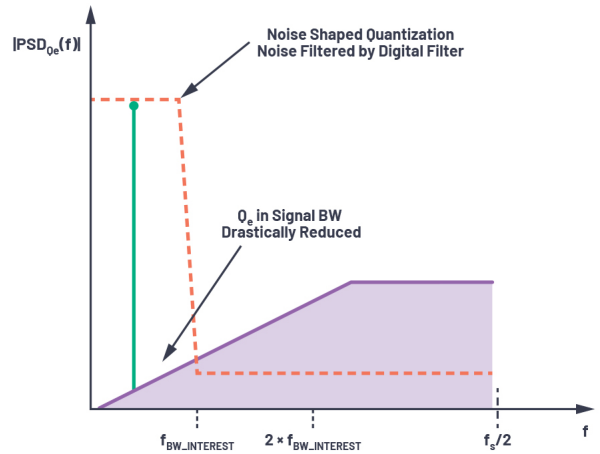$$NTF\_int = \frac{V_{OUTADC}}{Q_e} = \frac{sR_fC}{(1 + sR_fC)} \qquad (9)$$

In the frequency band of interest, the quantization noise is completely attenuated and pushed to "not to our concern" high frequencies. This is what's called noise shaping.

With the sampler in loop, the quantization-noise-shaping analogy remains the same. The difference being the NTF frequency response would have replicated images at every multiple of f_S *(Fig. 10)*, thus creating notches at every integer multiple of the sampling frequency.

The uniqueness of sigma-delta architecture lies in the fact that putting an integrator and a DAC loop around a crude ADC—for example, a 4-bit ADC—and applying the concept

of oversampling and noise shaping reduces the quantization noise significantly in the frequency bandwidth of interest. It also masks this crude ADC to a 16- to 24-bit precision ADC.

These basics of the first-order CTSD ADC can now be extended to any order of modulator loop. The sampling frequency, the crude ADC specifications, and the order of loop are top-level design decisions driven by the performance requirements of the ADC.

Step 7: Completing the CTSD Modulator with a Digital Filter

Generally, in an ADC signal chain, the digitized data is post-processed by an external digital controller for any signal information extraction. In sigma-delta architecture, as we know now, the signal is oversampled. If this oversampled digital data is directly given to the external controller, then a lot of redundant data needs to be processed. This causes excess power and real-estate cost overheads in the digital controller

design.

Therefore, before data is presented to the digital controller, the data samples are dropped in an efficient way without affecting the performance. This process, called decimation, is done by digital decimation filters. *Figure 11* shows a typical CTSD modulator with on-chip digital decimation filters.

Figure 12b shows frequency response for an in-band analog input signal. At the output of the modulator, we observe the noise shaping of the quantization noise, drastically reducing it in the frequency band of interest. The digital filter helps attenuate the shaped noise beyond this frequency bandwidth of interest so that the final digital output (D_{OUT}) is at the Nyquist sampling rate.

Step 8: Understanding the Clock Sensitivity of CTSD ADCs

So far, we have understood how CTSD ADCs keep the continuous integrity of the input signal, which significantly simplifies signal-chain design. This architecture also has a few limitations, mainly dealing with the sampling clock MCLK.

The CTSD modulator loop works on the concept of integrating the error current between I_{IN} and I_{DAC}. Any error in this integrated value would cause the ADC in loop to sample the error and reflect this in the output. For our first-order integrator loop, the integrated value over the sampling time period of T_s for constant I_{IN} and I_{DAC} is given by:

$$\delta Vout_{integ} = \frac{T_S}{RC} \times (I_{IN} - I_{DAC}) \qquad (10)$$

For an input of 0, the parameters that would affect this integration error are:

• **MCLK frequency:** As indicated by Equation 10, if the MCLK frequency scales, then the RC coefficient that controls the slope of integration also needs to be retuned to get back the same integrated value. This implies that a CTSD modulator is tuned for a fixed MCLK clock frequency and can't support varying MCLK.

• **MCLK jitter:** The DAC code and, hence, I_{DAC} change every clock time period T_s. If the I_{DAC} time period randomly changes, then the average integrated value keeps changing, as shown in *Figure 13*. So, any error in the sampling clock time period in the form of jitter would affect the modulator loop's performance.

CTSD ADCs are sensitive to the frequency and jitter of an
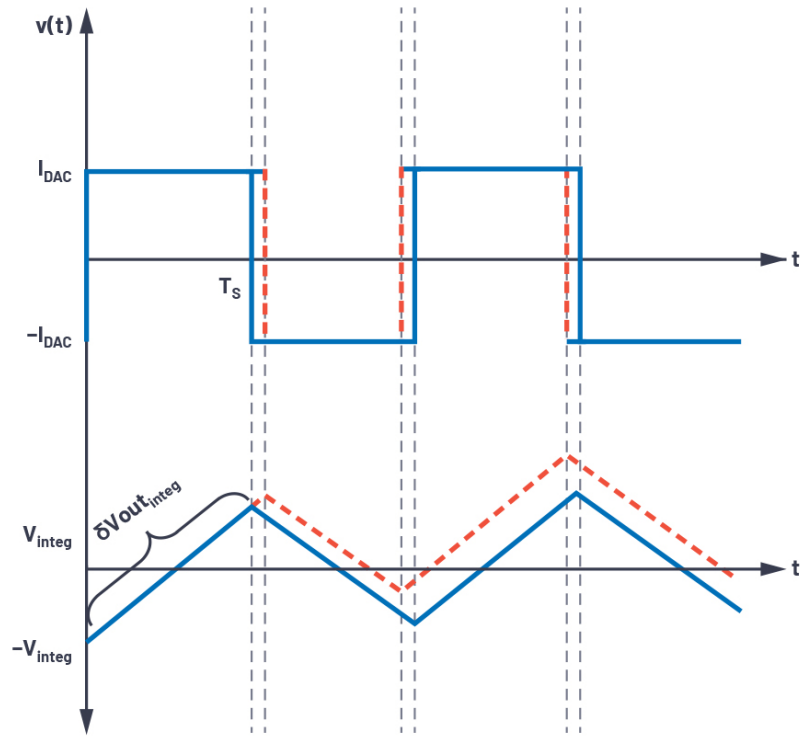
13. The clock sensitivity of a CTSD modulator.

MCLK because of the above reasons.[5] But Analog Devices has identified solutions to work around these fallacies. For example, the challenges of generating and routing accurate, low-jitter MCLK along the system to the ADC can be addressed using a local, low-cost crystal and oscillator near the ADC.

The fallacy around the fixed sampling frequency has been addressed by using asynchronous sample-rate conversion (ASRC) that enables a variable and independent digital output data rate for the digital controller irrespective of the fixed sampling MCLK. More information about this will be detailed later in this series.

Step 9: All Set to Explain the CTSD Concept to Your Buddies!

Part 1 of the series highlighted certain signal-chain advantages of a CTSD ADC, while this article focused on the insights of the modulator loop built from Step 1 to Step 6 using the concept of a closed-loop op-amp configuration. *Figure 12a* also helped us visualize these advantages.

The input impedance of a CTSD ADC is equivalent to the input impedance of the inverting amplifier, which is resistive and easy to drive. Using innovative techniques, the reference used by the modulator loop's DAC also has been made resis-

tive. The sampler of the ADC is after the integrator and not directly at the input, which enables inherent alias rejection for interferers outside the frequency band of interest.

We will deep dive into each of these advantages and their corresponding impact in a signal chain in the following articles in this series. Keep an eye out for Part 3—it focuses on inherent alias rejection and its quantification using a set of measurements and performance parameters introduced for the first time with the AD4134, which is based on the CTSD architecture.

Acknowledgements

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