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ABOUT ALTECH

Altech Corporation is an established United States supplier of components and devices used in industrial control, instrumentation, medical and automation applications. Altech provides a very broad line of products that meet UL and international standards and are RoHS and REACH compliant. Altech's commitment to continuous quality management has been recognized since 1999 when they were awarded ISO 9001 certification.

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Altech's products meet UL and international standards, and all are RoHS- and REACH-compliant. Altech's commitment to quality and continuous quality management had been recognized since May 27, 1999 when it was awarded the prestigious honor of ISO 9001 certification. Since then, Altech has successfully gone through the recertification process and complies with ISO 9001:2015.

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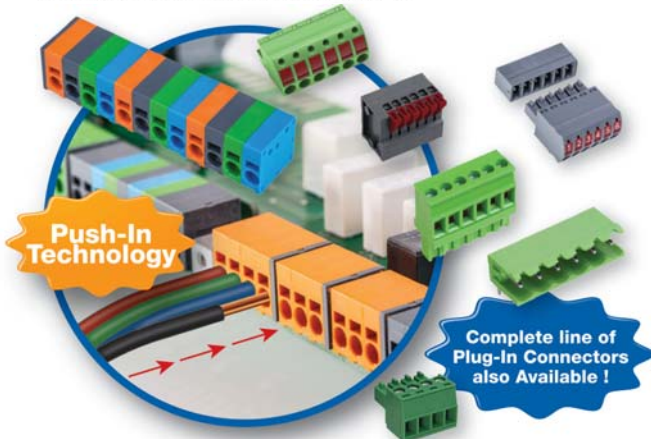


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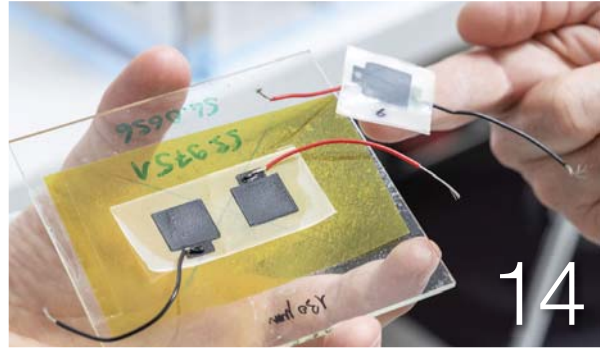
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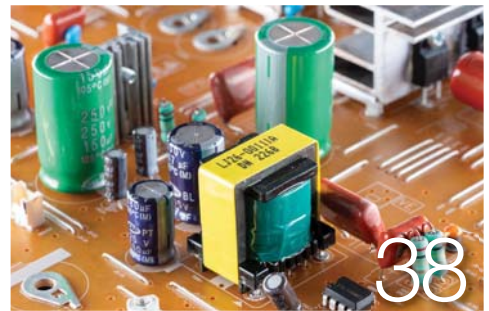
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Editorial

WILLIAM WONG
Senior Content Director

The Complexities of Electronic Design and Scheduling

Electronic design has always been technically challenging, which is why many of us got into the business. Unfortunately, it can be a bit more strenuous than just that these days. COVID-19 continues to upend everything from peoples' health to the supply chain. Designers now need to consider the availability of foundries and the chips they use. The lack of a second source often leads to alternate designs to compensate.

Still, some things never change around here, like the interest and questions about power and analog circuits. Luckily we have some articles like "Consider Realistic Voltage Sources When Designing Power Supplies" (see p. 38) and "EMI Shielding for Drones and UAVs" (p. 27) to explore those topics.

Another technology area that's cultivated more interest in design is the Internet of Things (IoT). IoT means connectivity and its corresponding increase in security attack surfaces, thus putting security at the level of power and analog when it comes to reader attraction. Of course, we have articles like "Identifying Vulnerabilities in Cellular Networks" (p. 19) and "The 4 Building Blocks for LoRa Networks" (p. 6) to address this area.

How engineers work together due to the internet and COVID are highlighted by our annual salary survey. The article "How Working Remotely is Spawning a Design Revolution" (p. 50) by Alix Paultre, Editor-at-Large, touches on how COVID-19 has affected our workflow. We will be taking a closer look at some of the more engineering- and software-specific collaboration-related tools in the future.

Also, looking forward to 2022, we will have more TechXchange Webinars, TechXchange Talks, and Kit Close-up videos for viewing on our website. We will be celebrating our 70th anniversary in 2022, including our new Do You Recognize These? series. It should be fun. ■

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The 4 Building Blocks for LoRa Networks

This article introduces the four main elements of LoRa network architecture and discusses some of the most common challenges faced by designers while developing LoRa end-nodes. How can regulatory certified LoRa modules help overcome such challenges?

Long-range (LoRa) technology is extending the reach of the Internet of Things (IoT) by combining long-range wireless connectivity with low-power performance. From smart cities to smart agriculture to supply-chain tracking, LoRa is an ideal choice to create flexible IoT networks that can operate in both urban and rural environments. But how easy is it really to develop a new LoRa solution or migrate to one?

Understanding a new wireless technology and choosing the right solution for your application can be exhausting. Wireless radio-frequency (RF) design usually requires in-depth RF expertise and adds significant development time for designers.

LoRaWAN Network Architecture

LoRa is a wireless modulation technique or physical layer that allows low-

power end-devices to communicate over long range. LoRaWAN—a wireless networking protocol that acts as a media-access-control (MAC) layer—is implemented on top of the LoRa physical layer. The LoRaWAN specification details the communication protocol and network architecture and is meant to provide secure communication of end-devices and interoperability within the network.

The LoRa network has four elements (Fig. 1):

- *End-nodes* are elements of the LoRa ecosystem that gather sensor data and transmit/receive the data. They're generally remotely connected and are battery-powered.
- The *gateway* is a transparent bridge between the end-nodes and network server. Typically, end-nodes use LoRaWAN to connect to the gateway, while the gateway uses high-bandwidth networks such as Wi-Fi, Ethernet, or cellular to connect to the networks.
- A *network server* connects to multiple gateways. It gathers data from the gateways and filters out duplicate messages, decides which gateway should respond to end-node messages, and adapts data rates to extend battery life of end-nodes.
- The *application server* collects data from end-nodes and controls the actions of the end-node devices.

Let's take a closer look at LoRa end-nodes and the challenges in designing them.

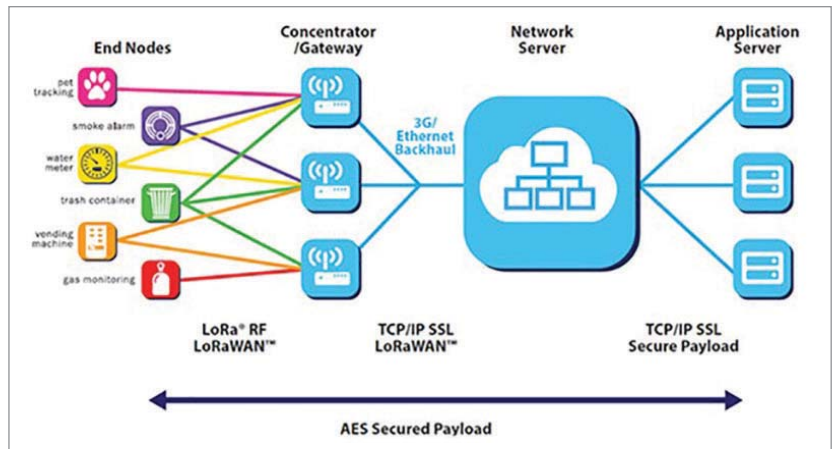
Common Challenges in Designing LoRa End-Nodes

End-nodes are simple objects, such as sensors and actuators. Typically, they comprise the "things" within the Internet of Things (IoT). In the LoRaWAN ecosystem, an end-node communicates to the network server through one or many gateways.

LoRa end-nodes are typically low-cost battery-powered applications that need to be power-efficient. Depending on the development time, target costs, power consumption, and RF expertise available, several options are available to build LoRa end-nodes. Before researching those options, let's look at some of the most common challenges that designers face when designing end-nodes. They include:

RF Design

As with any wireless design, signifi-



1. These are the four main elements of the LoRa network. (Source: LoRa Alliance)

cant RF design expertise is needed when designing LoRa end-nodes. When using LoRa systems-on-chip/systems-in-package (SoCs/SiPs), the end-node device developer is responsible for the entire RF design, including schematics, bill of materials (BOM), PCB layout, antenna tuning, and other RF hardware.

Even with the best documentation and application design guides, RF design isn't always easy. It not only requires in-depth RF expertise, but also adds up significant development time for designers. Furthermore, debugging RF designs most often requires special equipment, adding further to the development costs.

To overcome the RF design challenges, some suppliers offer SoCs/SiPs that are supported by excellent documentation, regulatory certified reference designs, and detailed chip-down design packages. However, for the shortest development time and reduced risk, an RF optimized, tested, and certified LoRa module is almost always the best choice. These modules can provide a complete solution as a single component reducing design risk and development times.

Regulatory Compliance and Certifications

LoRa/sub-GHz radios typically operate in the ISM license-free band. The frequencies vary depending on the region, making it challenging for hardware and

software designers. Diligent care must be taken to design a fully compliant solution while keeping the BOM costs minimal. Also, RF regulatory requirements are constantly changing. Thus, keeping up with the regulatory changes, re-testing the devices, and re-certifying for compliance can cost several thousands of dollars—as well as engineering time—for end-node developer companies, money and time that could otherwise be spent on new projects.

Using a certified LoRa module solves this issue easily; the module manufacturer takes care of keeping up with the regulatory requirements and re-certifying modules to the latest specifications. All of these costs and time spent on regulatory compliance can be completely avoided by choosing a regulatory certified LoRa module.

Multi-Region Operation

LoRa devices support several frequencies, depending on the region. Often, end-node manufacturers release their end-products in one major region first. Once the demand ramps up, companies investigate expanding the same design in other regions. Having a single SKU that supports multiple regions allows for seamless migration and expansion of the end-product into different countries and regions. A regulatory certified LoRa module that works for multiple

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(Continued from page 7)

frequency bands is ideal for this type of product expansion.

Robust Software

Generally, LoRa modules integrate the whole LoRaWAN stack inside the module. The end-node developer only needs to implement the initialization and communication to the module. With LoRa SoCs/SiPs and with standalone LoRa modules, the stack must either be provided by the manufacturer, or the developer must develop its own stack if no stack is provided.

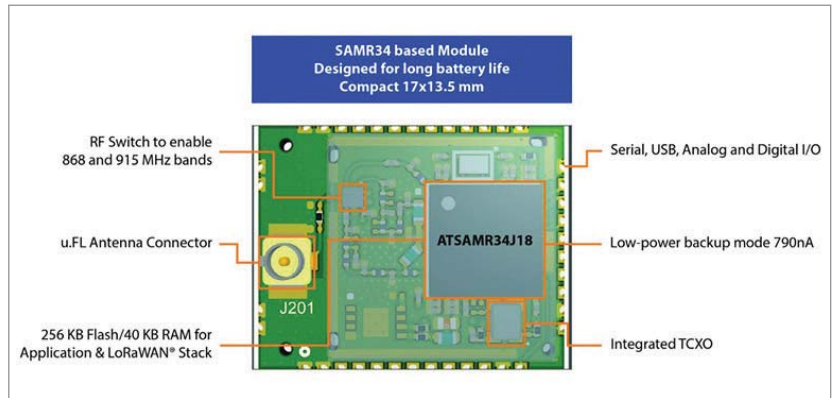
To minimize software development, it's recommended to choose LoRa modules/ICs that are supported by the manufacturer's LoRaWAN stack. Proven LoRaWAN stacks from manufacturers ensure interoperability of end-nodes with major LoRaWAN networks and gateways, enabling end-nodes to work across different networks with reduced risk.

Migration Path from Modules to SoCs

Many companies start their prototypes and initial production runs with certified modules to reduce risk and get their products faster into market. Once their product starts to ramp up, companies may decide to move to LoRa SoCs/ICs for increased flexibility or lower BOM costs. The migration isn't always easy, so it's very important to consider standalone modules that allow for simple software migration between the modules and ICs. Also, it's essential to choose suppliers that sell both modules and SoCs; therefore, the development platform, software migration, and support structure remain the same.

Regulatory Certified LoRa Modules Simplify LoRa End-Node Designs

LoRa modules consist of all required radio components along with LoRaWAN stack and RF circuitry, thus helping accelerate development of LoRaWAN end-devices. Since the RF development and the certification are implemented by the module manufacturer, any changes in certification specifications or component replacements are completely handled by



2. Shown is the block diagram for the WLR089U0 LoRa module.



3. The WLR089U0 LoRa module is based on Microchip Technology's SAM R34/35 family of ICs.

the manufacturer, saving tons of development time as well as re-certification costs for end-device manufacturers.

Standalone LoRa modules with highly integrated LoRa ICs provide enough memory to run the application code along with the LoRaWAN stack. This eliminates the need for an external microcontroller, saving board space and system costs. Figures 2 and 3 show a simple example of such a standalone module.

The WLR089U0 module based on the SAM R34/35 family of ICs from Microchip Technology is a compact module with 256 kB of flash and 40 kB of RAM, making it well-suited for space-constrained applications. The module includes an integrated RF switch, enabling multi-band operation and allowing the same module to be used across multiple geographies, facilitating market expansion for end-products. The WLR089U0 also is supported by Microchip's LoRaWAN stack and proprietary peer-to-peer software, easing the software development for end-users developing

Standalone LoRa modules with highly integrated LoRa ICs provide enough memory to run the application code along with the LoRaWAN stack.

LoRa applications.

Because the modules are based on the SAM R34/35 ICs, the migration path from modules to ICs and vice versa also is much simpler. Choosing such a module helps overcome all of the common design challenges while developing LoRa end-nodes, easing the entire design process.

Conclusion

Developing LoRa end-nodes can be complex and time-consuming. Highly integrated, certified LoRa modules provide an easy and proven approach to overcome the complex challenges involved in designing these end-nodes. Reliable software, larger memory, integrated RF switches, and regulatory certifications are some of the key features to look for in LoRa modules. Choosing a highly certified LoRa module not only helps simplify the design process, but also enables end-node developers to successfully differentiate their products and release them to market faster. ■

ADAPTABLE LOW PROFILE, COMPACT DIN POWER SUPPLIES



Managing the power requirements on a DIN rail system is becoming more challenging with new standards and increased compactness of control systems, particularly when mounted on smaller robotic systems and cobots.

A DIN rail system is one of the most efficient methods used to easily mount a variety of industrial control components inside an equipment rack. More often industrial controls are placed as close to the machine they are controlling as possible, further reducing the need for extra stretches of cables and wires. Although this is great for saving money on installation, it can cause real estate problems as everything become increasingly compact. Designed to be versatile and rugged—even for harsh environments—DIN rail systems are used in a wide variety of industries including utilities, building automation, machine tools, and medical equipment.

Besides standard circuit breakers, relays, and terminal blocks, DIN rail systems often incorporate important high-end components such as programmable logic controllers, motor and motion system controllers, and any number of additional special purpose devices meant to connect and interface with the growing IIoT networks in factories, buildings, and utilities around the world. For machine control, DIN rails often require power supplies that are able to integrate with an array of other devices and equipment.

Power Supplies

Standard DIN rail power supplies are typically over 5-inches high, 2- to 4-inches wide, and around 5-inches, or more, deep. These components can take up a lot of space on the rail. As DIN rail systems become tightly packed with devices offering special control features for greater industrial control capabilities, a large number of companies have been forced to solicit custom solutions for their power requirements.

A new series of ultra slim metal case DIN rail power supplies have been designed and manufactured by Altech that takes up less than half the space that a current power supply would normally occupy on a DIN rail. In comparison to standard 120 Watt DIN rail supplies that take up about 2 ½-inches of DIN

rail space, Altech's PSC-120 series would need only 1¼-inches of space on the DIN rail. These ultra-compact power supplies make it easy to include additional functionality in the same space as well as for use in shallow cabinets—without increasing costs. These ultra-compact high efficiency units also support 1+1 or N+1 redundancy and built in current sharing functions. These supplies also allow space for additional features to be added to a system on the same DIN rail.

Universal Input and Output

The Altech DIN rail power supplies are offered with a universal input feature that sets them apart from other products on the market. Regardless of power supply output, each product in the PSD and PSC series has an input requirement of 85-264 VAC/127-360 VDC. Output specifications vary for each unit in the series; for example, the PSC series power supplies provide outputs from 12 VDC to 48 VDC and up to 480 Watts. The PSD series power supplies cover wattages from 15 Watts up to 100 Watts and standard voltages include 5, 12, 15, 24 and 48VDC.

These new PSD and PSC DIN rail power supplies are particularly geared toward applications where the use of narrow cabinets is a necessary requirement due to real estate restrictions. This is particularly the case with the increased number of robots and cobots that are being produced today. The more portable an industrial machine becomes, the more important it is to have the controls—and power supply—available in a compact unit.

Up-to-Date Certification

Certification is a key requirement in industrial systems design and manufacturing for worldwide distribution. This includes new safety standards based on IEC 62368-1, which are superseding existing standards. While trying to keep things simple for product vendors, regulators in the U.S. and EU had agreed on the date the new standards would supplant the outgoing

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60950-1 and 60065 standards. Vendors were provided this unified target to focus their regulation compliance efforts in two of the most important worldwide markets. On December 20, 2020, the old standards were withdrawn, and any product covered by the scope of EN 62368-1 (the IEC standard as written into law by EU legislators) had to be tested in accordance with the new standard.

Following the EU's announcement, the UL organization in the U.S. confirmed it would move its own Effective Date for UL 62368-1 (the US version of IEC 62368-1) to supersede UL 60950-1 and UL 60065 as well. Therefore, everything changed at the end of 2020. And as the rule-makers have harmonized across the waters, OEMs must now have their new testing procedures and documentation in place.

Changing to an HBSE-Based Standard

IEC's technical committee had adjusted their standards-making philosophy to aim toward a less prescriptive and more future-proof document that helped create safer products for end users. With equipment increasingly operating in and around humans, we have officially entered the era of Hazard-Based Safety Engineering (HBSE) (see Figure 1). HBSE shifts the emphasis away from demonstrating that prescribed specifications have been met and requires product manufacturers to demonstrate that known hazards have been considered and the product has been designed to be safe to use in the expected context—such as cobots operating alongside a human in a production setting.



Figure 1: The HBSE three-block model shown is used to analyze energy classes, transfer mechanisms, and safeguards.

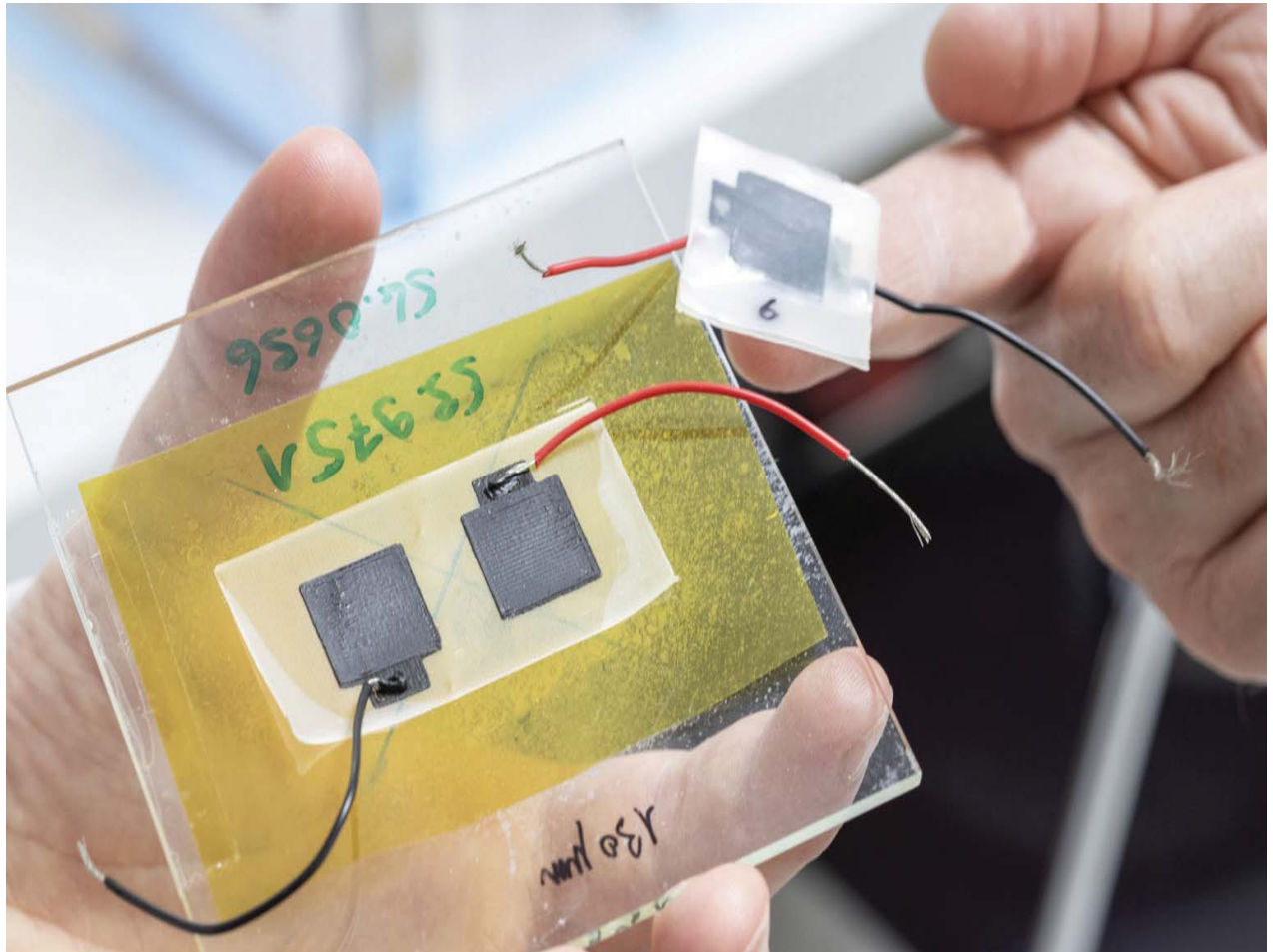
HBSE principles work to protect equipment users by identifying any potentially hazardous energy sources and the mechanisms by which the energy could transfer to a user, while proposing suitable means of preventing those transfers from happening. The scope includes normal operation and fault conditions. Safeguards are put in place to protect against pain or injury caused directly by electrical energy (electric shock) or thermal burn injury, and/or to prevent electrically caused fires that could result in pain, injury, death, or property damage. Importantly, HBSE also measures the effectiveness of the safeguards.

It is important for product designers to recognize that the new standards apply not only to the end product, but also to major components and subsystems used inside the product, such as the power supplies. For this reason, Altech has made sure that all their power supplies for their PSD and PSC series meet the latest standards. New 62368-1 hazard-based safety standards have been fully adopted in the U.S., Canada, EU, and other countries/regions. The older standards have been withdrawn. OEMs must test their new (and existing) products in accordance with the new standard.

Conclusion

DIN rail systems are used to save time and costs, allowing components to simply snap or slide into place rather than panel mounting each component separately. This is particularly advantageous for equipment that is operated near and around humans, such as the growing cobot industry. Power supplies for these systems are a key component and must meet the latest certifications as well as operate efficiently. Altech, once again, has stayed abreast of all the latest requirements for the wide variety of industries they serve and are able to supply components that offer high performance at reasonable costs.

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Despite their specific differences, the Internet of Things (IoT), device tagging, and other monitoring/tracking applications all have one thing in common: They all need a power source, even if only a small amount and for a limited, definable timespan.

The options for providing such power include electrochemical batteries, supercapacitors, or energy harvesting (separately or in some combination). However, they all share one trait: When they're no longer needed or viable—and many of these installations are shorter-term—they leave behind a power source that must be

disposed of properly, or more likely, will become litter and waste.

Now, a research team at EMPA (Swiss Federal Laboratories for Materials Science and Technology) has built print-on-demand supercapacitors using a modified, commercially available 3D printer along with their “not-so-secret sauce”—a recipe

for the gelatinous inks that the printer can dispense onto a substrate as surface.

The mixture consists of cellulose nanofibers and cellulose nanocrystals, plus carbon in the form of carbon black, graphite, and activated carbon. The researchers used glycerin, water, and two different types of alcohol plus a pinch of table salt (not for taste, of course, but for ionic conductivity) to properly liquify the solution and achieve the desired viscosity.

Despite the fragile sound of the design, this non-toxic capacitor isn't a delicate, limited-use component. It can withstand thousands of charge/discharge cycles and years of storage, even in freezing temperatures, and is resistant to pressure and shock. At the same time, when it's no longer needed, it can be placed in a compost pile or simply left "in nature." After just a few months, it will have decomposed into harmless particles.

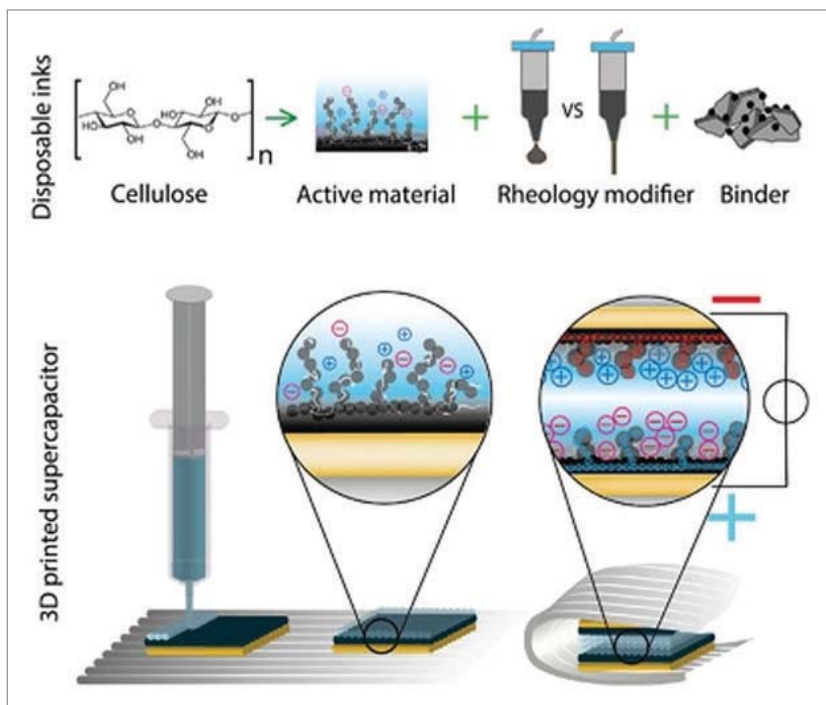
Developing the formulation and printing process was not a haphazard situation. "It sounds quite simple, but it wasn't at all," said Xavier Aebly of EMPA's Cellulose & Wood Materials lab. "It took an extended series of tests until all the parameters were right, until all the components flowed reliably from the printer and the capacitor worked." He added, "As researchers, we don't want to just fiddle about, we also want to understand what's happening inside our materials."

Multilayered—But Not a PCB

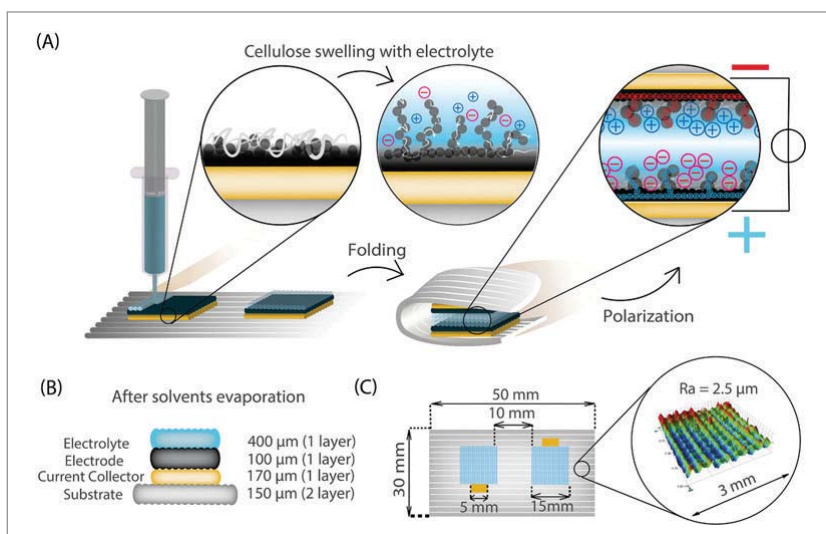
The supercapacitor needs four layers, which are produced by the 3D printer in sequence: a flexible substrate, a conductive layer, the electrode, and finally the electrolyte (Fig. 1). The researchers used a substrate made from ink composed of cellulose nanofibrils (CNFs), cellulose nanocrystals (CNCs), and glycerol as the base layer. The ink for the current collector contained graphite, carbon black, and shellac. The electrode ink incorporated CNFs, CNCs, glycerol, activated carbon, and graphite particles. The ink for the electrolyte contained CNCs, glycerol, and NaCl.

(Continued on page 18)

“It sounds quite simple, but it wasn’t at all. It took an extended series of tests until all the parameters were right, until all the components flowed reliably from the printer and the capacitor worked.”



1. The process of printing the supercapacitors is conceptually simple, and the materials and chemical solutions used are a precise combination of common substances.



2. The solvents in the "inks" evaporate after the 3D printing, which results in the ultra-thin supercapacitor layers.

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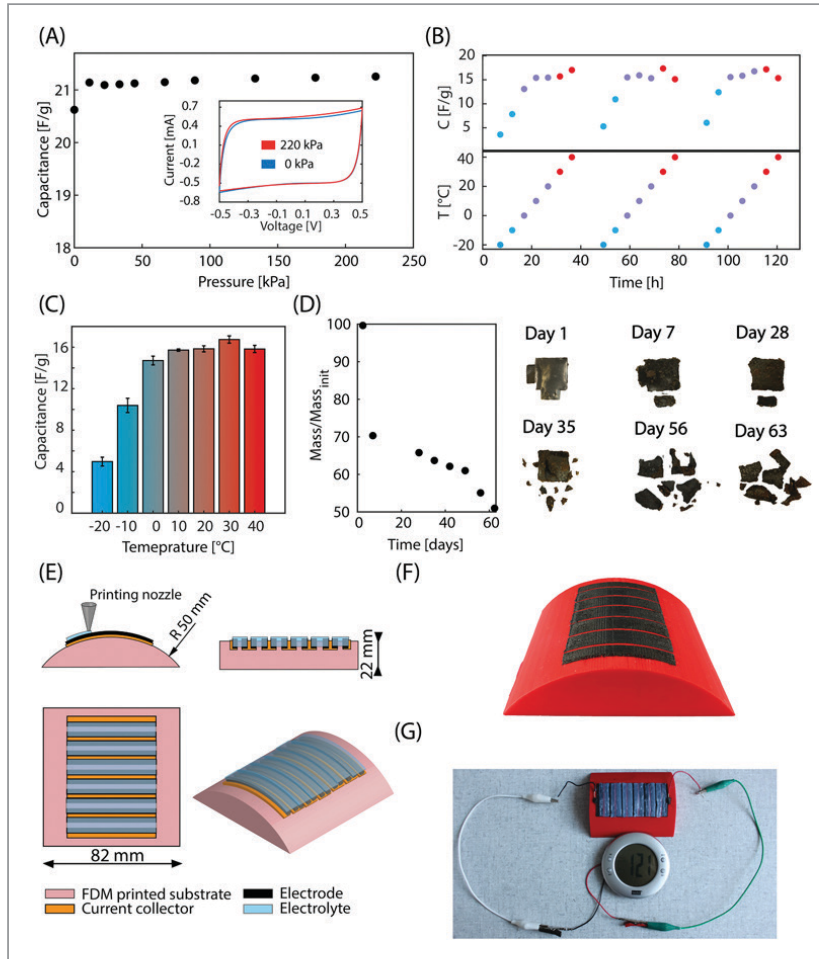
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1 2 3+4-



Dedication Makes The Difference

(Continued from page 15)



3. Shown is the performance of the supercapacitor (a through c); characterization of the rate of disintegration and bio-friendly degradation (d); and use of the supercapacitors in an assembly that powers a small clock (e through g).



4. The capacitor disintegrated after two months buried in soil, leaving only a few visible carbon particles.

These materials were printed on top of each other onto the substrate. They used direct-ink-writing (DIW), a printing technique in which a gel ink is extruded line-by-line and layer-by-layer to form 3D objects. The whole multilayer assembly is then folded up like a sandwich, with the electrolyte in the center (Fig. 2).

These materials were printed on top of each other onto the substrate. They used direct-ink-writing (DIW), a printing technique in which a gel ink is extruded line-by-line and layer-by-layer to form 3D objects.

The resulting devices supported a high capacitance of 25.6 farads/gram of active material with an operating voltage up to 1.2 V. One was used to demonstrate a small clock (Fig. 3).

The team also tested performance over time and temperature. To clearly demonstrate the biodegradability of the construction, they also performed decomposition tests and found that after just two months, the capacitor disintegrated, leaving only a few visible carbon particles (Fig. 4).

The work is detailed in their paper “Fully 3D Printed and Disposable Paper Supercapacitors” published in *Advanced Materials*; it’s behind a pay-wall and there’s no open-access copy posted (but you can read the original for a modest up-front fee, visit <https://onlinelibrary.wiley.com/doi/10.1002/adma.202101328>). There’s also open-access Supporting Information that has more details on the chemical composition of the inks, the setup parameters of the 3D printer, and additional test results (visit <https://onlinelibrary.wiley.com/action/downloadSupplement?doi=10.1002%2Fadma.202101328&file=adma202101328-sup-0001-SuppMat.pdf>). ■



Pravin Chakravarty, Dreamstime.com

Identifying Vulnerabilities in **CELLULAR NETWORKS**

This article takes an in-depth look at a systematic framework for the analysis of cellular-network protocols, involving a 4G LTE example, to enhance security.

Cellular networks are a critical infrastructure supporting applications in all domains we may think of, ranging from e-commerce, transportation/mobility, and education to eHealth/personal well-being and manufacturing. Cellular networks will be a key infrastructure for Internet of Things devices, and, indeed, the vision is that next-generation cellular networks will be more about devices than people. In other words, the goal of next-gen cellular networks is to be “sensing networks.”

However, even without looking into what next-gen cellular networks will be, it’s clear that technologies for cellular

networks have made major advances in the past few years. Fourth-Generation Long-Term Evolution (4G LTE) technology has increased the bandwidth available for smartphones, in essence delivering broadband capacity.

The most recent 5G technology further enhances transmission capacity and reduces latency, energy consumption, and error rates through the use of several technologies, including millimeter waves; small cells; massive multiple-input, multiple-output antennas; beamforming; full duplex transmission; and software-defined networks (SDNs). It enhances the flexibility of cellular networks by separ-

ating network control and forwarding planes and making the control plane directly programmable.¹

Because cellular networks are pervasive and used in sensitive applications, their security is a critical requirement. For example, a denial-of-service attack against a cellular network may paralyze communities and service infrastructures, with disastrous consequences.

Securing cellular networks is a challenging task because of their complexity. Cellular networks consist of multiple layers—e.g., physical layer, radio-resource-control (RRC) layer, non-access stratum (NAS) layer, etc. Each layer, in turn, has

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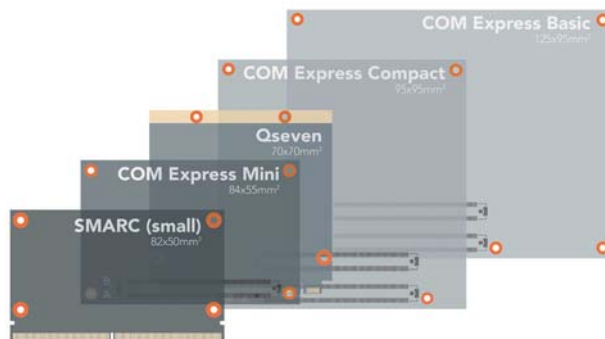


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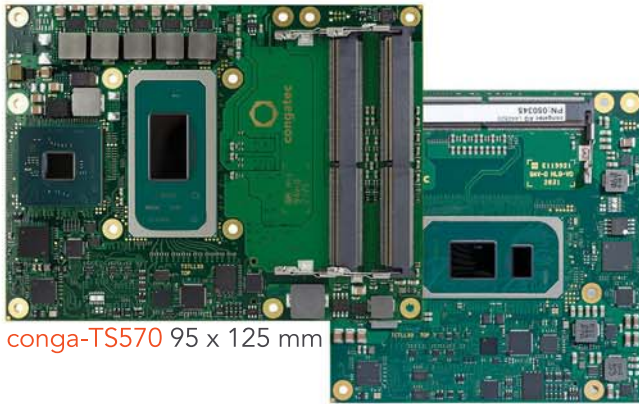
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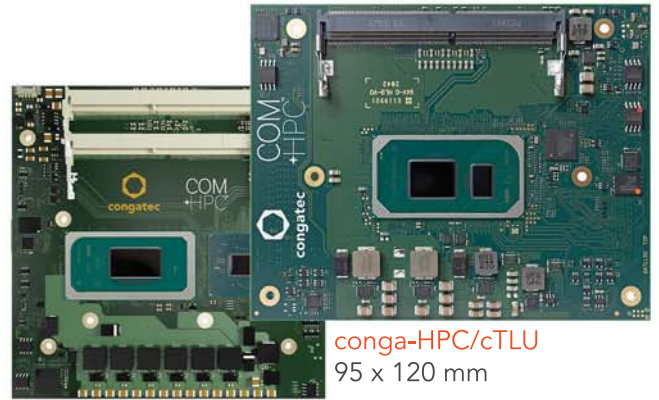
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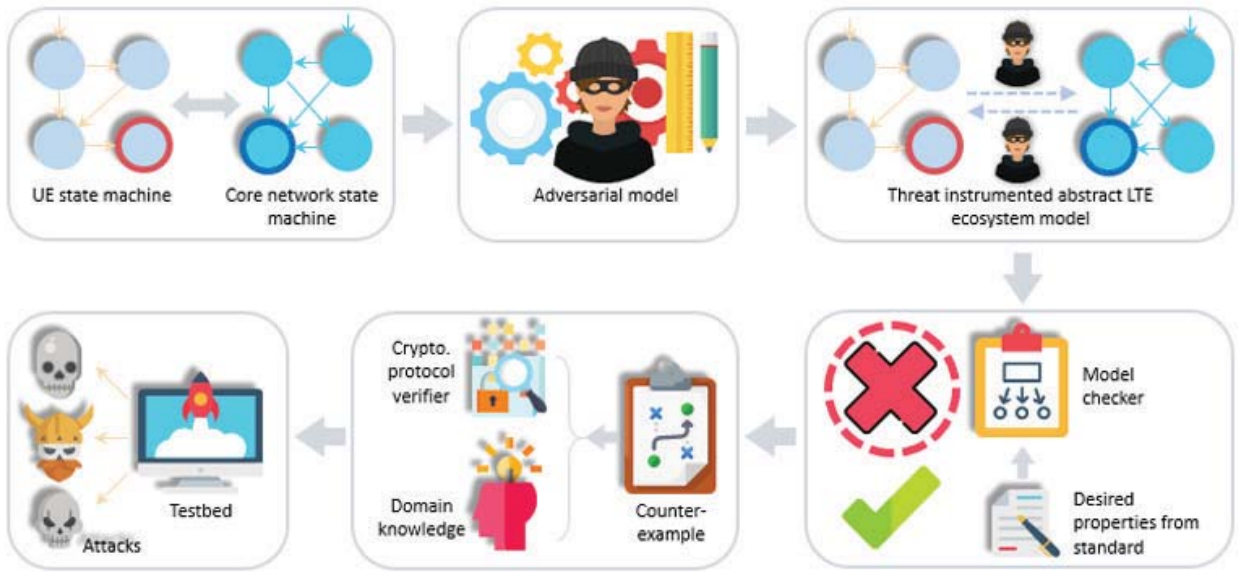
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1. As depicted in this architecture, the input to the LTEInspector methodology is a representation of each protocol in terms of two finite state machines, the user equipment, and the core network. (Image from Reference 3)

its own protocols to implement its procedures, such as the protocols for attaching/detaching devices to/from the network and for paging devices notifying of incoming voice calls and Short Message Service (SMS) text messages. Additional requirements, such as backward compatibility and interoperation across different wireless communication technologies, add to the complexity.¹

Comprehensive approaches to protecting cellular networks require deploying a wide variety of security techniques, ranging from basic techniques such as encryption and digital signatures, to software patching, anomaly detection, network segmentation, device hardening, etc. (see Reference 2 for an example of security measures for network infrastructure devices). However, a critical prerequisite to securing cellular networks is that the protocols designed, implemented, and deployed in them must be free of vulnerabilities. Due to the complexity of those protocols, systematic methodologies for their analysis are required.

Methodologies for Verifying Cellular Network Protocols

Perhaps the first systematic methodology for analyzing cellular network

protocols is the LTEInspector approach,² developed for the analysis of the NAS layer of the 4G LTE protocol stack. This layer manages the establishment of communication sessions and maintains continuous communications with the user equipment (UE), i.e., the cellular phone, as it moves.

The NAS layer provides a set of protocols governing the interactions between the UE and the core nodes, such as the mobile switching center, serving GPRS support node, or mobility management entity (MME). We refer to the set of core nodes as the “core network” (CN). Each such protocol consists of multiple steps. For example, the protocol for UE attach includes the following high-level steps:

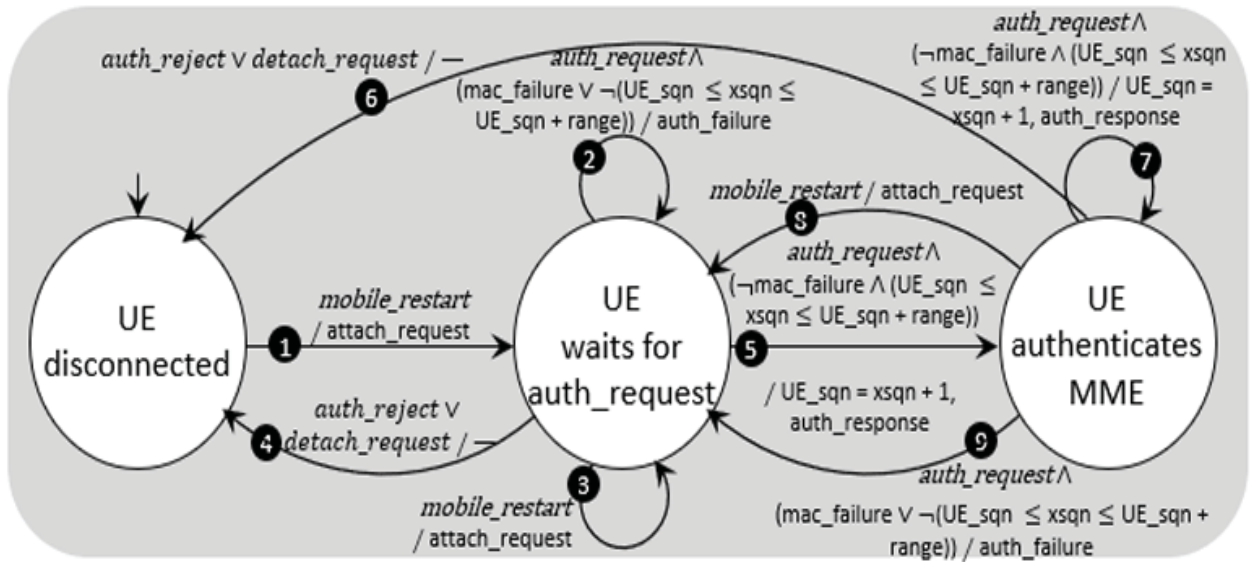
1. The UE sends an attach request to the CN, providing its security capabilities.
2. A mutual authentication is executed between the UE and the CN.
3. If authentication is successful, the UE and the CN negotiate the algorithms to use for encryption and digital authentication.
4. Once the negotiation is completed, the CN sends the UE an accept attach message.
5. The UE confirms the attach.

Attacks and other failures may happen during any such step. The goal of the LTEInspector methodology is to analyze multi-step protocols to identify vulnerabilities in these steps.

The input to the LTEInspector approach is a representation of each protocol in terms of two finite state machines (FSMs), one for each party involved in the protocol—that is, the UE and the CN (Fig. 1). An FSM is an abstract machine that can be in exactly one state among a finite number of states at any given time. The FSM can change from one state to another in response to some input; these changes are referred to as “transitions.” Preconditions also can be associated to transitions; in such cases, for the input to trigger a transition, the preconditions must be true. Also, as part of a transition, actions can be executed.

FSMs are, thus, a representation well-suited for the analysis of multistep protocols. An example FSM modeling the attach protocol at the UE side is shown in Figure 2. In the example, we use the MME as the party, from the CN, involved in this protocol.

From the diagram, we can see that the UE is initially in a disconnected state and then, upon the phone restart (indicated



2. A finite state machine—such as this simplified example UE FSM modeling the attach protocol—is a representation well-suited for the analysis of multistep protocols. (Image from Reference 3)

by the condition *mobile_restart*), the UE sends an attach request to the MME and transitions to the state in which it waits for the authentication request (that is, the state *UE waits for auth_request*). Once the UE is in this state, different transitions can happen. For example, the UE is restarted (Transition #3) or the authentication fails (Transition #4), or the authentication of the UE by the MME is successful and, as a result, the UE moves to state in which it authenticates the MME (Transition #5).

Thus, the goal of the LTE methodology is to determine scenarios (i.e., sequences of transitions) in which the UE, because of attacks, is unable to reach the final intended state (i.e., the state in which the UE has been authenticated by the MME and the MME has been authenticated by the UE).

To identify such attacks, one must consider the capabilities of the attacker, referred to as “adversarial model” that are relevant to the protocols to be analyzed. Because the focus of LTEInspector is on vulnerabilities in communication protocols (and not, for example, on vulnerabilities in the equipment hardware), LTEInspector adopts the Dolev-Yao attack model.⁴

Under the Dolev-Yao attack model, the capabilities of the attacker include dropping/modifying messages exchanged on the network, injecting false messages, impersonating legitimate parties in communications, and eavesdropping messages.

Under the Dolev-Yao attack model, the capabilities of the attacker include dropping/modifying messages exchanged on the network, injecting false messages, impersonating legitimate parties in communications, and eavesdropping messages. Also, under this attack model, the attacker adheres to the assumption that the attacker is unable to decrypt messages without possessing the proper decryption keys and cannot forge the digital signatures of legitimate parties without possessing the keys used for the signature.

The FSM extended with the inclusion of the adversarial model is then given as input to the NuSMV model checker,⁵ together with properties to be verified. Then, by using an iterative process known as “property refinement,” each property of interest is verified separately.

In property refinement, further conditions are added to the property to be verified to exclude spurious cases that can lead to property violations, but which do not represent vulnerabilities. If no violations are detected, the property is considered as verified by the protocol.

On the other hand, when there’s a violation, the model checker returns the scenario that leads to the violation of the property. The scenario is then analyzed via a cryptographic verifier to determine whether the violation still occurs under the cryptographic assumptions about the attacker. If this is the case, as a last step, the attack is checked in an actual testbed with commercial UEs to determine whether the attack is possible in practice, as commercial UEs may implement additional defenses.

By using LTEInspector, several new vulnerabilities were identified that can be exploited in actual attacks (see Reference 3 for details on these attacks). Most such vulnerabilities were due to the lack

(Continued on page 26)

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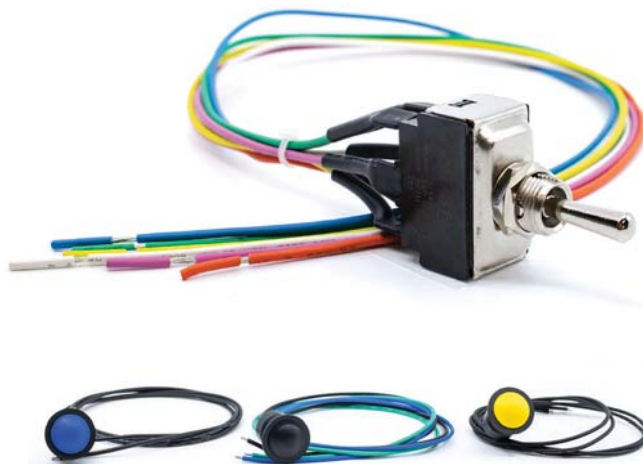
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(Continued from page 23)

Extracting models from actual implementations of the protocols has the advantage that automatic or semi-automatic approaches can be used, such as the recent ProChecker methodology.⁹

of deployment of well-known security techniques for some messages exchanged by the protocol. Examples include lack of replay protection and lack of digital signature for certain broadcast messages, such as the paging messages broadcast by cellular towers to notify UEs of calls and SMS.⁶

Starting from LTEInspector, other notable methodologies were designed, including 5GReasoner,⁷ which extends LTEInspector by modeling, in addition to the NAS layer, RRC, and a fuzzing-based approach to identifying design and implementation vulnerabilities in 5G code by carriers and device vendors.⁸

Creating FSM Models of Communication Protocols

The application of formal methodologies, like LTEInspector and 5GReasoner, requires formal models of the protocols to be analyzed. Based on our experience, such a model can be extracted from the standardization documents, as in the case of the model developed for LTEInspector, or from the protocol implementations. Both approaches have challenges.

Extracting models from standardization documents requires a huge amount of manual effort, as these documents are often very large and convoluted. Addressing this issue would require the design of specialized natural language processing approaches, perhaps based on artificial-intelligence/machine-learning techniques.

One advantage, though, is that the analysis performed on such models allows one to identify errors and ambiguities in the standardization documents or other specification documentation. Indeed, among the new vulnerabilities found by LTEInspector, more than half were due to issues in the specification from standardization documents.

Extracting models from actual implementations of the protocols has the advantage that automatic or semi-automatic approaches can be used, such as the recent ProChecker methodology.⁹ ProChecker leverages the testing infrastructure used for the code to extract from the implementation of an FSM model of the protocol. Because the model is extracted from the implementation, it's more fine-grained than a model obtained from the natural language specification.

Using a more detailed model allows one to identify vulnerabilities that aren't identified by more abstract models. For example, when applying ProChecker to an industrial codebase that has a size of around 80 GB, implementation of the NAS layer identified three new protocol attacks. These weren't identified in analysis by LTEInspector using a more abstract model extracted from the standardization documents, as well as six implementation issues.

One disadvantage is that the extracted model may be very large, which results in scalability issues with the formal analysis tools used. Furthermore, the model may contain unnecessary details that make it more difficult for the programmers/software engineers to understand the vulnerabilities.

Key Insights

Ensuring that cellular network protocols are free of vulnerabilities of varying nature is a challenging task that requires the use of several techniques. For example, memory vulnerabilities, such as buffer overflows, are today well-understood and identified in various ways, such as by fuzzing testing. On the other hand, logical vulnerabilities, e.g., lack of digital signatures on messages, are more difficult

to identify. Formal verification methodologies, like the ones discussed earlier, are more suitable for identifying these vulnerabilities.

However, the use of these methodologies requires extensive domain knowledge to determine the proper abstraction level(s) for the model and the properties. In general, having an abstract model is useful in defining an initial set of relevant properties and verify whether the protocol, as initially specified, has vulnerabilities. Then a more detailed model can be extracted from the implementation and analyzed by refining the properties defined for the abstract model. In addition, the model extracted from the implementation can be compared with the abstract model to detect whether the implementation is noncompliant with the specification.

To conclude, we have promising techniques and methodologies, and, hopefully, research by industry and academia will enhance and engineer them for practical use. ■

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EMI SHIELDING for Drones and UAVs

Most every electronic circuit will pose the threat of EMI radiation on other circuitry, with drones and UAVs being particularly susceptible. There's one simple but important solution: implement EMI shielding.

Most drones and unmanned aerial vehicles (UAVs) rely heavily on seamless communication from ground systems. Cell-phone towers, buildings and large metal structures, high-voltage power lines, and a high concentration of Wi-Fi networks in an area can cause serious electromagnetic interference (EMI) in drone performance.

EMI effects on drone operations are unpredictable. They can severely disrupt a drone's navigation system by shifting the drone's compass out of alignment. When flying close to large structures,

EMI can degrade the quality of GPS reception of a drone. It also may disrupt the communication between a drone and its controller.

There's a growing trend toward drones/UAVs being used to inspect utility areas such as electrical power grids and pipelines. Infrastructure like cell towers also need visual inspection. This is far less costly than a "truck roll" to a site.

A dilemma occurs when a cell-tower antenna is being visually examined by a drone/UAV. The cell-tower transmitting antennas can easily exceed the interference threshold for these aircraft. Usually

the drone/UAV will return to its home base when sensing a high EMI signal.

Often, larger drones have an exterior fuselage made from a light metal or a thin aluminum foil to help prevent lightning-strike EMI damage.

This article takes a look into various types of EMI fields and some solutions to mitigate those fields to prevent failures in drone performance.

Magnetic EMI Fields Affecting Drones with Onboard WPT Systems

Drone chassis are typically designed



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1. This DJI F550 drone has WPT charging capability. (Image from Reference 1)



with non-metallic materials to reduce the weight and size of the aircraft. Wireless power transfer (WPT) has kilohertz-frequency magnetic fields that can easily penetrate the drone body and disturb internal drone electronics. One good example of such drones with WPT is the DJI F550 drone (Fig. 1).

Three test cases for EMI were examined:

- Test case #1 had the coupled coils in free space
- Test case #2 showed that the performance of magnetic coupling to wirelessly charge the drone had poorer coupling performance due to the copper PCB. This case had a lateral misalignment of the coils equal to 200 mm.
- Magnetic shielding was employed in test case #3, which reduced any coupling problems. The system performed close to coupled coils in free space (just like test case #1). This case had a lateral misalignment of the coils equal to 200 mm (Fig. 2).

Magnetic field levels in the WPT drone example, along with the associated EMI problems, were studied in the presence of the metallic drone frame and engines. The magnetic field was reduced in the most sensitive area of the drone, i.e., in the electronics on the PCB and in the

autopilot system, by using a thin layer of ferrite material. This test also limited the effect of the drone's metallic area on the WPT charging system's performance. The presence of a ferrite shield enabled a coupling performance very close to that of test case #1 with the coils in free space.

Calibrating Drone/UAV Compass Far from EMI Sources

Calibration of a drone/UAV compass will play a key role in accurate navigation. Ideally, a drone/UAV compass should be calibrated according to the Earth's magnetic field and free from the influence of external fields. Compass calibration should be performed away from any potential sources of EMI.

In addition, users need to be sure to calibrate the compass away from urban areas. Be away from powerlines, steel girders, or rebar embedded in concrete. An open field with minimal man-made structures will work best. Finally, users must also keep mobile devices away from the drone/UAV while performing the calibration.

EMI in UAVs

Designers should be aware of testing methods for EMI/EMC susceptibility. UAV exposure to EMI/EMC is fairly unknown and could range from non-existent to over 10,000 V per meter if

they fly too close to power lines. Traditional aircraft have several levels of EMI/EMC protection from the individual line replaceable units (LRUs) to the overall fuselage. Commercial UAVs will typically have minimal ability to filter out radiated noise. The true challenge for design engineers, though, is that while they're typically trained on the EMI test method, oftentimes that's not the case when it comes to critical low-cost design methods to avoid EMI susceptibility.

A plethora of electronic components reside in a commercial UAV. The wide variety of components in the UAV provide plenty of opportunities for failure from EMI sources both internal and external (Fig. 3).

EMR/EMI Shielding Solutions

Electromagnetic radiation (EMR) needs to be directed to a particular safe area of a Wi-Fi system, and then absorbed, with the use of proper coatings that can enhance the performance of Wi-Fi in the presence of this EMI. There are three interactive components of EMI emission: the transmitter and receiver sources of electromagnetic energy, and the path for propagating this energy.

We can separate EMI shielding into four entities depending on the frequency range and whether it's continuous or pulse:

- EMI power spectrum shielding, which is for the range 1 to 100 kHz.
- EMI shielding is the radio frequency range 100 kHz to 1 GHz.
- The microwave, and beyond, frequency band of the electromagnetic energy.
- The electromagnetic pulse (EMP), which has a broad frequency band with high-intensity short-duration bursts of electromagnetic energy, such as in a nuclear explosion or an electric discharge.

The Internet of Things (IoT) is becoming more present in our everyday activities, from mobile phones to smart homes and even autonomous cars. Now the ubiquitous applications for drones are beginning to feel the disruptive effects of EMI in IoT applications based on the information received by their sensors.

Embedding the sensor node into a viable case to protect against electromagnetic attacks is a solution that needs some research. A better way to implement this, especially in areas such as drones, which need low weight and small size, is to implement electromagnetic shielding to reduce the electromagnetic field (EMF) and protect sensor nodes from interference.

Designers need to reduce EMF radiation levels from the equipment they're designing as well as mitigate sources of external disturbances to immunize their design.

A shielding effectiveness (SE) parameter describes the performance of the chosen solution and is the most important parameter in electromagnetic shielding materials. The IEEE has a standard for this known as IEEE 299-2006: IEEE Standard Method for Measuring the effectiveness of electromagnetic shielding enclosures.

Flexible EMI Shielding

Shielding layer or layers of Polyaniline (PAni)

PAni and other intrinsic conducting polymer (ICP) materials show potential to replace metal and carbon-based tech-

nologies. These flexible materials provide a lightweight, thin layer of coating to mobile-phone and Wi-Fi devices for EMI shielding and have achieved a variety of S_{21} shielding values. Drones and UAVs will greatly benefit from this lightweight, flexible material.

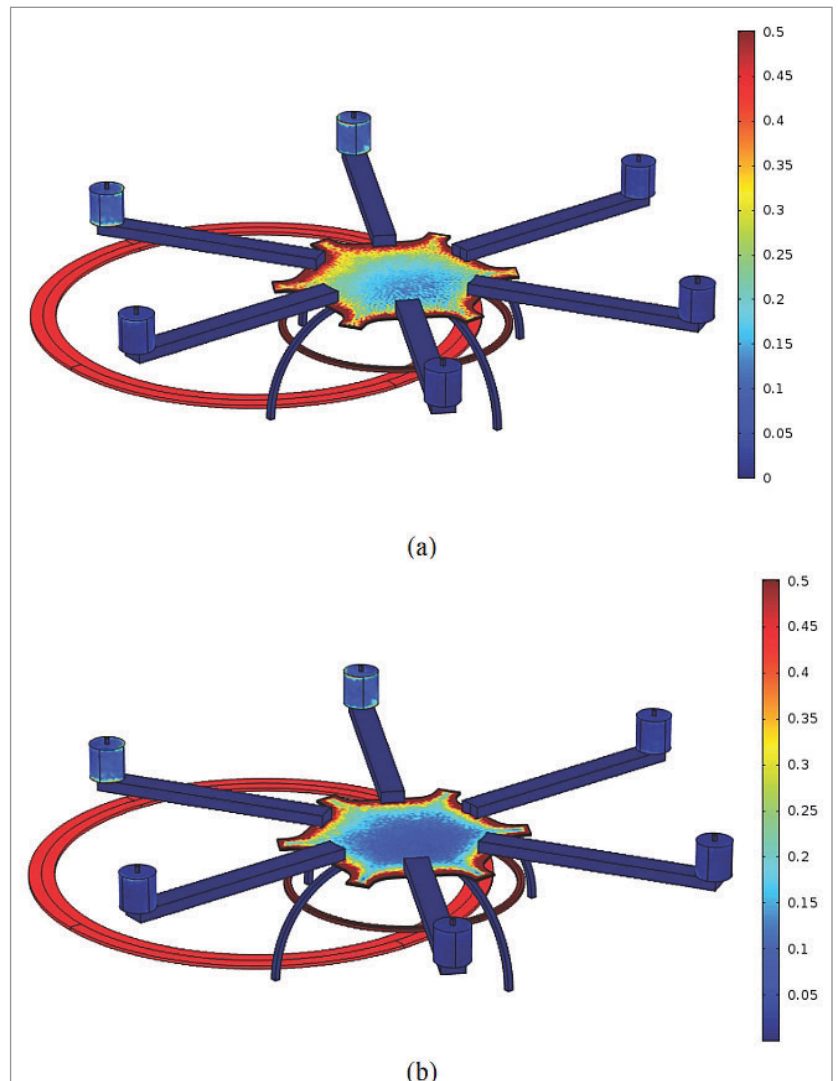
Electrically conductive EMI gaskets

Gaskets will be needed when there are imperfect mating surfaces. For EMI reduction, gaskets must be electrically conductive and flexible.

In more highly conductive gasket materials, there will likely be more susceptibility to oxidation due to the hardness of the oxides. Some oxide layers will remain thin, while others can build up in thickness quickly. This buildup forms an insulation between the gasket and flanges, but that can be overcome by using slow-oxidizing materials or coatings, like nickel, tin, or zinc.

Such EMI gaskets include metal beryllium-copper (BeCu) spring fingers, mesh gaskets, elastomeric gaskets filled with

2. The illustration demonstrates the distribution of induced current density J (A/mm²) on the drone due to a lateral misalignment of the coils equal to 200 mm for test case #2 (a) and a lateral misalignment of the coils equal to 200 mm for test case #3 (b). (Image from Reference 1)



(Continued on page 34)

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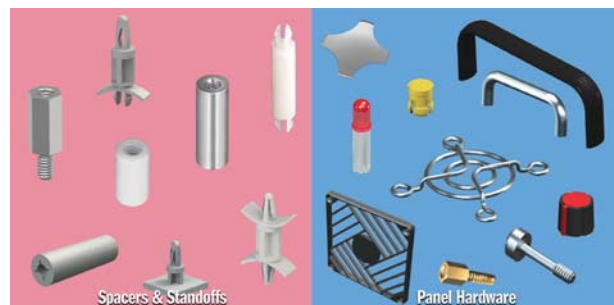
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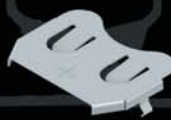
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EMI Shielding for Drones

(Continued from page 31)

plated metal fillers, and electrically conductive caulks and sealants.

Summary

EMI can wreak havoc on flying drones and UAVs. Cell-phone towers and cell phones are ubiquitous and often are powerful sources of EMI to drones and UAVs. So how does this happen if cell phones operate at 1.9 GHz? Intermodulation is usually the primary culprit here. High-voltage lines also may interfere with drone/UAV operation. High con-

centrations of Wi-Fi equipment can be offenders as well. And finally, buildings and large metal structures may reflect EMI sources.

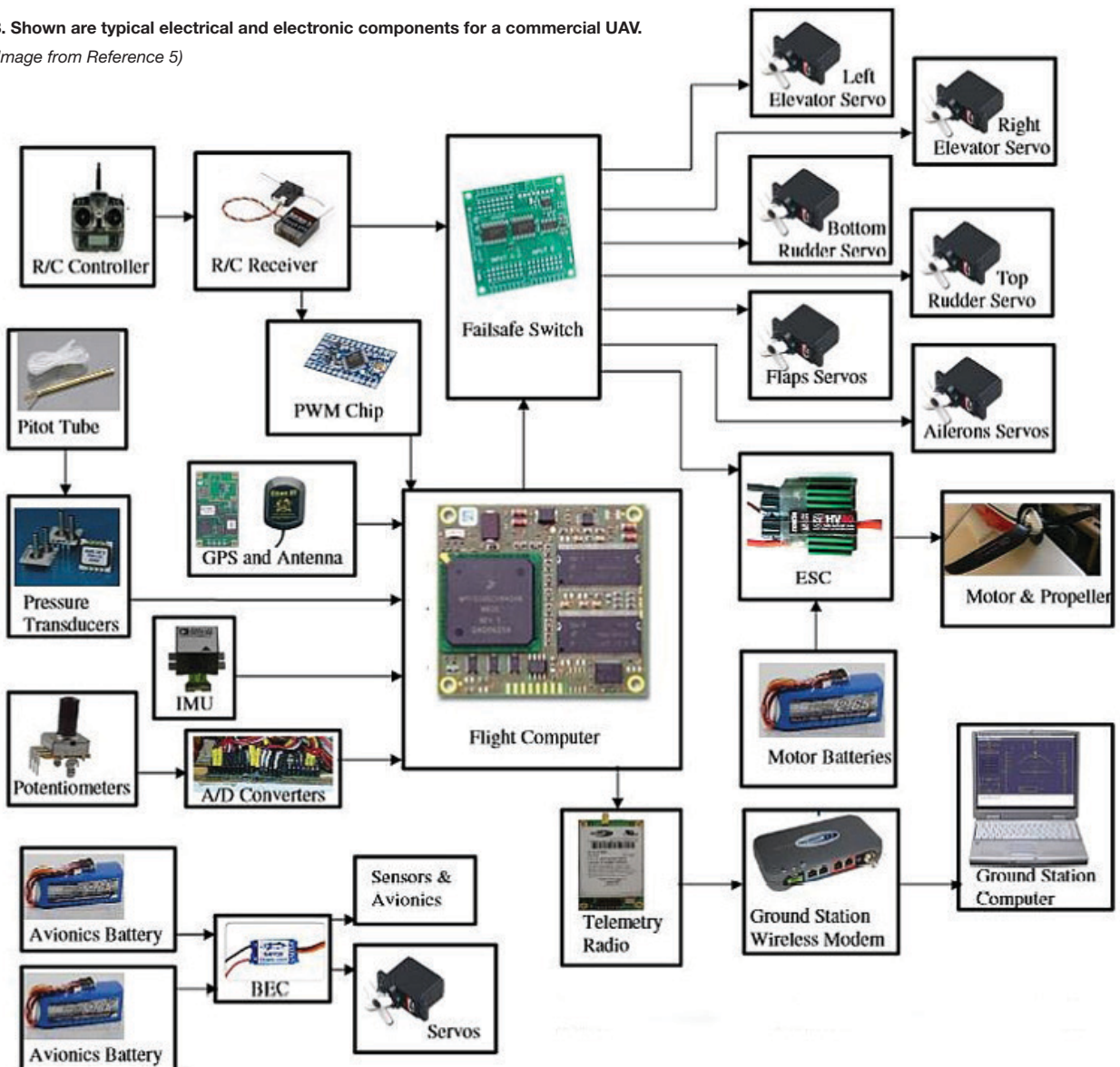
Fear not, valid solutions mentioned in this article will thwart any EMI intrusions on drones and UAVs. Careful drone/UAV design can prevent flight control errors. Even more powerful, potentially catastrophic EMI offenders can be reflected away from sensitive drone/UAV surfaces with the right design techniques discussed here.

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4. Low EMF Three Phase Resonant Magnetic Field Charger for Drone with High Q Reactive Loop Shielding, IEEE Xplore
5. Improving UAV Reliability, DfR Solutions
6. Flying Your Drone in Urban Areas with Heavy Signal Interference, Pilot institute
7. Electromagnetic interference shielding in unmanned aerial vehicle against lightning strike, TELKOMNIKA, Vol.17, No.2, April 2019, pp. 915-919

3. Shown are typical electrical and electronic components for a commercial UAV.

(Image from Reference 5)



Pain Points for RF Product Design

Many unique RF challenges emerge in the development of products, from implementing active wireless technologies to passive RFID tagging. To help address them, it's crucial to engage your RF engineers early in the design and product requirements stage.

Having been involved in developing products in virtually every product category from consumer to medical to commercial to DoD/aerospace, we've discovered that in every case requiring wireless technology, one comes across the seemingly black art of RF system design. Such engineering requires a high level of experience to solve tough problems involving strong fundamental expertise in physics.

The problem set in RF design spans the gamut from implementing active wireless communication technologies (transmit and receive) like satellite, cellular, Wi-Fi and Bluetooth, to passive RFID tagging used in applications such as NFC payment systems or tagging of retail items like clothing. RF system design also includes UL- and FCC-related issues, robust circuit design, and good PCB layout to minimize unintentional radiated emissions and low susceptibility to outside interference.

Here are five of the RF challenges in developing technology products:

1. Issues related to PCB design

PCB design, particularly high-density and mixed-signal boards, presents a big challenge. While physically larger/lower-density boards may be able to leverage off-the-shelf or reference antenna designs, in cases when circuits are compressed, there may not be easy antenna solutions.

Antenna configuration and placement is a major factor in radio performance.

In many handheld and mobile products, severe space constraints make it difficult to incorporate efficient antenna operation due to limitations on antenna size. This can drive the need to use small chip antennas, for example. For monopole antennas such as chip antennas and quarter-wave whip antennas, the PCB ground plane is needed to form the counterpoise half. As a result, PCB size constraints can make it challenging to optimize antenna efficiency and communication range.

In a host of products, the current crop of systems-on-a-chip with integrated radios and antennas are ideal solutions. However, these come with their own challenges especially in high-density systems.

2. Multiple radio systems

The more radios in the system, the more antennas and more intricate the antenna design. This presents challenges in board layout that affect performance and crosstalk noise-related issues that are difficult to resolve. With close placement of antennas, interference between cellular and Wi-Fi can be an issue implying the need for careful antenna placement, orientation, and filtering techniques.

3. 5G system design

Everyone is jumping on the 5G bandwagon for many of the right reasons. 5G builds upon the existing technologies and frequency bands of 4G, but also adds a new band of frequencies in the region of

25 to 40 GHz for super high-speed communication applications. However, high-frequency 5G systems present design and application challenges.

Due to the high frequency, performance is impacted by reduced range—high frequencies don't penetrate the environment as well as lower frequency ranges. It's a tradeoff between range, bandwidth, and transmission rates when considering 5G implementation.

4. System design and regulatory issues

The obvious domain for RF designers is in radio integration. However, such engineers also are called upon to debug problems in passing regulatory requirements. Virtually every product with a wire has run into challenges passing the radiated and conducted emissions and susceptibility requirements.

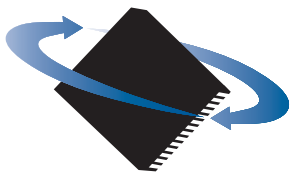
Systems in the corporate lab not impacted by noise get into the agency approval process and find noise problems that can be traced to things as simple as cable layout. RF engineers must assist in design of robust guard-band on emissions and susceptibility to ensure variances in the test setup don't result in failures. Such failures can be a killer due to additional redesign cost and added agency lab time.

It's crucial to engage RF engineers early in the design and product requirements stage to ensure PCB design, layout, and shielding is up to snuff. For example, a design must have sufficient capacitance, good power/ground plane layout, and good signal trace routing to minimize spurious emissions and contamination from external noise sources. Often, cables cause spurious emission failures, too.

5. Finding the talent

Good RF engineers must have a strong background in both electrical engineering and physics. Not only is the competition for experienced talent fierce, but there's a scarcity of RF-focused engineers being turned out of engineering colleges and universities. ■

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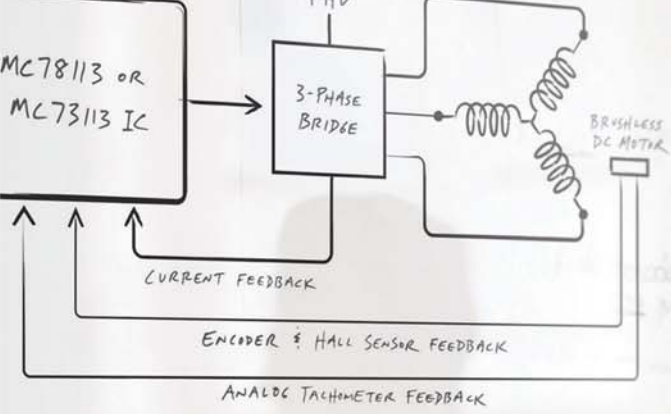
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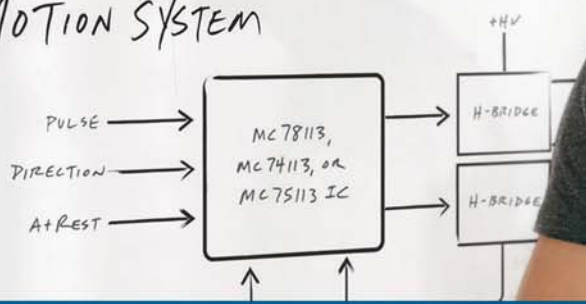
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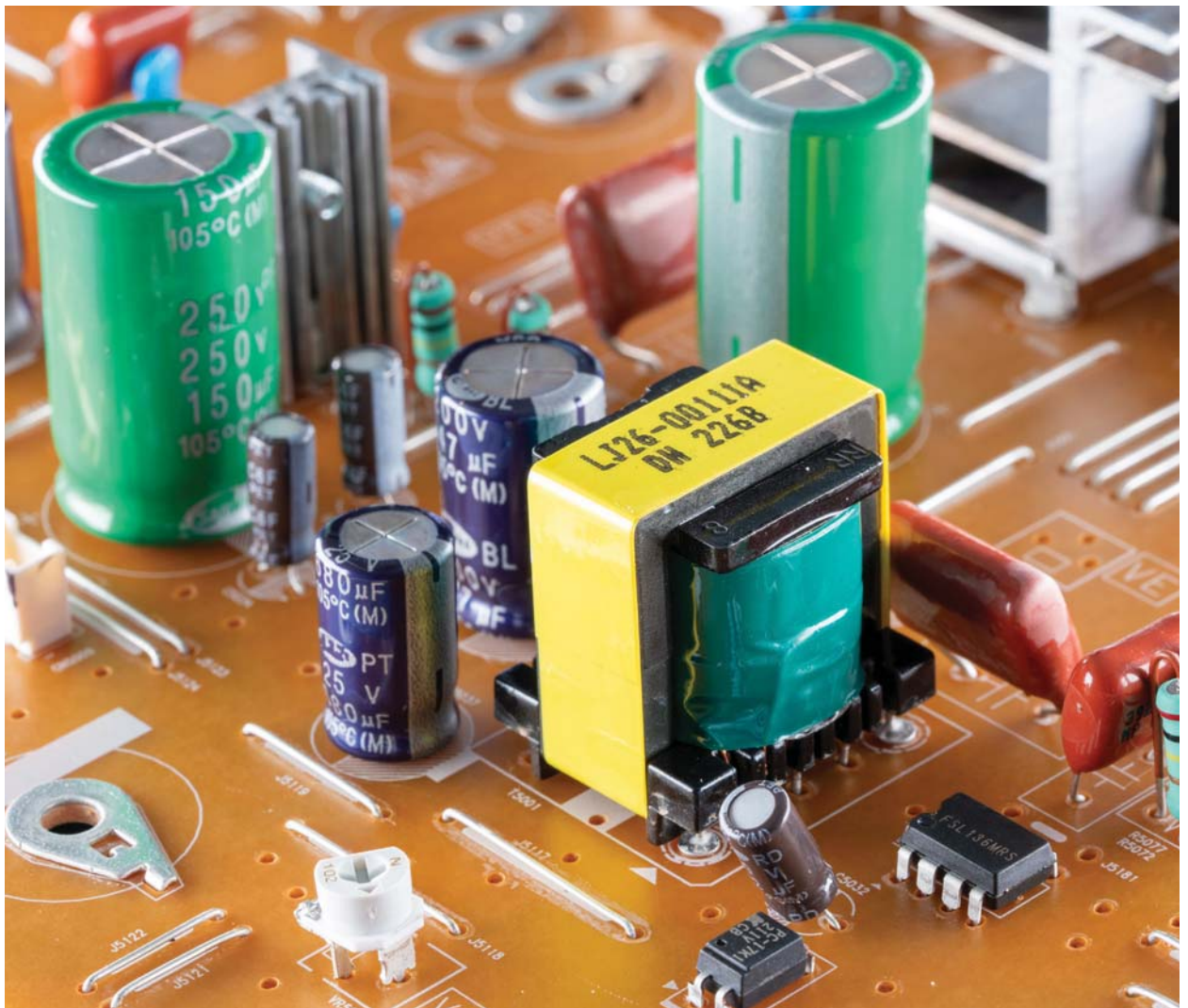


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CONSIDER REALISTIC VOLTAGE SOURCES

When Designing Power Supplies

Real-world behavior must be taken into account to build a reliable power system, and that means an input voltage must be within the permissible range for the given switching regulator.



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A power supply's source, in actual use, is never ideal. The real behavior, including parasitics, must be considered to build a reliable power system. When we use power supplies, we ensure that a dc-dc converter, such as a switching regulator, can withstand a certain input voltage range and generate the required output voltage from it with sufficient current.

The input voltage is frequently specified as a range because it's usually not regulated exactly. For a power supply to function reliably, though, there must always be an input voltage within the permissible range available to the switching regulator.

For example, a typical input voltage range for a 12-V supply voltage may lie between 8 and 16 V. *Figure 1* shows a step-down converter (buck topology) that generates 3.3 V from a nominal voltage of 12 V.

However, when designing the dc-dc converter, it's not sufficient to only consider the input voltage minimum and maximum values. *Figure 1* shows that the buck converter has a switch at its positive input. This switch is turned on or off. The switching speed should be as high as possible so that only low switching losses occur, but this causes a pulsed current to flow on the supply line.

Not every voltage source can deliver such pulsed currents without any problems. As a result, voltage drops occur at the input of the switching regulator. To minimize this, backup capacitors are required right at the input of the power supply. This type of capacitor is presented as C_{IN} in *Figure 1*.

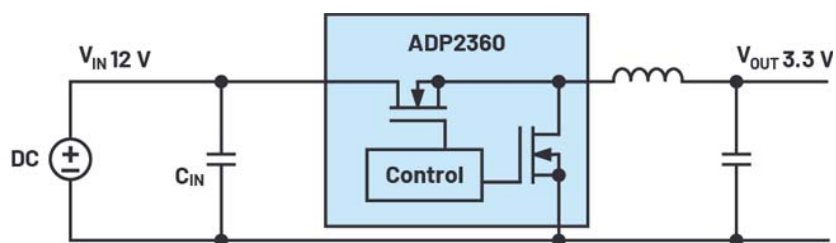
Figure 2 depicts the circuit from *Figure 1*, but this time with the parasitic elements of the supply line and the voltage source itself. The internal resistance of the voltage source (R_{SERIES}), the inductance and the resistance of the supply line (R , L supply line), and any current limitation are key voltage-source characteristics that must be considered to guarantee trouble-free operation of the switching regulator.

For the most part, the correct selection of the input capacitors can ensure proper operation of the circuit. The first approach should be to take the recommended capacitance value for C_{IN} from the datasheet for a switching-regulator IC. However, if the voltage source or the supply line exhibits special characteristics, it makes sense to simulate the combination of the voltage source and the switching regulator. *Figure 3* shows a simulation performed with the LTSpice simulation environment from Analog Devices.

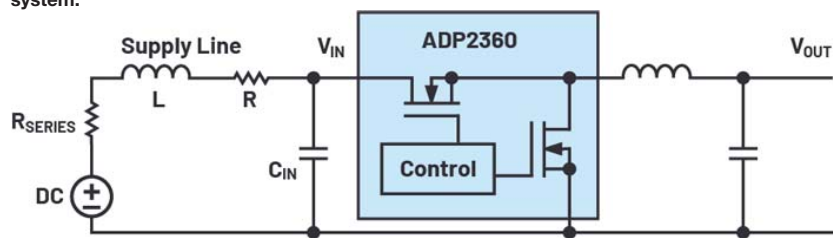
A simulation circuit for the ADP2360 buck converter is shown in simplified form in *Figure 3*—the input voltage IN is generated with an ideal voltage source. Because no internal resistance is defined

for the voltage source and no parasitic values are given for the supply line between the voltage source and the switching regulator, the defined voltage is always applied to the V_{in} pin of the ADP2360. Therefore, it's not necessary to add an input capacitor (C_{IN}).

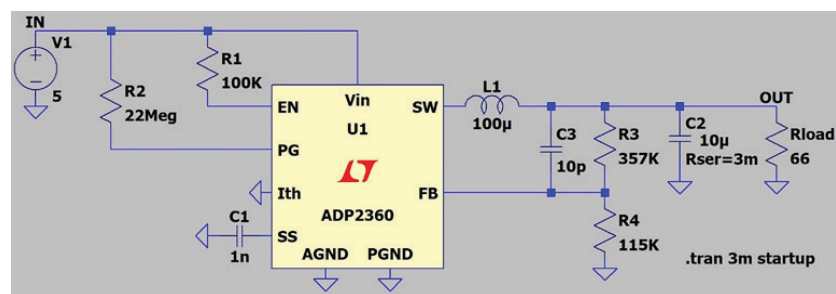
In the real world, though, an input capacitor is always required with a switching regulator because the voltage source and the supply line aren't ideal. If a simulation environment such as LTSpice also is used to check the behavior with different input capacitors, a voltage source with internal resistance and a supply line with parasitic values for resistance and inductance (*Fig. 2, again*) must be used. ■



1. A step-down switching regulator is shown together with the (dc) voltage source of the system.



2. Here's the circuit from Figure 1, but with the parasitic elements of the supply line and the voltage source shown.



3. This LTSpice simulation is checking the behavior of a switching regulator's input voltage.

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The Briefing:

Why Foundries Are Not the Only Culprits Behind Chip Deficit

While foundries are investing aggressively to ease the global chip shortage, other factors are prolonging the supply woes, from tight supplies of raw materials to a lack of back-end packaging and test capacity.

The global chip shortage has plagued the electronics industry for most of the year, wreaking havoc on the auto industry before cascading into other sectors, such as consumer electronics, where even Apple has started to feel the pain.

The main culprit has been the lack of front-end production capacity at foundries. While contract chip suppliers are investing aggressively in fabs to turn things around, it can take a long time to increase the industry's output.

But other parts of the supply chain have also emerged as bottlenecks. Shortages persist in blank silicon wafers that are processed and diced into chips. There are also supply constraints for substrates, chemicals, and resins used in chip packages. A shortage of capacity for back-end assembly and testing, compounded

by snags in the supply chain, has also become a chokepoint. All these factors are leading to higher costs and longer lead times.

“Like wafer fab capacity, there is a need for expanded packaging capacity. However, the margins in assembly and test are a fraction of those in wafer fabs, so there is more hesitation to add capacity speculatively. There also is a shortage of assembly equipment, with some lead times increasing” to more than three months, said Mark Fulthorpe, automotive analyst at IHS Markit. The chip shortage is not expected to end until at least 2022.

In this gallery, we look at some areas of the supply chain outside foundries dragging out the chip shortage. Check back in on *Electronic Design* online in the future as we follow up on many of these topics.

Image courtesy of Soitec



▲ Silicon Wafers

Chip foundries run on vast amounts of electricity, water, and raw materials such as chemicals, gases, and silicon wafers. Intel, TSMC, Samsung, and other chip manufacturers buy polished plates of raw silicon and scorch billions of transistors on the surface before slicing them into logic, memory, or other types of chips. The blank slabs of silicon (or other materials) come in diameters of up to 300 mm.

Global shipments of silicon wafers soared 6% to 3.535 billion square inches in the second quarter of 2021, racing ahead of a record set in the first quarter, according to SEMI, a trade group that represents companies from every sector of the electronics industry's supply chain.

Globally, shipments of the raw wafers increased 12% compared to a total of 3.152 billion square inches in the same quarter last year. That highlights how GlobalWafers, Soitec, Siltronic, Sumco, and other industry players have ramped up to meet demand.

The trade group said that the global supply of 200- and 300-mm silicon wafers is "tightening" due to the unrelenting demand over the last year.

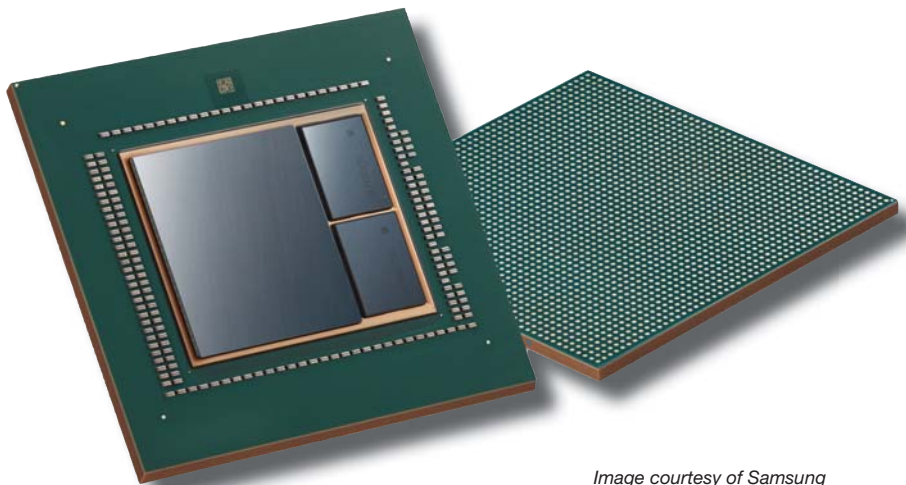


Image courtesy of Samsung

▲ Package Substrates

One of the major chokepoints in the industry is in substrates. A surge in global demand—coupled with various snags in the supply chain—is sending semiconductor companies scrambling to buy this indispensable part.

A substrate serves as the base of a computer chip's package, linking it to the circuit board (PCB) in a system. A substrate consists of many different layers, each of which incorporates copper traces and other interconnects. These wires serve as high-speed electrical con-

nections from the chip to PCB. Laminate substrates are key components of flip-chip ball-grid-array (BGA) packages.

The supply chain woes are centered on a shortage of Ajinomoto build-up film (ABF) substrates. Top semiconductor firms such as AMD, Broadcom, Intel, NVIDIA, and Xilinx rely on these substrates to roll out many of the most advanced chips in the world. But substrate manufacturers (largely located in Japan) have been averse to invest in more capacity due to concerns about a future glut.

(Continued on page 46)

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Chip Supply Deficit

(Continued from page 43)

Some chip vendors are taking matters into their own hands. In April, Lisa Su, AMD's chief executive officer, told analysts that it would intervene directly to increase capacity at suppliers. "On the substrate side, in particular, I think there

has been under-investment in the industry," she said. "We've taken the opportunity to invest in some substrate capacity dedicated for AMD, and that will be something that we continue to do going forward."

Intel is also ramping up its internal assembly and test operations to help improve the availability of substrates. In August, CEO Pat Gelsinger said this has helped Intel get its hands on "millions" of additional substrates for its devices.

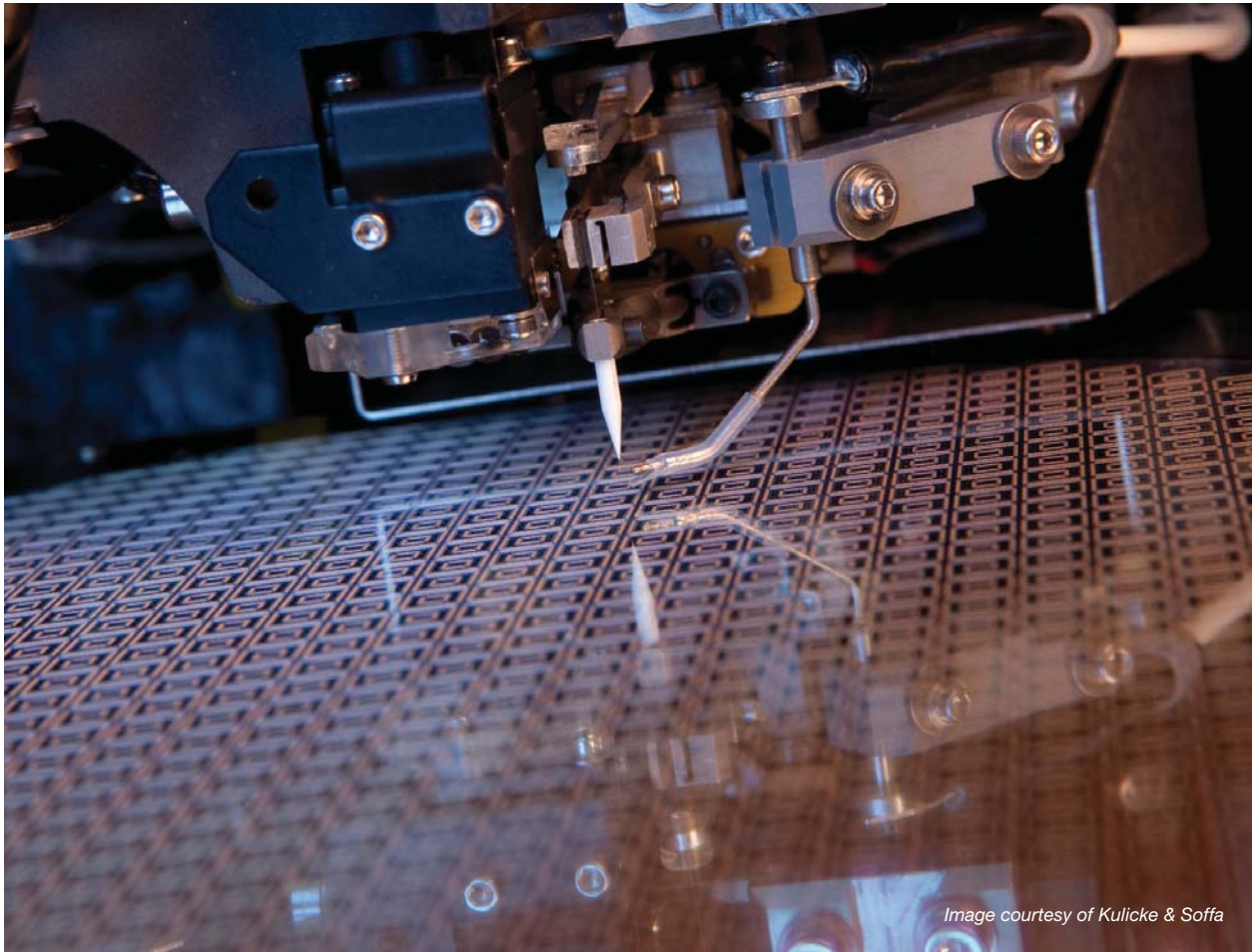


Image courtesy of Kulicke & Soffa

▲ Wire Bonding

Wire bonding is the process of stitching one chip to another chip or substrate using fine wires. Chip packaging giant ASE Technology and others warn wire-bond capacity is severely constrained, largely due to the boom in the automotive chip market.

Wire bonding is used to manufacture many different types of packages, including quad-flat no-leads (QFN) and quad flat-pack (QFP), both of which belong to the "leadframe" category of packaging technologies. Leads on the leadframe are

connected by fine gold or copper wires to the I/O terminals on chips using tools called "wire bonders."

Wire-bond packages are widely used in chips based on legacy nodes, such as power-management chips in short supply for cars and consumer electronics. They are also frequently encapsulated in resin or other types of molding for increased rigidity.

"Capacity remains tight," Ten Wu, ASE Technology's CEO, said on a recent conference call, adding that it is seeing longer lead times. "We believe the

wire-bond shortage will last through the whole of 2021."

Part of the problem is that it has become more of a challenge to procure wire-bonding equipment from Kulicke & Soffa (K&S) and other specialty semiconductor gear makers to help meet soaring demand.

"The industry still has a shortage of back-end capacity and it still needs a lot of equipment from us," said Fusen Chen, chief executive officer of K&S, on a quarterly conference call with analysts in August.

Epoxy Resin and Plastics ▶

After the silicon die is attached to the leadframe or substrate with bonding wires, the final chip is then encapsulated. Usually, it is placed in a case molded from epoxy resins, with only the leads protruding out from the edges of the package in the case of QFN, QFP, or other leadframe packages.

Conversely, the leads in a substrate-based package such as the BGA take the shape of small bumps or balls instead of bonding wires.

Industry analysts say the chip sector is being hit by higher prices and increased supply chain hiccups for high-grade resins and plastics used to encapsulate and protect chips. Global demand for resins used not only in chip packaging but also automobile parts and industrial pipes is outstripping supply, according to market research firm AlixPartners.

“Frankly, this has potential to become a hidden version of the semiconductor crisis for many of the same reasons,” warned Marc Iampieri, senior analyst for operations, transportation, and logistics at AlixPartners.

“Rising demand for plastic products combined with recent supply disruptions has led to complications around quality, cost, and timeliness of delivery.”

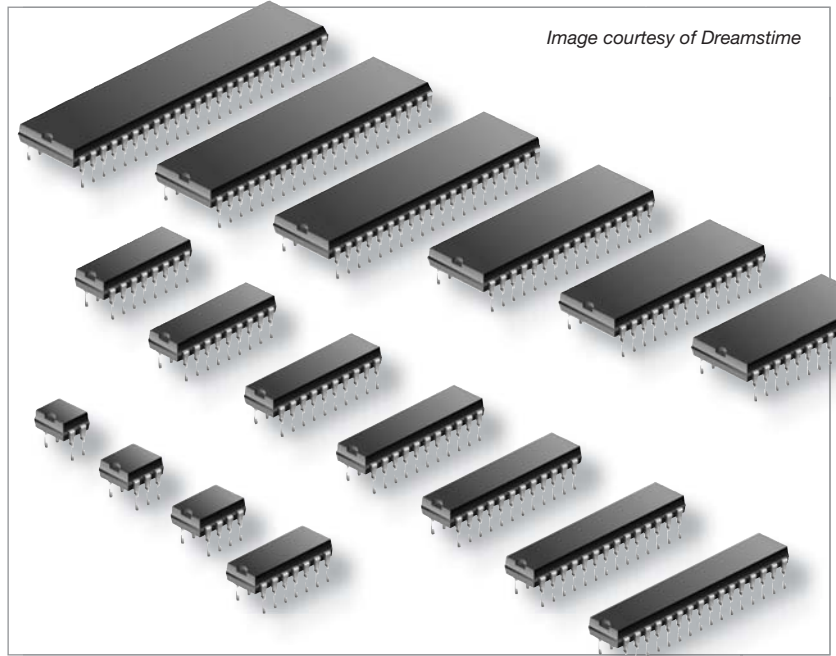


Image courtesy of Dreamstime

▼ Chip Testing

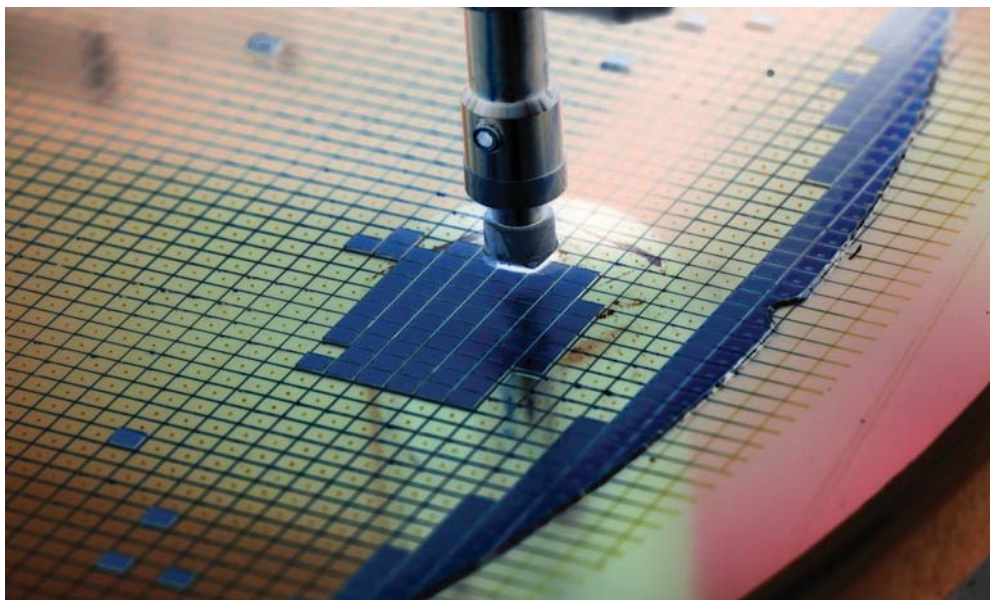
The final phase in manufacturing a chip is testing, which has also become a bottleneck for the semiconductor market.

Outbreaks of the coronavirus in South-east Asia, a major center for outsourced chip assembly and testing, has complicated the chip shortage. The flare-up has slowed operations in the region.

As a result, semiconductor companies that can afford it are bringing more back-end testing and assembly operations in-house to help prevent potential bottlenecks as the sector's wafer supply improves.

Delivery times for chip testing equipment are also up, as companies struggle to fill orders fast enough. “Lead times have

pushed out because of the very, very tight supply chain environment we're dealing with,” said Sanjay Mehta, CEO of Teradyne, on a conference call with analysts in July. He said that it usually only takes around three months to supply a chip testing system to a customer. But supply constraints have increased its lead times by more than a month on average, resulting in delays of more than 20 weeks in some cases. ■





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How Working Remotely is Spawning a **DESIGN REVOLUTION**

The forced isolation from COVID brought a perfect storm of need to foment a greater acceptance of advanced design and development tools.

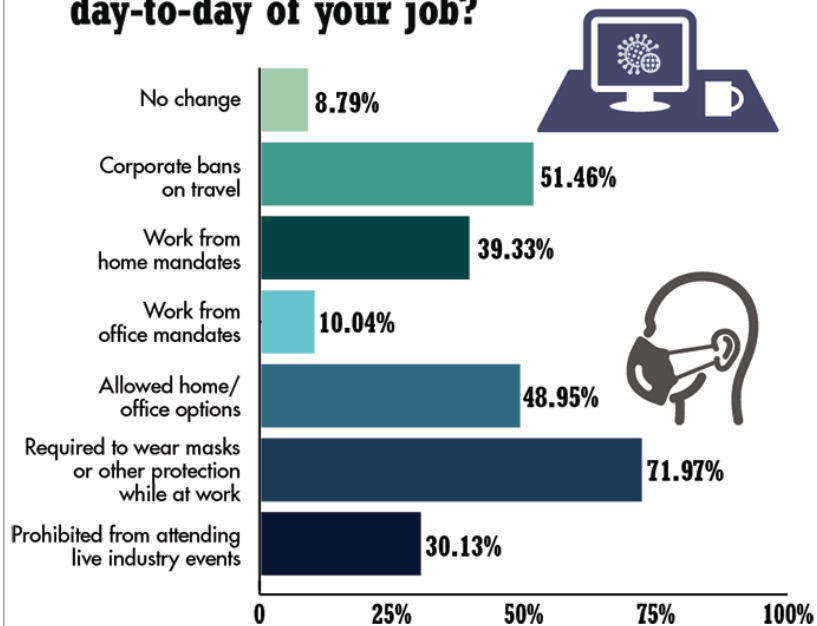
The saying “every cloud has a silver lining” is very apt for the situation we’ve found ourselves in during this age of COVID-19. The forced isolation and need to separate has caused a great deal of hardship on every level and in every venue of society. However, the need to interact at both a social and business level forced us to investigate

solutions such as telepresence and other collaborative tools to operate.

Holding meetings with people and sharing data with others online wasn’t a new concept a couple of years ago—that movement was already on its way to more widespread adoption. Companies were using these tools to do business before COVID-19, but they were mostly mul-



How has COVID-19 affected the day-to-day of your job?



1. Team separation was among the biggest COVID-19 impacts on day-to-day work.

(46.93%), prohibitions on attending live industry events (29.96%), being allowed to work from a home office (50.72%), and even work-from-home mandates (34.84%). This pretty much forced everyone with the ability to create a home office to make one.

The tools required to perform work vary from company to company and industry to industry, but the common-denominator includes the ability to communicate with team members, schedule and manage event timelines, and share data and documents. These needs are often dealt with using separate software-based solutions, but a growing number of all-in-one collaboration suites are emerging.

This multifaceted need is driving even more functionality into currently available solutions. The collaborative-tool marketplace is a relatively new one, and like many software-based industries, far from mature. Many people now routinely perform a significant number of tasks using collaborative tools—a number that will

grow in both number and depth as the tools continue to mature.

When we asked our engineering audience about the collaboration tools they currently use (Fig. 2), email led the list at 96.22%, beating out the telephone (74.59%) and texting (69.37%). Video conferencing has become a primary tool for both social interaction and business, coming in at number two with 79.82% of our respondents using it. This underscores the desire for the highest level of interactivity possible in interpersonal communications.

The next island of responses involved tools used to conduct business. The need to schedule and plan, to share files and documents, and to meet other people in a common industry is important for a business to operate. Tools for cloud-based file and document management (35.32%) narrowly edged scheduling and planning tools (35.32%), followed closely by virtual-event platforms (30.81%). This shows that many functions traditionally done face-to-face are being done virtually, successfully.

(Continued on page 54)

tationals with far-flung principals and high-end freelancers who needed to be everywhere.

The pandemic created a “perfect storm” of need that significantly increased adoption of remote tools, causing additional development in a fledgling industry. The latest collaborative tools are not only useful for telepresence, they’re also fomenting a design revolution based on real-time design and manufacturing.

Impacting Work

In our 2021 Salary Survey, we asked our engineering audience about how COVID-19 affected their day-to-day job (Fig. 1). The most prevalent business actions quoted included corporate bans on travel

FAQ

UNDERSTANDING THE BENEFITS OF DIN ENCLOSURES

DIN enclosures are widely used in Europe and are growing in use in a broad variety of OEM systems across the world. These enclosures can be customized and fabricated to customer needs and specifications in OEM quantities.

What is DIN mounting and why should I consider using it?

DIN is a metal rail standard widely used for mounting industrial control equipment inside of controls panels. They are broadly used in Europe for both industrial and home automation applications and should be considered whenever you are engineering a system for the global market.

Are DIN enclosures available in enough versions that I can use them in multiple applications?

Since DIN applications are limitless and work for all manner of electromechanical devices including relays, sensing and monitoring devices, timers, transducers, printed circuit boards, housing electrical and electronic systems, and much more, you can find a wide range of products.

Can I incorporate a DIN enclosure without the high cost of specialized equipment?

Absolutely. Because DIN enclosures are widely used in Europe, they are readily available in a wide range of sizes and designs, choices of cover styles, terminal-to-board connection options, and 35mm DIN rail or panel mount configurations. For this reason, DIN enclosures are typically very economical, easy to assemble and install, and provide integral, ready-to-wire terminals in an attractive package. Because they are used globally, the level of quality meets or exceeds national and international standards for performance and safety.

What types of materials are the enclosures made from?

Depending on the series enclosure you need for your application, housing shell materials are generally glass-filled polyamide or glass-filled polycarbonate. Terminal materials include tinned bronze, brass, or steel with chromated steel screws, and spring terminals of stainless steel.

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What if I have a custom application?



Shown are two customization application examples.

Do DIN enclosures come with extended environmental protections such as temperature and moisture?

Can I incorporate DIN components into my IoT system?

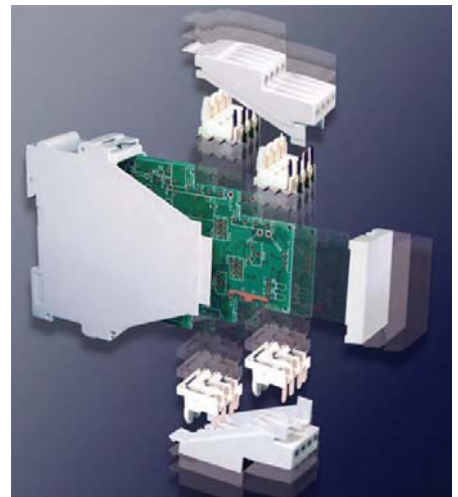
I have a printed circuit board that I would like to convert to DIN rail. How do I incorporate a DIN enclosure into my design for holding the PCB and to make connections between the board and the outside of the enclosure?

Customization is fairly easy (see Exploded View). When working with the right supplier, they can cut special holes and cutouts for operating, setting, or indicating components that you wish to install, as well as include ventilation slots or special machined entrance points. Terminals can be marked for quick identification and efficiency in wiring as well. Even instructions and custom markings can be imprinted on the enclosures. Some enclosure manufacturers, such as Altech Corp. offer enclosures that can be molded in custom colors and custom configurations when ordered in OEM quantities. Further, some enclosure series offer a modular design that allows the user to incorporate different connection systems such as plug-in terminal blocks with screw or spring terminals (push-in). Series that include different switch cabinet enclosures, distribution enclosures, and a mounting rail bus system—for multifunction, compact, modular, or custom solutions are available.

DIN enclosures are generally meant for use in panels so water protection is not necessary. The enclosures' terminals are usually IP 20 rated to be touch proof and meet VBG4 as well as other European accident prevention requirements. Temperature ratings, depending on the enclosure series chosen can be up to 257 degrees F (125 degrees C) and meet UL94V-O standards.

Since DIN enclosures and components are used around the world, they are perfect for IoT applications that need to have a standard look, feel, and interconnection. Equipment monitoring, building management and safety, home utilities, and other IoT applications can greatly benefit from using DIN enclosures for a clean, attractive, and consistent appearance.

DIN enclosures are made to incorporate specific sizes of printed circuit boards so that they are held securely in place. The PCB must be the correct size to mount properly in the enclosure. They are usually slid into PCB guides so your board may need to be modified to the correct size to fit properly. When choosing a DIN enclosure for an existing PCB you should look for a series that has a similar or larger PCB size as well as paying attention to the board layout and terminal configuration. Integrated terminals in the enclosure allow for different types of PCB connections like machine solderable pins, card edge connections and wire jumper or hand solder connections. These terminals are then terminated outside the enclosure with screw or spring clamp terminals for convenient wiring when the product is installed.

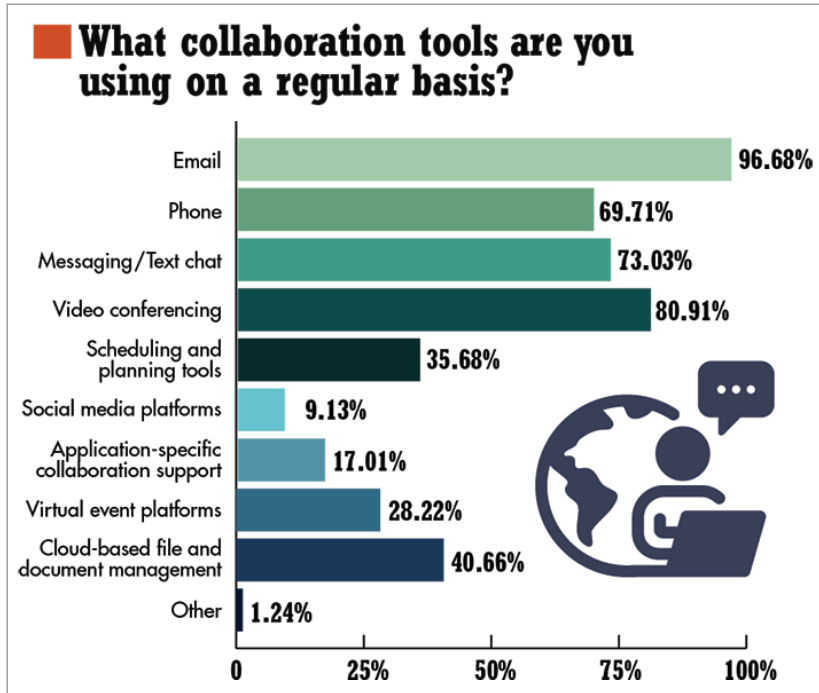


Seen in this exploded view, DIN enclosures incorporate a number of components, most of which can be customized to suit a wide variety of application needs.

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(Continued from page 51)



2. People desire the highest level of interactivity possible in interpersonal communications.

Cascading Benefits

Once people begin using a new tool, they also find new places and ways to use it as a solution for the needs around them. Most tools, regardless of type, offer peripheral benefits. Some of these are very apparent to the user and often are the primary purpose the solution was obtained. However, sometimes it takes a while for a tool's full benefits to be appreciated.

For example, a design and development company may start using a collaborative planning tool to integrate the actions of a separated team, finding significant additional benefit in peripheral functionality. This could be something like the ability to create a bill of materials automatically, without the need of an additional engineer to monitor the process. That either reduces headcount or frees up a needed engineer for another aspect of product development.

This aspect directly addresses the shortage of engineers available to work on any given project, as one engineer can fill many boots with cloud-based development tools. In the survey, the most desired were RF (44.81%) and analog (41.54%) engineers.

Sharing engineering resources isn't just a software solution, because many of the latest benchtop hardware tools such as oscilloscopes can now be operated remotely. This enables an engineer to troubleshoot hardware from the other side of the globe, if there's someone at the place of need who can place the probes for them.

Another significant benefit that comes from migrating your development process online is the ability to perform real-time design-while-build. Your team can utilize the same collaborative development tools they used to create a product, redesigning it on-the-fly to address manufacturing issues, functionality upgrades, or custom orders. The ability to react immediately to initiatives in a proactive manner can be a major force multiplier in a highly competitive marketplace.

Designing the Future

Not surprisingly, this growth in the market for collaborative tools of all kinds—societal and commercial—and the infrastructures needed for them is reflected in the design projects of our audience. When we asked them what

The ability to react immediately to initiatives in a proactive manner can be a major force multiplier in a highly competitive marketplace.

best describes your current design project, 14.81% replied with communications systems and equipment, such as local-area/wide-area networking products, wireless, cellular, RF and microwave, Bluetooth, etc.

Another big area of interest was in industrial control systems and equipment (including robotics) at 9.88%, reflecting the impact of smart systems on manufacturing (Industry 4.0). This area of industry will eventually meld with the aforementioned collaborative development tools, further enabling real-time manufacturing oversight and management, and on-the-fly redesign and custom work.

This also is reflected in the answers to our question about the technologies having a major impact on their designs. Almost half of the responses (40.83%) said it was test equipment, which makes sense in light of the need to test, validate, and optimize these advanced interlaced technologies. Wireless networking came in second at 35.93%, followed by sensor integration at 32.12%, with power management a very important concern at 30.67%. It reflects the growth in the cloud-enabled IoT, the devices, and the infrastructure.

Looking Forward

The impact of COVID-19 may have accelerated the adoption of collaborative design tools, but the functionality they provide, and the cascading benefits offered, would have made the transition to their use inevitable. The latest generation of hardware and software solutions for engineering design and development is only beginning to mature, and the best in many ways is yet to come as these tools more deeply integrate into the engineering community. ■

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VPT'S QUALIFIED PRODUCTS are available in a variety of screening levels to meet specific application needs in addition to qualified radiation-hardened and radiation-tolerant levels specifically designed for space environments.

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DC-DC converters from 1 – 250 Watts, point-of-load converters from 3 – 20 Amps, EMI filters, transient suppressors, inrush current limiters, bus converters, and thermal pads. VPT's VXR Series for rugged military and commercial avionics applications is epoxy-encapsulated with dual-sided thermal conduction and features a wide input voltage range (9 to 60 Vdc). The patented V-SHIELD® epoxy-encapsulated packaging is highly resistant to chemical, solvent, and salt environments, and is fully compatible with high-volume manufacturing processes including wave solder, cleaning solvents, high-pressure sprays, and aqueous wash.



VPT also offers a range of DC-DC converters and accessories designed, tested, and proven for the challenging environment of space. The SVR Series products feature maximum levels of radiation hardening with a Total Ionizing Dose (TID) of 100 krad(Si) and SEE of 85 MeV/mg/cm². VPT's SV Series of products for space feature maximum levels of radiation tolerance with a TID of 30 krad(Si) and SEE of 44 MeV/mg/cm². Both families of space products are based on space-proven heritage designs and available qualified to MILPRF-38534 Class K.

VPT recently released its first commercially available, GaN-based, space-qualified line of DC-DC converters, the SGRB series. The SGRB series is radiation tolerant, achieves high efficiency up to 95%, and includes a fixed-frequency reduced voltage switching topology which results in low input and output noise. This makes it well-suited for space-borne telecommunications where high efficiency, low noise, and radiation tolerance are imperative.

Global customers of VPT include NASA, Lockheed Martin, Boeing, Raytheon, ESA, and Thales. VPT is part of the HEICO Electronic Technologies Group (NYSE:HELA) (NYSE:HEI). More information can be found at www.vptpower.com.

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DESIGN WITH CONFIDENCE

Proven DC-DC Converters,
EMI Filters and Accessories



Avionics & Military Series

- ✓ 1-120+ watts
- ✓ MIL-PRF-38534 Class H and Class K
- ✓ 100% hermetic
- ✓ -55°C to +125°C
- ✓ DLA SMDs available

Hi-Rel COTS Series

- ✓ 5-250 watts
- ✓ Six-sided metal, potted or fully encapsulated V-SHIELD® packaging
- ✓ Rugged environmental screening
- ✓ -55°C to +105°C

Space Series

- ✓ 5-120+ watts
- ✓ Developed for TOR compliance
- ✓ TID: 100 krad (Si)
- ✓ SEE: 85 MeV
- ✓ -55°C to +125°C
- ✓ MIL-PRF-38534 Class H and Class K
- ✓ DLA SMDs available
- ✓ Engineering models typically ship from stock
- ✓ Other radiation levels and custom versions available

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