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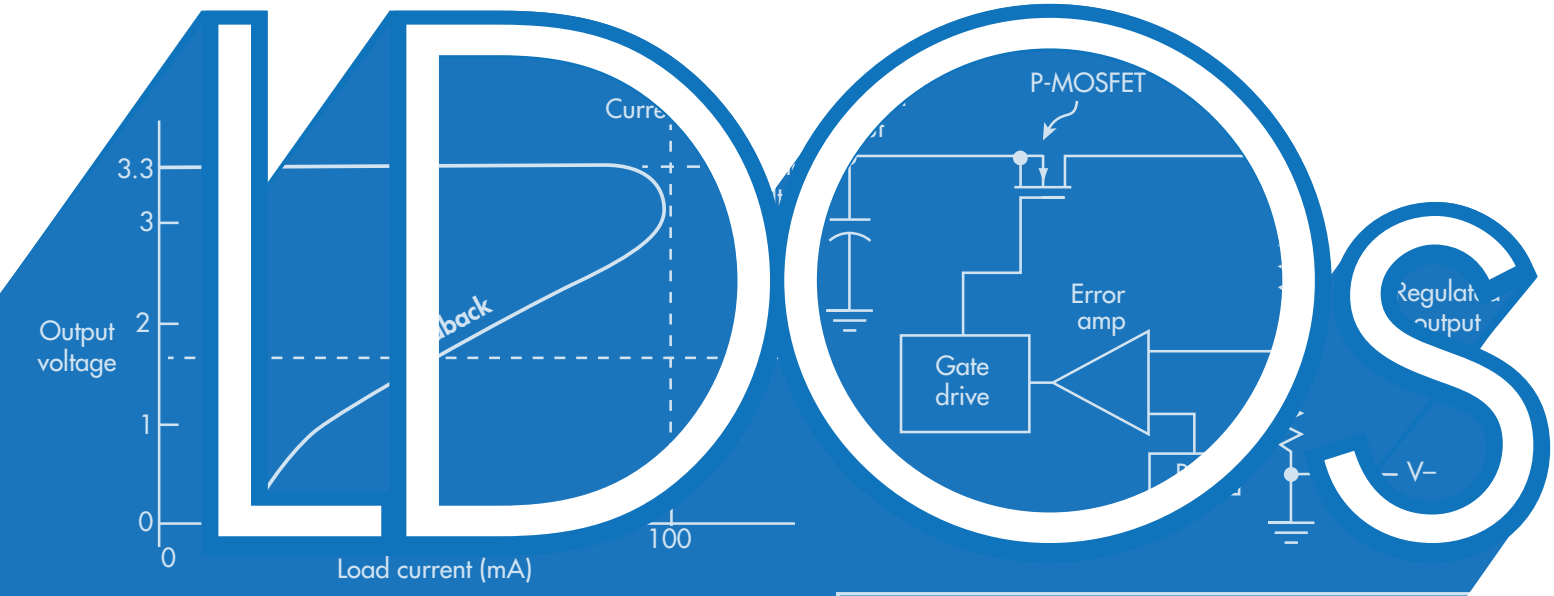
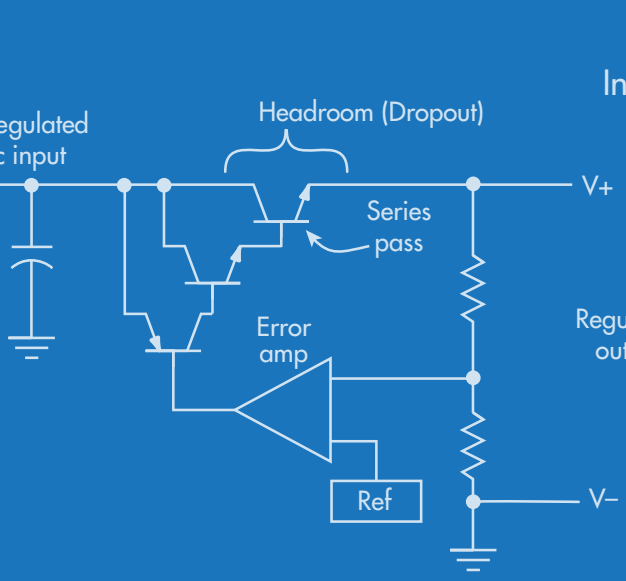
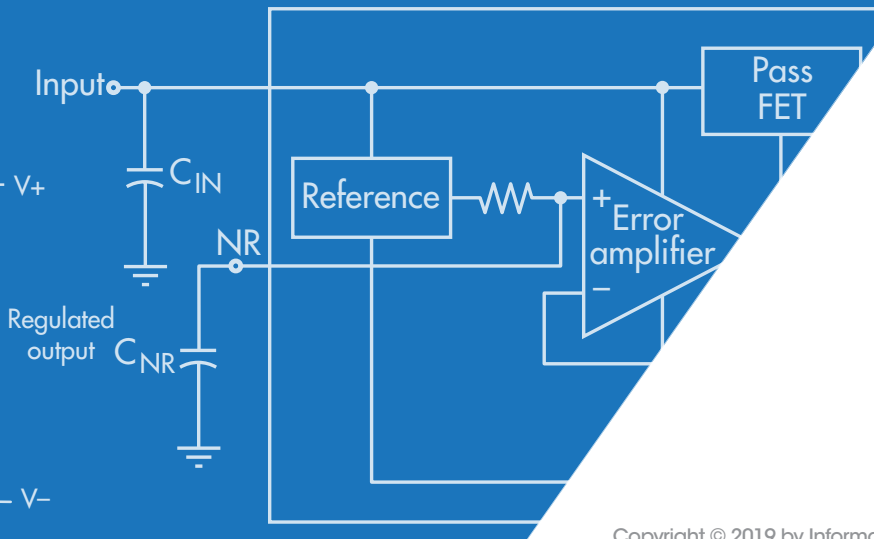
LDOs







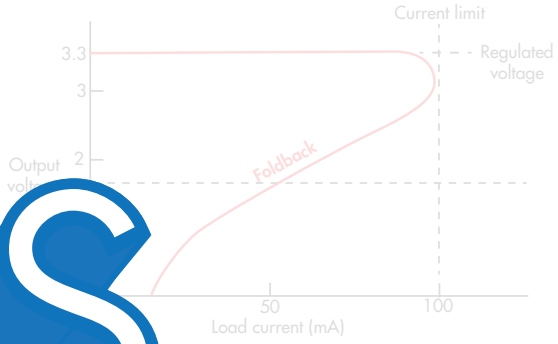
BEST OF...

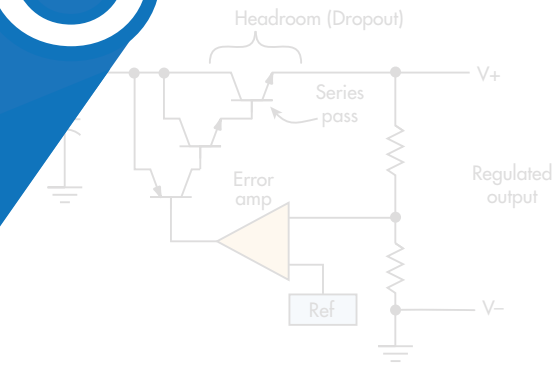
LDOs

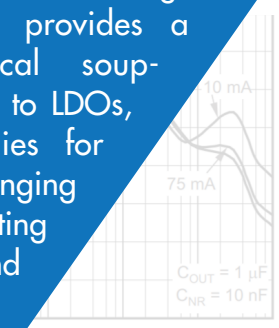
Karen Auguston Field, Content Director

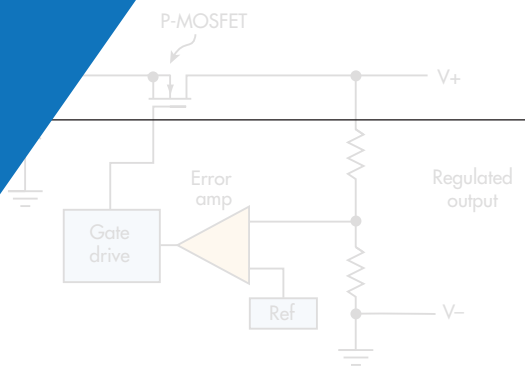
INTRODUCTION

LOW DROPOUT (LDO) linear voltage regulators are prized for their unique combination of low dropout voltage, low quiescent current, fast transient response and low noise. As a consequence, they find applicability in most electronic product designs, so there's a good chance engineers find a need to incorporate into their designs. This E-book provides a highly-practical soup-to-nuts guide to LDOs, from strategies for measuring their performance, wringing the most out of them, to protecting them in harsh environments and applying them to applications such as industrial automation.









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TEXAS INSTRUMENTS

CHAPTER 1:

The Power Behind the LDO

In a nutshell, a low-dropout regulator provides a stable dc output voltage for a stable dc input voltage. What are the basic concepts that drive this ubiquitous device?

BONNIE BAKER, BB@ATW, LLC

You will see a power blog series from me on Power Electronics in the upcoming months. These blogs will post every other week, with topics centering around power supplies. This first installment will be about the low-dropout regulator (LDO).

Succinctly, a dc-dc converter is a power-supply device that does just that: Change a dc voltage to a higher or lower dc voltage. All electronic systems require constant voltage supplies to drive the signal-generating components and devices under their umbrella. Constant is a keyword because it's possible to have a power converter that has a degree of ripple on the output voltage line. If you use a power converter with an output ripple, the challenge is to ensure that this ripple doesn't interfere with the expected signal quality impacting the onboard chips.

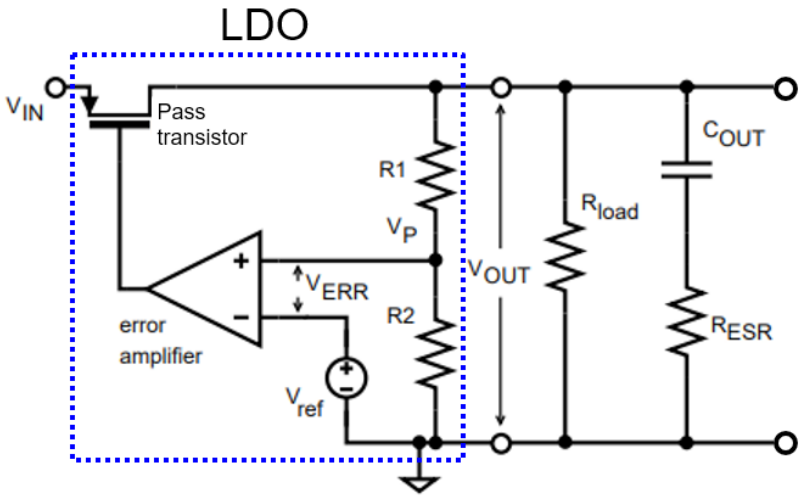
The two fundamental types of dc-dc converters are linear and switcher. With the linear converter, the delivery of the source power is continuous to the load. The pass element for this continuous, linear signal to the load regulates the current flow between the source to the load. The other type of dc-dc power supply is a switcher converter. The switcher-type converter delivers bursts of power as the pass element is switching on and off.

Before we go any further, there are essential converter characteristics to keep in mind as you perform your final selection. The fundamental characteristics for your system requirements are in terms of the input-voltage range, output-voltage level, and current rating. But to dig a little deeper, knowing the efficiency and transient response of the dc-dc converter is equally critical. Finally, the size and cost of your application's components may turn out to be the most critical specifications.

LINEAR REGULATOR

An LDO linear regulator provides a stable dc output voltage for a stable dc input voltage. Usually, you find LDOs in radio-frequency and precise analog applications that have extremely small signal voltages. For these regulators, there's no switching action, and consequently, electromagnetic interference (EMI) becomes a "no-worries" situation. The characteristics that these applications require from their power source are narrow V_{IN} to V_{OUT} differences, high precision, and low noise.

The fundamental construction of the LDO contains a current source, bandgap reference, amplifier, a pair of resistors, and a driving transistor *(see figure)*.



Shown is a simplified LDO circuit.

In the figure, the input voltage (V_{IN}) powers the pass transistor, voltage reference (V_{REF}) and op amp. The op amp forces the non-inverting input to equal V_{REF}, which in turn, from the R_1/R_2 voltage divider, establishes the voltage

value at V_{OUT}. The voltage reference in the LDO is usually a stable bandgap reference that provides a dc voltage at the inverting input of the op amp. The pass transistor provides the output drive current to the LOAD, while R_1 and R_2 hold V_{OUT} steady.

LDOs have a fast transient response to accommodate the needs of FPGA or multicore processors, where fast changes occur in the load. The icing on the cake for LDOs is that they're usually low cost and require fewer external components. There are no switching currents in or out of an inductor, which actually doesn't exist in this circuit, minimizing the LDO's EMI generation.

The efficiency of any power device is equal to:

$$\text{Efficiency} = P_{OUT}/P_{IN}$$

where P_{OUT} is equal to the power out or V_{OUT} x I_{OUT}, and P_{IN} is equal to the power in or V_{IN} x I_{IN}.

Looking at the figure, the V_{IN} must be greater than the $V_{OUT} + V_{Pass\ transistor}$. This relationship locks in the efficiency of the LDO. Basically, the I_{OUT} value tracks the I_{IN} value. In addition, if V_{IN} is much greater than V_{OUT} (which is independent of I_{OUT} and I_{IN}), the efficiency becomes worse. In many circuits, this efficiency disadvantage of the LDO can eliminate it as an option. From there, the only alternative is to use a switching power supply, if you can tolerate the output switching noise.

Which brings us to this column's next installment. In a few weeks, you will see the inner workings of inductive switching supplies.

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CHAPTER 2:

"Come on Feel the Noise"—Measuring LDO Performance

LDOs provide low-noise power in sensitive analog and RF applications. When verifying the device's datasheet parameters, it's crucial to use the proper test setup.

PAUL PICKERING, Contributing Editor

With all due respect to heavy-metal band Quiet Riot (*Fig. 1*), who covered the song in the title (and the British band Slade who did the original 1973 version), if you can in fact "Feel the Noise" from your linear regulator, something is seriously wrong. Although seeing, smelling, or tasting the noise would arguably be worse!

In power-supply design, the linear regulator is widely used to tame the high-frequency transients emitted by high-efficiency switching supplies and prevent them

1. Quiet Riot discussing LDO noise in 1983… ouch. (Courtesy of Ultimate Classic Rock)

from affecting sensitive analog and RF circuits. Unlike a switching topology, though, a linear regulator can only convert a higher input voltage into a lower output voltage—it includes a pass element that dissipates the excess power as heat. A low-dropout (LDO) design reduces the input-to-output voltage differential to 200 mV or less.

When specifying an LDO's noise performance, we can distinguish between two types of noise, each one with its own datasheet parameter.

INTERNALLY GENERATED NOISE

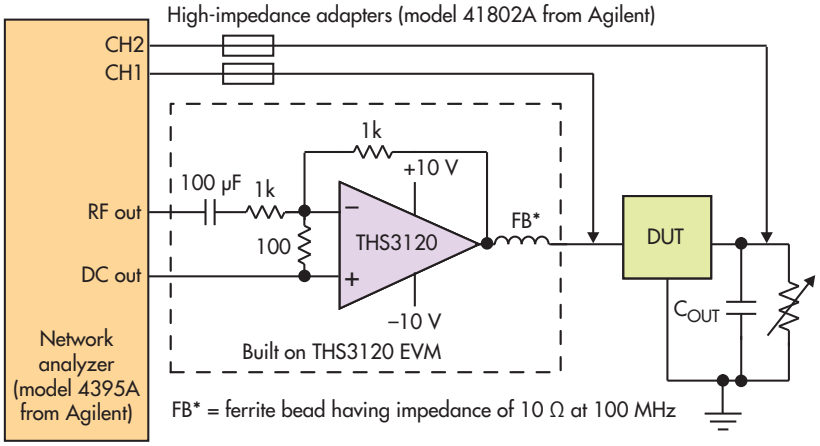
Intrinsic noise is generated in the device itself. It's characterized by an output spectral-noise-density graph in the datasheet, which shows how the noise, expressed in μV/√Hz, varies over frequency. Datasheets typically include several graphs that describe how the output noise varies with output current (I_{OUT}), output voltage (V_{OUT}), and other parameters. Figure 2 shows the spectral-noise-density graph for the TPS7A49, an ultra-low-noise LDO designed for precision instrumentation applications.

Several different physical mechanisms contribute to intrinsic noise. Thermal noise results from the random motion of charge carriers (either electrons or holes) in a conductor; it's proportional to absolute temperature and is independent of current flow. Thermal noise occurs in both active and passive devices; it's one type of white noise and therefore has a flat spectrum.

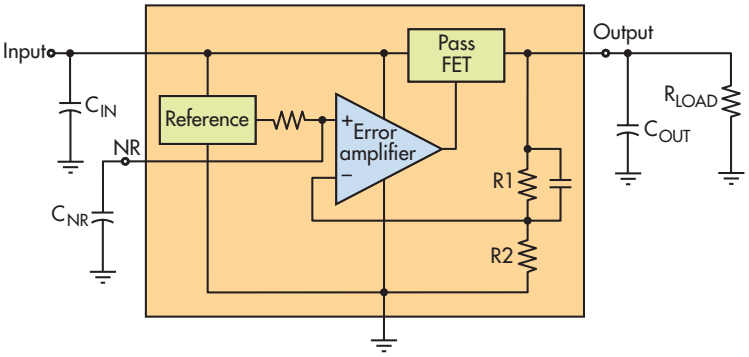
Flicker noise, on the other hand, occurs only in active devices and varies by technology: PMOS vs. NMOS, for example. Flicker noise is proportional to current flow and inversely dependent on frequency; hence, its other name of *1/f* noise.

Finally, shot noise is caused by electrons or holes randomly crossing a potential barrier such as a PN junction. It's also associated with current flow and exhibits a flat frequency spectrum.

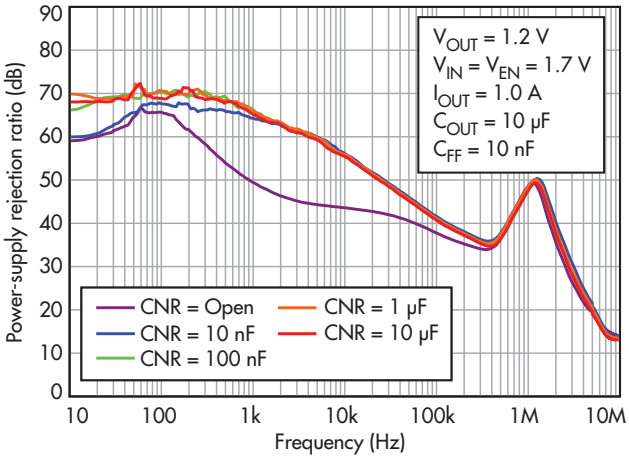
Although every block in the LDO shown in *Figure 3* contributes to the overall output noise, the amplified reference noise forms the largest component because it has a large number of active and passive elements. In addition, any noise appearing on the reference is amplified by the error amplifier and has a disproportionate effect on the noise performance.



2. The TPS7A49 exhibits RMS output noise of 15.44 μV rms from 10 Hz to 100 kHz at I_{OUT} = 1 mA under the specified test conditions. (Source: Texas Instruments)



3. The bandgap reference is the primary source of an LDO's internally generated (intrinsic) noise. The noise-reduction capacitor (C_{NR}) reduces reference noise by combining with the internal resistor to form a low-pass filter. (Source: Texas Instruments)



4. The TPS7A91 graph of PSRR varies with the size of the noise-reduction capacitor C_{NR}. PSRR also depends on the output voltage and other factors. (Source: Texas Instruments)

EXTERNALLY GENERATED NOISE AND PSRR

The power-supply rejection ratio (PSRR), also called the power-supply ripple rejection, describes how well the LDO rejects noise from an external source that appears on its input. This external noise can originate from a switching power supply, parasitic coupling, or elsewhere. The PSRR compares the output ripple and the input ripple over the frequency range of interest for the application.

PSRR is expressed in decibels (dB)—the higher the number, the better the rejection. The equation is:

$$\text{PSRR (dB)} = 20\ \text{Log}_{10}\left(\frac{V_{IN}(f)}{V_{OUT}(f)}\right)$$

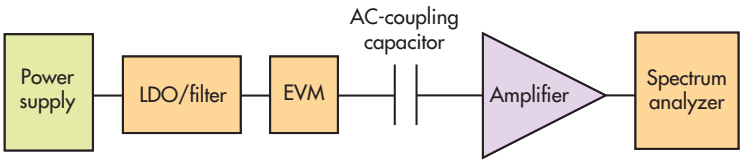
One of the dominant internal sources of PSRR in an LDO is, not surprisingly, the bandgap reference. Any ripple that couples from the input to the reference is amplified and appears on the output, so it's important to have a bandgap reference with high PSRR.

Typically, the solution for both internal noise and PSRR is simply to filter the bandgap with a low-pass filter (LPF). As shown in Fig. 3, this LPF is accomplished by adding an external capacitor (C_{NR}) to the existing internal resistor.

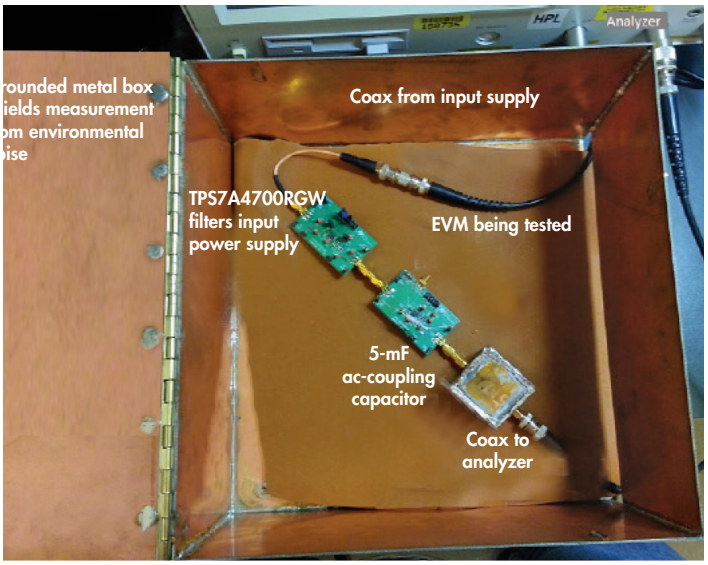
At low frequencies, the LPF reduces PSRR because it passes bandgap ripple in this range. A low-ESR ceramic output capacitor improves PSRR performance: The capacitance value should be chosen based on the frequencies that are important for the application. Finally, careful attention to board layout will reduce the feedthrough from input to output via board parasitics.

As an LDO's load current increases, so does its open-loop output impedance, because the output impedance of its MOSFET pass element is inversely proportional to the drain current. This, in turn, lowers the gain. Increasing the load current also moves the output pole to higher frequencies, which boosts the feedback-loop bandwidth.

Increasing the load current, therefore, reduces PSRR at lower frequencies due to reduced gain, and increases it at higher frequencies due to more bandwidth. The TPS7A91 in *Figure 4* includes circuitry to maintain a consistent PSRR over frequency. Its PSRR decreases by about 10 dB as the load current IOUT increases from 100 mA to 1 A, but this differential remains essentially the same from 1 kHz to 10 MHz.



5. When measuring the intrinsic noise of an LDO (mounted on the evaluation module, or EVM), it's important to minimize the effects of noise from other sources, including the environment. Protective measures include input and output filters and a shielded enclosure. (Source: Texas Instruments)



6. The complete setup showing the grounded metal enclosure, input filter LDO, DUT EVM, separately housed blocking capacitor, and coaxial input and output cables. The foam sheet prevents accidental shorts to the case. (Source: Texas Instruments)

MEASURING LDO NOISE PERFORMANCE

When characterizing an LDO and measuring its noise performance, it's important to ensure that the results reflect only the noise we're interested in. We don't want noise from the downstream power supply feeding the LDO to couple into the device and adversely affect the intrinsic noise measurement, for example.

As a result, each type of measurement has a different test setup and procedure.

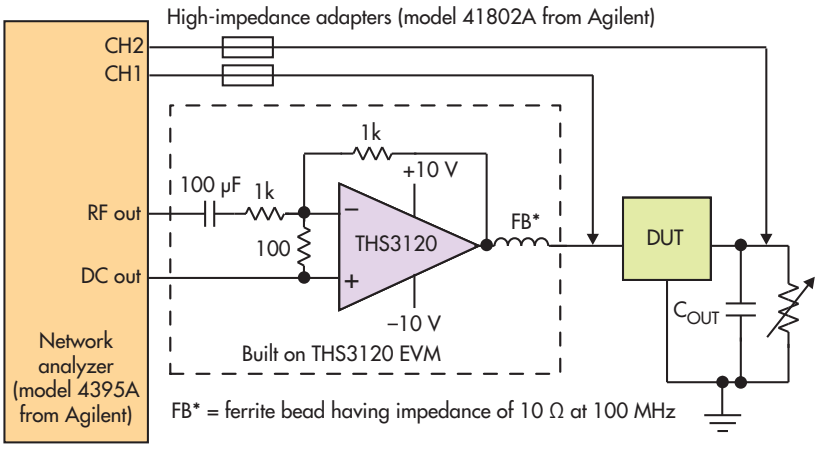
MEASURING INTRINSIC NOISE

Figure 5 shows a typical test setup used to measure intrinsic noise. The LDO to be tested (the device under test, or DUT) is mounted on an evaluation module (EVM) and powered by an external power supply.

For lowest noise, a purely resistive load is used for the DUT. A battery is preferred as the power source, but this

may not be practical for high-current DUTs. Bench power supplies are readily available, but tend to be noisy with spikes at the 50- or 60-Hz line frequency. A linear supply is preferable if available.

An LDO/filter block between the power supply and EVM helps to reduce the effects of power-supply noise. A passive pi-filter consisting of two capacitors and an inductor with a cutoff below the line frequency is one option, but will be expensive and bulky. Alternatively, an upstream LDO can cut down on power-supply noise while reducing cost and size. Make sure that it has low noise and high PSRR over a wide frequency range—for example, like those in the TPSA47xx ultra-low-noise LDO family.



7. A recommended method of measuring PSRR uses a high-bandwidth amplifier as a summing node to inject the signals and provide isolation. The PSRR is measured under a variety of load conditions. (Source: Texas Instruments)

A coupling capacitor after the DUT blocks its dc output and only passes the ac noise component to the downstream circuitry. Such a capacitor should have a 3-dB cutoff an order of magnitude lower than the lowest frequency being measured. This leads to a large-valued component when measuring frequencies down to 10 Hz, say, when used with a coaxial cable of 50-Ω characteristic impedance. The capacitor in *Figure 6* is a parallel array of numerous smaller capacitors totaling 5100 µF. It's housed in its own shielded box with coaxial connectors.

If the system noise floor is too high relative to the LDO's noise output, an optional amplifier after the capacitor can boost the signal to help the spectrum analyzer more easily measure the signal.

The correct settings on the spectrum analyzer are also important. For example, the width of the bandpass filter (the resolution bandwidth, or RBW), should be at least a decade smaller than the measured frequency. This increases the resolution, but also extends measurement time.

The magnitude of the noise fluctuates due to its random nature: The averaging function makes multiple measurements of each point and averages the results. Set the sample average to between 25 and 50.

Finally, the whole test setup, shown in Fig. 6, should be mounted in a grounded and shielded enclosure to minimize the effects of environmental noise. For an in-depth discussion of the test setup and procedure, consult this application note.

MEASURING PSRR

Figure 7 shows the recommended test setup to measure PSRR performance. The EB5061B Network analyzer generates both dc and an RF noise signal, then compares the input and output voltages to arrive at the results. The EB5061B has a frequency range from 5 Hz to 3 GHz.

A high-bandwidth amplifier acts as a summing node to amplify the analyzer output signal, provide isolation between the ac and dc components, and supply the DUT. The THS3120 is a low-noise, current-feedback amplifier that can provide an output current of up to 475 mA. The available EVM includes the required external components.

For best results, any LDO input capacitor should be removed before beginning the measurement, as a capacitive load could cause the high-speed amplifier to become unstable. To minimize added inductance, keep wire lengths as short as possible and use high-impedance probes placed directly on the VIN and VOUT pins to measure the input and output voltages.

While selecting the values of ac and dc inputs, be sure to keep within the specifications of the DUT. For example, the total input ($V_{DC} + V_{AC}$) to the DUT should be less than its absolute maximum input-voltage rating, and the value of ($V_{DC} - V_{AC}$) should always allow sufficient headroom (dropout voltage V_{DO}) across the LDO at the specified output voltage.

At very high frequencies, the amplifier's frequency response will roll off the ac component of the DUT input signal. Eventually, its effects will be too small to measure on the DUT output.

If a network analyzer isn't available, an alternative approach uses a signal generator, a dc source, and an oscillo-

scope. With this setup, the PSRR graph is assembled piece-by-piece by calculating the PSRR at each ripple frequency and combining the results. This approach is obviously slow and cumbersome. Furthermore, the resolution and sensitivity of the oscilloscope at millivolt input levels limits it to LDOs with PSRRs of less than about 50 dB.

For further information on this topic, consult this application note.

CONCLUSION

LDOs are widely used to provide low-noise power in many sensitive analog and RF applications, and it's important to be able to verify the LDO datasheet parameters in the lab. It's just as important, though, that the test setup itself doesn't skew the results. This article discusses some of the considerations needed to arrive at an accurate result.

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CHAPTER 3:

Regulator Review: Wring the Best Performance Out of Your LDO

Follow these practical steps to augment the efficiency of this fundamental building block in circuit design.

PAUL PICKERING, Contributing Editor

A low-dropout (LDO) regulator is a simple, inexpensive way to generate a regulated output voltage from a higher-voltage input. It's inherently low-noise because it has no switching transients, and it requires few if any external components, so it takes up little board space.

The LDO is easy to use right out of the box, but that doesn't mean its performance can't be improved. In this article, we'll review the principles of operation of the standard regulator and the LDO, and discuss a couple of ways to boost its noise performance.

TRANSFORMING A STANDARD REGULATOR INTO AN LDO

A linear regulator is inefficient because it dissipates power across the regulation device to regulate the output voltage. The regulation device is typically a power transistor—either a bipolar device or a FET.

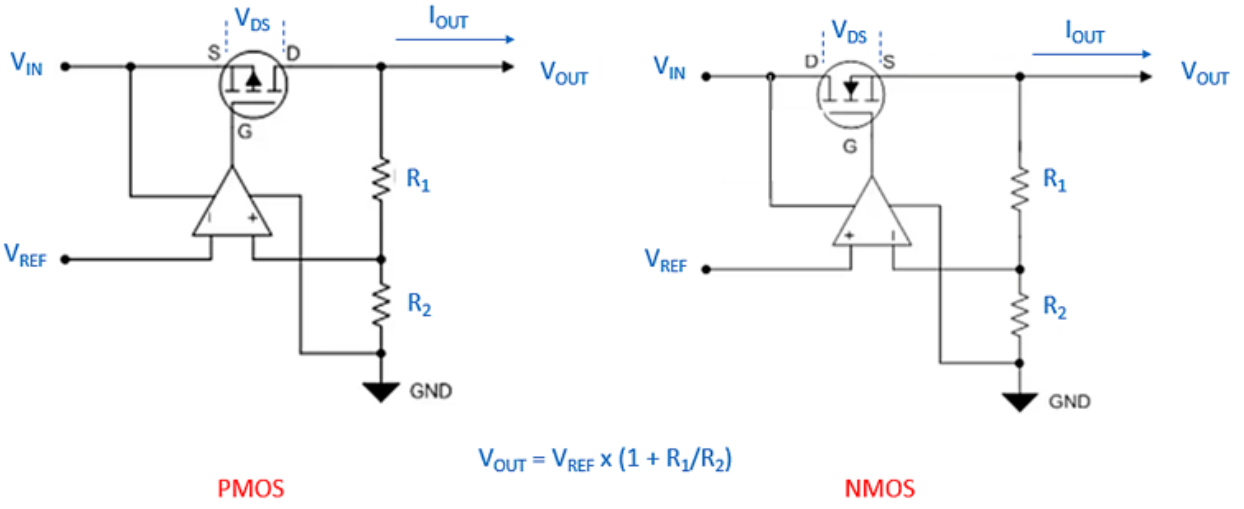
Figure 1 shows MOSFET linear-regulator circuits with both PMOS and NMOS power transistors. In both circuits, the voltage across the regulator's power transistor is

$V_{DS} = V_{IN} - V_{OUT} = I_{OUT} \times R_{DS}$

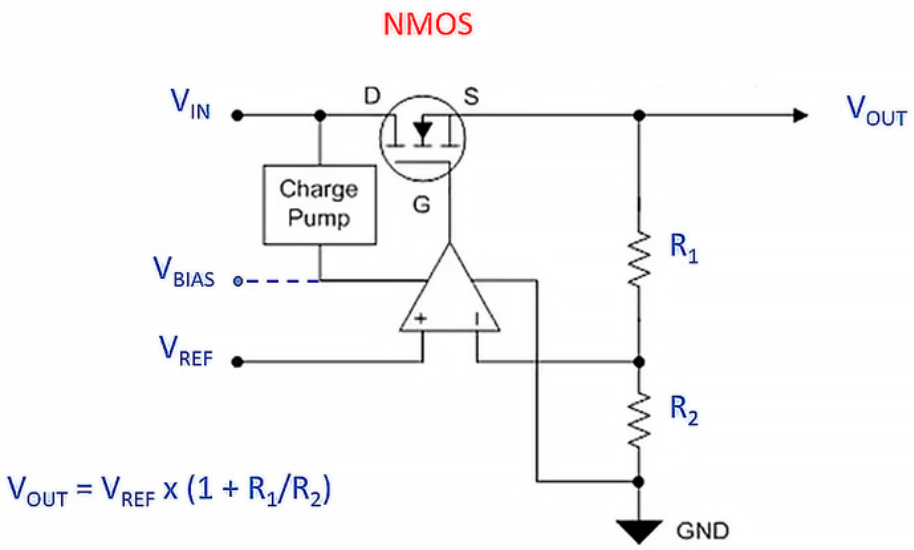
where R_{DS} is the FET's drain-to-source resistance. V_{DS} depends on the FET's gate-to-source voltage (V_{GS}).

The regulator control circuit uses R1 and R2 to divide down V_{OUT} and compares the scaled value to a reference voltage (V_{REF}). The resulting error signal drives the FET's gate voltage (V_G); this, in turn, controls V_{GS} to regulate V_{OUT} against changes in load current (I_{OUT}) or input voltage (V_{IN}). In these basic designs, V_G can range between the error amplifier's positive and negative supply rails: V_{IN} and ground.

The minimum allowed value of V_{DS} is called the dropout voltage (V_{DO}). For proper operation, $V_{IN} \geq V_{OUT} + V_{DO}$. If V_{IN} falls below this value, the regulator will drop out of regulation and will not be able to maintain the desired output. Instead, the output voltage will track the input



1. The basic PMOS and NMOS linear regulator architectures. (Source: TI Training: LDO Basics—Dropout Voltage video)



2. Here, the basic NMOS circuit is modified to enable LDO operation. Either a charge pump or an external bias voltage can be used. (Source: TI Training: LDO Basics—Dropout Voltage with Jose Gonzalez video)

voltage minus the dropout voltage.

As its name implies, an LDO is designed to minimize the value of V_{DO}. A state-of-the-art LDO can produce a regulated output with a dropout voltage as low as 100 mV. With the spread of low-voltage, power-efficient designs, LDOs are the dominant linear regulators today.

How do we turn a standard regulator design into an LDO? At the design stage, a larger-size power FET will yield a lower dropout voltage because it has a lower resistance. However, the architecture of the circuit is the main determining factor, especially the minimum and maximum values of V_{GS}.

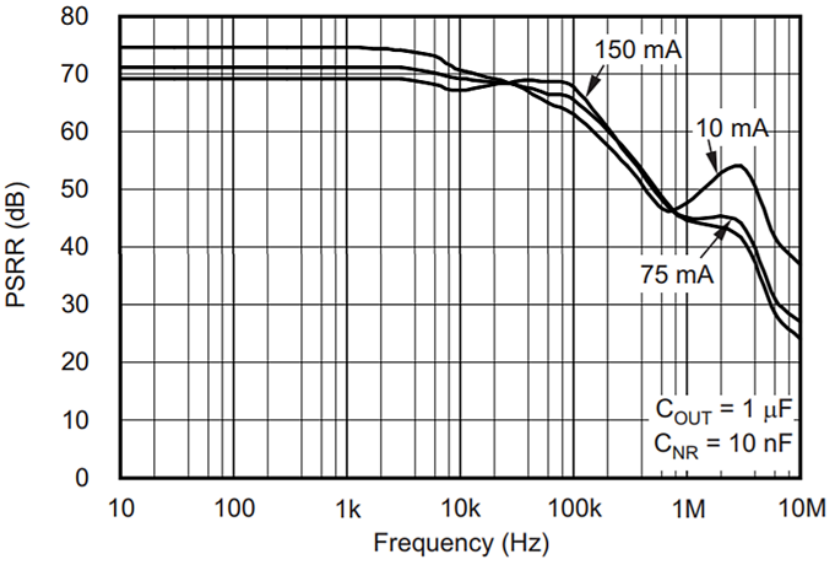
The P-channel MOSFET (PMOS) design requires a negative V_{GS} to operate. If either V_{IN} or I_{OUT} increases, the control circuit responds by driving V_{GS} more negative. In the PMOS case, $V_S = V_{IN}$. The maximum negative V_{GS} occurs when driving V_G to the negative rail; this corresponds to $V_{GS} = -V_{IN}$. Reducing the dropout voltage ($V_{IN} - V_{OUT}$) doesn't affect the magnitude of V_{GS}, making an LDO design possible.

For the N-channel MOSFET (NFET), the situation is reversed. If V_{IN} decreases, the control circuit must drive V_G more positive to increase V_{GS}. The error amplifier can still drive V_G between V_{IN} and ground, but now $V_S = V_{OUT}$, so the maximum value of V_{GS} is ($V_{IN} - V_{OUT}$)—in other words, the voltage across the FET.

A FET doesn't even begin to turn on until V_{GS} is greater than a threshold voltage of about 2 V. The NMOS circuit as shown limits the minimum dropout voltage to 2 V, not exactly LDO territory.

Adding an internal charge pump between V_{IN} and the error amp's positive supply solves the problem *(Fig. 2)*. The charge pump boosts the error amplifier's positive rail, allowing it to drive a higher V_{GS}, and making an LDO design possible. An alternative implementation supplies the higher positive rail via an external BIAS pin. Ultra-low-dropout LDOs such as TI's new TPS7A10 use this approach.

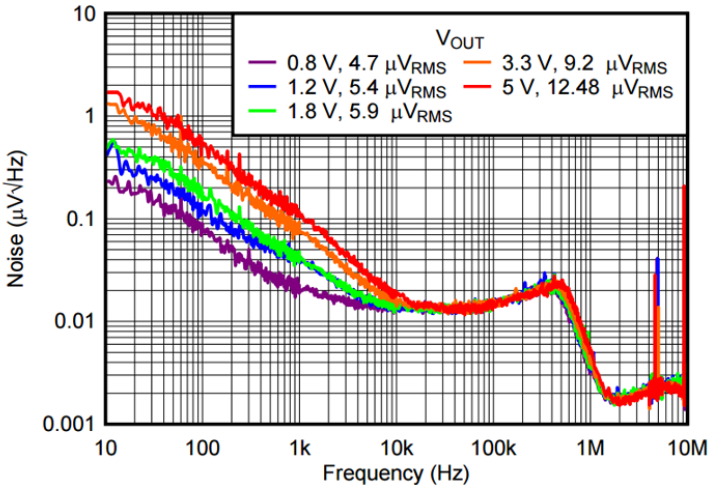
As we've discussed, low noise is an advantage of a linear regulator or LDO, and many applications use an LDO to clean up the noisy output of a switching power converter. Two parameters in the datasheet characterize the LDO's noise performance, so we'll discuss these now.



3. The TPS717 features a high-bandwidth, high-gain error loop gain for high PSRR. (Source: TI "TPS717" PDF)

INPUT NOISE AND PSRR

The power-supply rejection ratio (PSRR), also called the power-supply ripple rejection, describes how well the LDO rejects noise from an external source, such as a switching power supply, that appears on its input. The PSRR compares the output ripple and the input ripple of the LDO over the frequency range of interest for the application.



4. The spectral noise density of an LDO increases with VOUT at lower frequencies. (Source: TI Blog: "LDO basics: noise—part 1")

Figure 3 shows the graph of PSRR vs. current for the TPS717, a low-noise, high-bandwidth PSRR LDO with 150-mA maximum output.

PSRR is expressed in decibels (dB)—the higher the number, the better the rejection. The equation is:

$$PSRR\ (dB) = 20\ Log_{10}\left(\frac{V_{IN}(f)}{V_{OUT}(f)}\right)$$

A couple of factors can affect the PSRR. An increased load current affects both ends of the frequency range. The output impedance of the FET is inversely proportional to the drain current, so an increase in I_{OUT} lowers the PSRR at lower frequencies because it lowers the error-loop gain. At the same time, increasing the load current moves the output pole to higher frequencies. This increases the feedback loop bandwidth, which increases the PSRR at higher frequencies.

The PSRR also lowers when V_{DS} drops below about 1 V because the FET begins to transition from the active (saturation) region of operation into the triode/ohmic region, which also causes the feedback loop to lose gain.

When comparing PSRR performance between LDOs, it's important always to match V_{IN}-V_{OUT} and load currents. It's also important to compare LDOs with identical V_{OUT}, since PSRR is usually better at lower output voltages.

OUTPUT NOISE AND SPECTRAL NOISE DENSITY

Of course, the LDO itself isn't noiseless. It generates internal (intrinsic) noise that appears on the output and adds to the residual input noise discussed above. Several physical mechanisms contribute to intrinsic noise in LDOs and other components.

Thermal noise occurs in both active and passive devices due to the random motion of charge carriers (either electrons or holes) in a conductor. Thermal noise is proportional to absolute temperature and is independent of current flow. It has the flat spectrum characteristic of white noise.

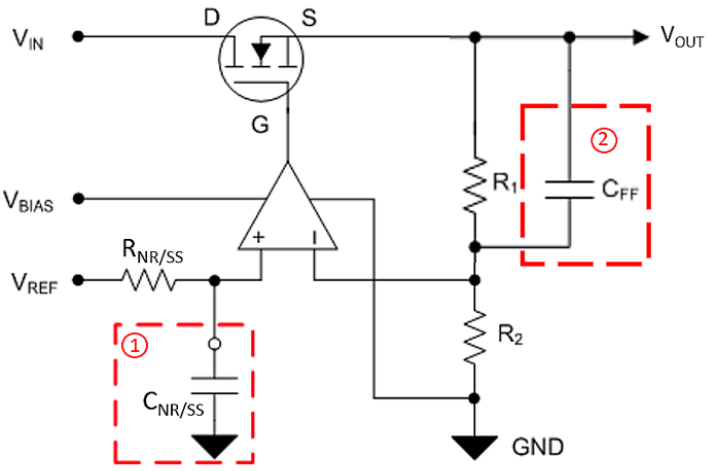
Flicker noise occurs only in active devices and varies by technology. Flicker noise is proportional to current flow and inversely dependent on frequency, hence its other name of 1/f noise.

Finally, ***shot noise*** is caused by electrons or holes randomly crossing a potential barrier such as a PN junction. It's also associated with current flow and has a flat frequency spectrum.

Intrinsic noise is expressed in μV√Hz; it's characterized by an output spectral noise density graph in the LDO datasheet showing how the noise varies over frequency. Datasheets typically include several graphs that describe how the output noise varies with output current (I_{OUT}), output voltage (V_{OUT}), and other parameters.

Figure 4 shows the spectral noise density versus V_{OUT} for the TPS7A91, a 1-A high-accuracy low-noise LDO with 200-mV maximum dropout voltage.

The output noise is concentrated at the lower end of the frequency spectrum. Datasheets commonly provide a single noise value for comparison purposes. This value represents the output noise integrated from 10 Hz to 100 kHz and is expressed in microvolts root-mean-square (μV_{RMS}). Using this metric, the TPS7A91's output noise figure is 4.7 μV_{RMS}.



5. Adding a noise-reduction capacitor (1) and a feed-forward capacitor (2) can improve LDO noise performance. (Source: TI Blog: "LDO basics: noise—part 2," Fig. 1)

Be careful when comparing components from different manufacturers. Some datasheets integrate the noise over another frequency range, such as 100 Hz – 100 kHz, or even use a custom range. Integrating over a select frequency range can help mask unflattering noise properties, so it's important to examine the individual noise curves in addition to the integrated value.

TO IMPROVE LDO NOISE PERFORMANCE, START WITH THE VOLTAGE REFERENCE

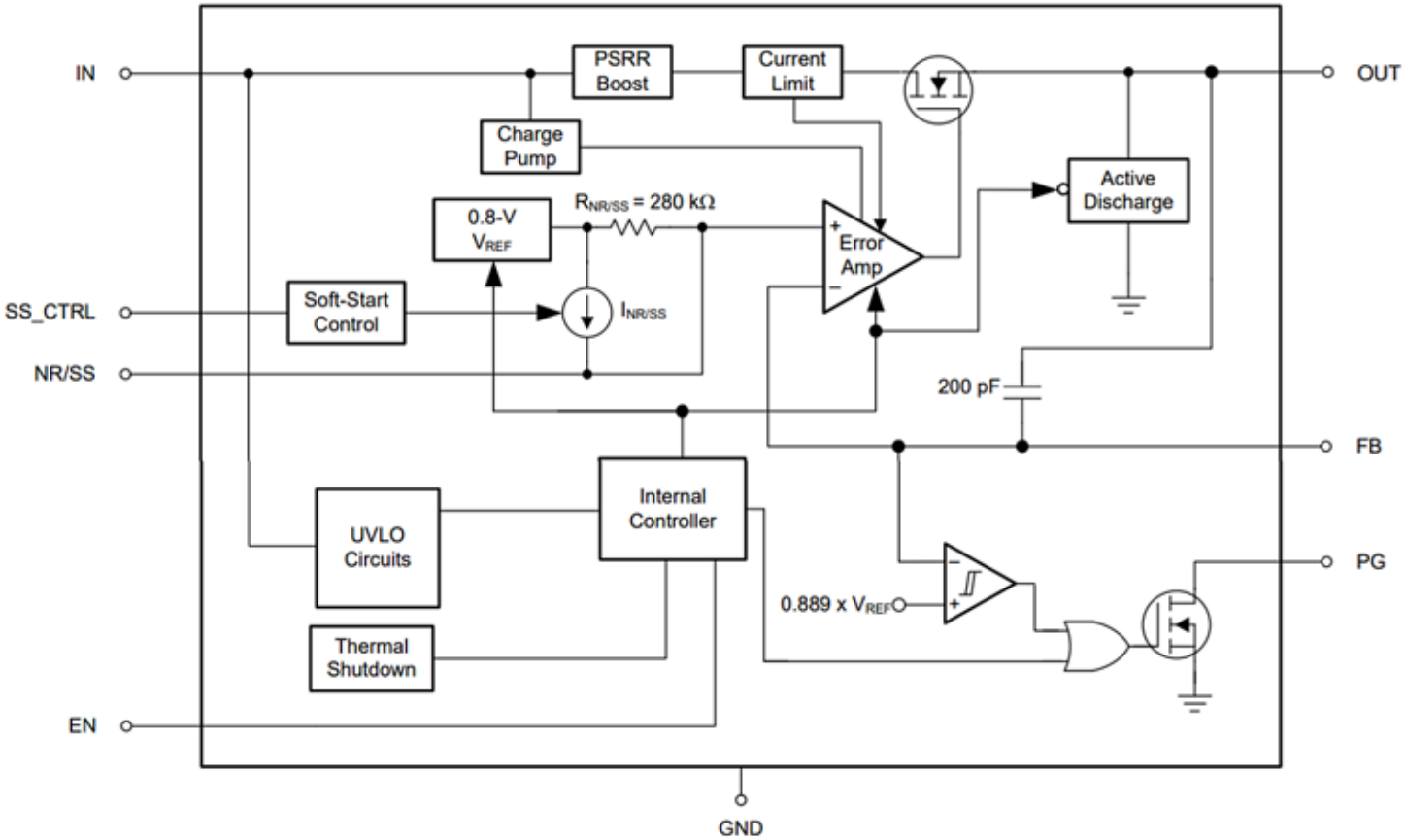
How do we improve the noise performance of the standard LDO? Although every component in the LDO contributes to the overall noise, the voltage-reference circuit is the main culprit. There are two reasons: the circuit has many noise-generating active and passive components; and any noise on V_{REF} is amplified by the error amplifier. Any input ripple that appears on the reference is also amplified and appears on the output; therefore, the bandgap reference must have high PSRR as well as low noise.

The solution for both internal noise and PSRR is simply to add a low-pass filter (LPF) in series with the bandgap reference output. As shown in *Figure 5*, this LPF is accomplished by adding an external capacitor $C_{NR/SS}$ to the existing internal resistor $R_{NR/SS}$, and many low-noise LDOs include a pin for this purpose.

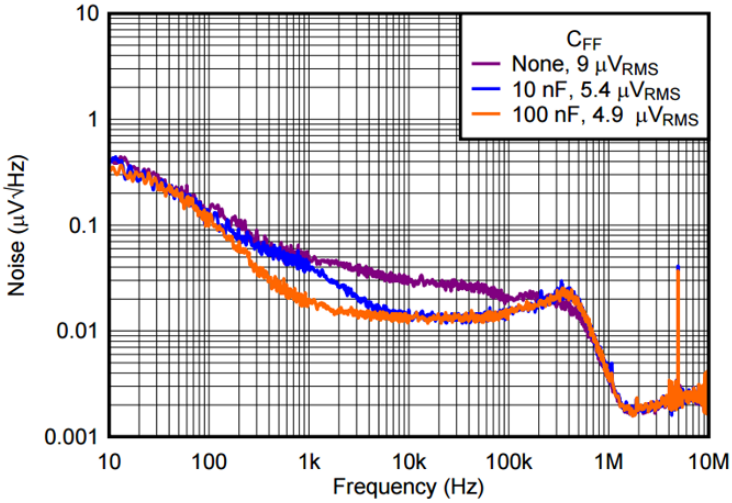
The capacitor serves a dual purpose: when the LDO is initially powered up, the V_{REF} voltage seen by the error-amplifier ramps up as $C_{NR/SS}$ charges through the internal resistor. In effect, the LPF adds a soft-start, hence the "NR/SS" subscript on the resistor and capacitor. This soft-start is helpful in preventing a current-limit condition if the LDO must charge a large-value output capacitance at startup.

The LPF isn't a panacea. Adding it reduces the PSRR at low frequencies because it passes bandgap ripple in this range. A low-ESR ceramic output capacitor improves PSRR performance. The capacitance value should be chosen based on the frequencies that are important for the application. Careful board layout design will reduce the ripple feedthrough from input to output caused by board parasitics.

Another strategy to prevent the output noise from being amplified by the error amplifier is to add a feed-forward capacitor. C_{FF} provides an ac bypass around resistor R1, leaving the dc gain unchanged but reducing the gain at



6. The TPS7A91 is an adjustable-output LDO optimized for low-noise operation. (Source: TI "TPS7A91" PDF)



7. Adding a feed-forward capacitor CFF improves the TPS7A91's output noise performance at lower frequencies. (Source: TI Blog: "LDO basics: noise—part 2," Fig. 2)

higher frequencies.

Adding a feed-forward capacitor has multiple effects on LDO performance, including improved noise, stability, load response, and PSRR. It also improves the phase margin of the feedback loop, enhancing the LDO's load transient response with less ringing and faster settling time.

A feed-forward capacitor can't be added to a standard three-terminal fixed-output LDO because the R1/R2 node is internal. Still, many LDOs designed for low-noise operation make this node available on a pin. Of course, adjustable-output LDOs such as the TPS7A91 in *Figures 6 and 7* include a pin (FB) for external resistors and C_{FF}. This device also features a $C_{NR/SS}$ pin.

The table provides a summary of the effects versus frequency of the two noise-reduction techniques discussed above: C_{NR} and C_{FF}.

CONCLUSION

The LDO is the dominant architecture for linear regulation.

COMPARING NOISE-REDUCTION TECHNIQUES

Parameter	Noise		
	Low frequency (1 kHz)	Mid frequency (1 kHz – 100 kHz)	High frequency (>100 kHz)
Noise-reduction capacitor (CNR)	✓✓✓	✓	No effect
Feedforward capacitor (CFF)	✓	✓✓✓	✓

This article discussed the two main FET LDO architectures, the sources of noise, and reviewed techniques to help improve noise performance. For a deeper discussion of LDO noise, go here. PSRR is discussed in more detail here, and you can find out more about using an LDO feedforward capacitor in this application report.

Texas Instruments offers over 500 LDOs for different applications, giving the designer a broad range of features: low noise, wide V_{IN}, small size, low I_q, and processor attach.

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CHAPTER 4:

The Heat Is On: Protecting the LDO in Industrial Environments

Low-dropout regulators are important components that power many industrial data-acquisition systems, and controlling their internal temperature to avoid damage is a key design goal.

PAUL PICKERING, Contributing Editor

The Industrial Internet of Things (IoT), with its emphasis on real-time monitoring and control, has led to an explosion in the number of sensors attached to industrial machines and processes *(Fig. 1)*. Many of the quantities being measured are analog in nature, including pressure, temperature, and flow.

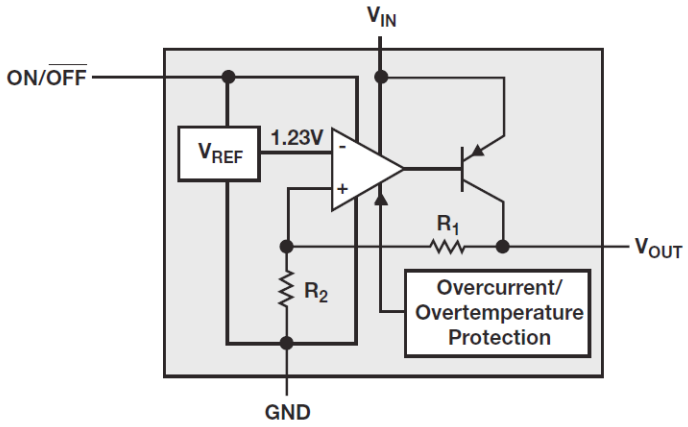
A typical data-acquisition system consists of a precision analog front end connected to the sensor, followed by an analog-to-digital converter that sends information over a wired or wireless connection to a gateway and then to the cloud.

SWITCHING VS. LINEAR REGULATORS—A (VERY) SHORT OVERVIEW

The power supply to an industrial data-acquisition system typically consists of a mix of switching and linear regulators. Each type of design has its strengths and weaknesses. At its heart, a switching design relies on a power transistor that changes the analog input voltage into a pulse-width-modulated (PWM) pulse train whose duty cycle depends on the output voltage and current. The topology chosen depends on the application. A switching regulator can convert an input voltage to a higher level (boost), a lower level (buck), or even convert a positive voltage to a negative voltage.

Switching regulators are highly efficient—up to 95% or higher—so a compact design can handle large amounts of power. The high efficiency makes a switching regulator the preferred choice for larger power-conversion tasks, such as providing an industrial rack with system dc power. To address that space, Texas Instruments has developed a

1. The automated factory depends on accurate data from multiple analog sensors. (Source: TI blog: "How to ensure precision in automated processes")



2. A linear regulator maintains a constant voltage VOUT as the load current varies. The PNP pass transistor dissipates excess power as heat. (Source: TI: "Linear power for automated industrial systems" PDF)

wide array of switching regulators.

On the other hand, the transistor's switching action generates noise that appears as a ripple on the output. In addition, there's some amount of delay before the switching controller can detect and respond to sudden load changes.

In a data-acquisition system, the high level of noise is a problem when providing clean power to the sensitive analog circuitry that buffers or amplifies a low-level sensor input. That's the domain of the linear regulator.

A linear regulator *(Fig. 2)* has very low output ripple and noise because it doesn't use any switching element. Instead, its power transistor operates continuously. Any difference between the desired output voltage and the actual one is expressed as an error signal. The power-transistor control circuit uses the error signal to adjust the power transistor and move the output voltage closer to the desired value. The feedback loop is analog in nature, so the linear regulator responds instantaneously to load variations.

A linear design can only convert a higher input voltage V_{IN} to a lower output voltage V_{OUT}. A voltage representing the difference between the input and output ($V_{IN} - V_{OUT}$) appears across the power transistor; for a current I_{OUT}, the power transistor therefore dissipates the wasted power as heat:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + (V_{IN} \times I_{ground})$$

(V_{IN} x I_{ground}) represents the power consumed by the control circuitry of the device. As ($V_{IN} - V_{OUT}$) increases, the linear regulator dissipates more power and the power supply becomes progressively less efficient. Therefore, the difference between V_{IN} and V_{OUT} should be kept as low as possible.

A linear regulator's input voltage must be higher than the desired output voltage by a certain value—the dropout voltage V_{DO}—to maintain regulation. If the input falls below the minimum value, the output voltage begins to decline. The value of V_{DO} varies with input voltage, output current, and junction temperature, but a low-dropout (LDO) regulator can have a dropout voltage as low as a few tenths of a volt. Key LDO parameters include dropout voltage, output voltage, output current, input voltage range, package type, package size, control features like enable or soft-start, power-dissipation capability, and noise performance.

Texas Instruments offers over 500 LDO regulators for industrial, consumer, communications, and automotive applications.

LDO THERMAL PERFORMANCE AND PACKAGING

Since the LDO dissipates excess power as heat, its thermal performance is of great interest to the designer. There are two main areas of concern: Making sure that the part doesn't get too hot; and protecting it if the temperature exceeds a safe threshold. Let's take a closer look at these two topics.

Why do we care about the temperature of an LDO? Although low temperatures can cause problems, in power devices we're primarily concerned about high temperatures.

In fact, at a high-enough temperature (around 290°C for doped silicon), semiconductor action ceases—the electrical differences between the n- and p-regions disappear, and the p-n junction no longer controls the carrier flow. Long before

DISSIPATION RATING TABLE

PACKAGE	$R_{\Theta JC}$ (°C/W)	$R_{\Theta JA}$ (°C/W)(1)
TO-220	2	58.7(2)
TO-263	2	38.7(3)

(1) For both packages, the $R_{\Theta JA}$ values were computed using JEDEC high K board (2S2P) with 1 ounce internal copper plane and ground plane. There was no air flow across the packages.
(2) $R_{\Theta JA}$ was computed assuming a vertical, free standing TO-220 package with pins soldered to the board. There is no heatsink attached to the package.
(3) $R_{\Theta JA}$ was computed assuming a horizontally mounted TO-263 package with pins soldered to the board. There is no copper pad underneath the package.

3. Many LDOs, such as the TPS759 shown here, offer a choice of packages with different $R_{\theta JA}$ values. Note that the test conditions are clearly stated. (Source: TI: "Power Good Fast-Transient Response 7.5-A Low-Dropout Voltage Regulators" PDF)

that point, though, thermal overstress caused by excess heat melts the package, warping and cracking the integrated circuit.

There are more subtle effects, too. Many operating parameters are temperature-dependent. At high temperatures, the device may still operate, but compliance with the datasheet specifications is no longer guaranteed.

An LDO datasheet lists several high-temperature limits, as well as the likely consequences if they're exceeded. Consult the datasheet for specifics, but the table below summarizes the results.

During operation, the LDO temperature at the junction T_J rises above ambient temperature T_A due to the power P_D dissipated across the pass transistor. The value of T_J is given by:

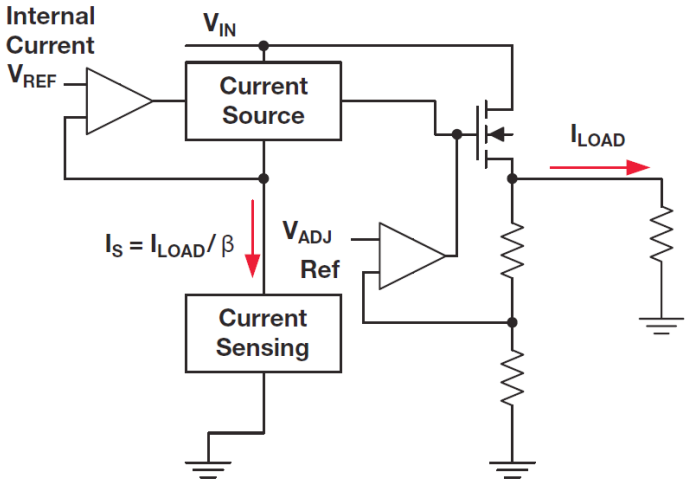
$$T_J = T_A + (P_D \times R_{\theta JA})$$

where $R_{\theta JA}$ is the thermal resistance of the device from the junction to the ambient environment, expressed as degrees Celsius per watt. This parameter is stated in the datasheet as shown in *Figure 3*. It specifies the temperature rise for each watt of power consumed and is a measure of the thermal performance of the device package. You should be careful not to rely solely on $R_{\theta JA}$ to estimate the temperature of the device in the application, because the real-world value also depends on the PCB design, layout, and other factors.

You can compare the thermal performance of two devices from different manufacturers if each one uses a standardized test, such as JEDEC's EIA/JESD51-x standard, to measure $R_{\theta JA}$. For more information on the thermal performance of IC packages, consult this application report.

LDO TEMPERATURE LIMITS

Term	Definition	Consequences if exceeded
Absolute maximum junction temperature	The temperature beyond which device damage occurs.	The device may not function or meet expected performance at this temperature.
Absolute maximum operating temperature	The maximum junction temperature at which the device functions electrically.	The lifetime of the device is reduced if the device operates continually at this temperature.
Recommended operating temperature	The junction temperature at which the device operates continuously at the designated performance over the designed lifetime.	The reliability of the device may be degraded if the device operates above this temperature.



4. The LDO "brick-wall" current limit shuts off the LDO output when the load current exceeds the limit value. (Source: TI blog: "LDO basics: Current limit," Fig. 1)

FOLLOW THESE STEPS TO MINIMIZE LDO TEMPERATURE RISE

If an LDO is supplying power, its temperature is going to rise. But you can take steps to help remove the heat from the device and battle the laws of physics.

Many LDOs come in a variety of packages. Unless your design is severely space-limited, you can choose a larger, more thermally efficient package. Choosing the right package can make a big difference. The TPS732 250-mA LDO, for example, is available in three package types: an 8-pin SON (3.00 × 3.00 mm), a 6-pin SOT-223 (6.50 × 3.50 mm), and a 5-pin SOT-23 (2.90 × 1.60 mm).

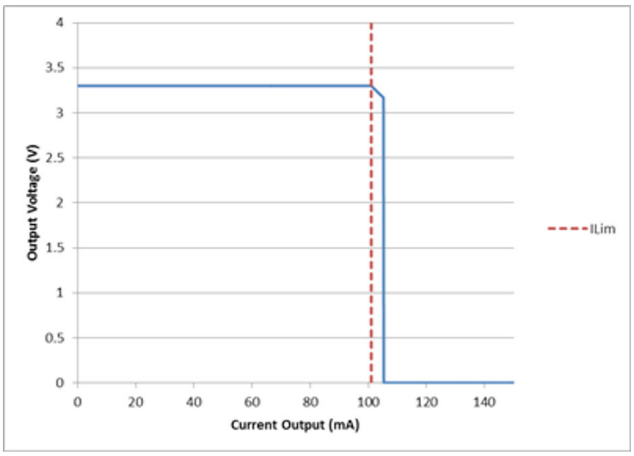
The values of $R_{\theta JA}$ for these packages are 58.3, 53.1, and 205.9°C/W respectively. Why the huge variation? The SON and SOT-223 are relatively large power packages with exposed copper pads; these are soldered to the PCB ground plane and provide a thermally efficient conduit to remove heat. The SOT-23 package lacks a thermal pad; it's also the smallest in size, so it has the smallest surface area to remove heat through radiation and convection.

We can perform a quick calculation to illustrate the difference between packages in the TPS732. Let's assume V_{IN} = 5.5 V, V_{OUT} = 3 V, and I_{OUT} = 250 mA. The ground current I_{ground} varies with temperature, V_{IN}, and I_{OUT}; at the maximum recommended operating temperature, 125°C, it's about 0.72 mA.

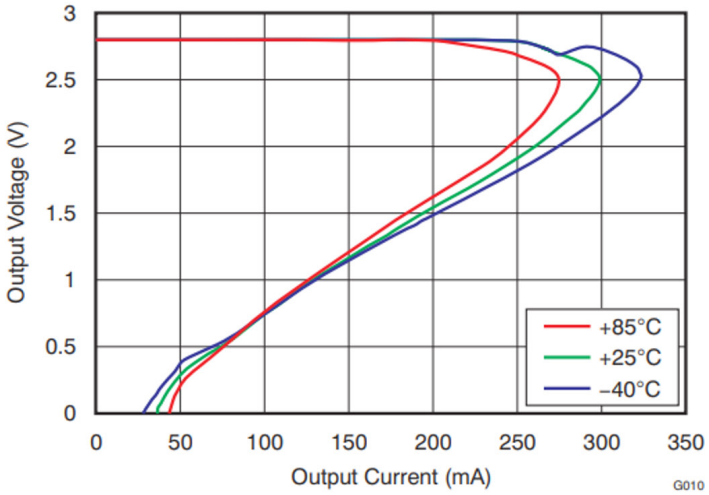
Using the equation above gives:

$$P_D = (5.5 - 3.0) \times 0.25 + (5.5 \times 0.00072) = 0.63 \text{ W}$$

(a)



(b)



5. Two varieties of current limit: brick-wall (a) and foldback (b). (Source: TI blog: "LDO basics: Current limit," Figs. 2,3)

For an ambient temperature, T_A, of 25°C, let's compare T_J for the three packages:

$T_{J(SON)} = 25°C + (58.3°C/W \times 0.63\ W) = 61.73°C$

$T_{J(SOT223)} = 25°C + (53.1°C/W \times 0.63\ W) = 58.45°C$

$T_{J(SOT23)} = 25°C + (205.9°C/W \times 0.63\ W) = 154.72°C$

The junction temperatures for the first two packages are well within the recommended operating temperature range, but $T_{J(SOT23)}$ exceeds the maximum temperature by a large margin. In fact, it's dangerously close to the temperature (160°C) that activates the TPS732's thermal-protection circuit.

A thermal-protection circuit is a standard feature on LDOs: When activated, it disables the output, protecting the LDO from overheating damage, and letting it cool. For the TPS732, when T_J cools to around 140°C, the thermal-protection circuit turns off, and the TPS732 resumes supplying current to the load.

If conditions don't change, the part will heat up again and eventually reactivate the thermal protection. The LDO will continue to oscillate at some frequency that's a function of the thermal-protection hysteresis, the power dissipation, and other variables. A calculation such as the one above is a standard part of the LDO design and would normally force a switch to a more thermally efficient package.

What other steps can the designer take to reduce the temperature rise and avoid thermal shutdown? Decreasing the thermal resistance between the LDO and the PCB is another sound strategy. If the LDO has a thermal pad, it should be soldered to the ground plane or attached to a heatsink. Much of the heat leaves the LDO via the pins, so increasing the size of the input, output, and ground planes will also decrease the thermal resistance. Most datasheets for Texas Instruments' LDOs contain a detailed thermal analysis and layout recommendations.

Finally, you can reduce the value of P_D by adding a power resistor R_P in series with the LDO input. The resistor reduces the input voltage at the LDO input pin, and therefore the power that must be dissipated across the power transistor. For an input current I_{IN}, the voltage seen at the LDO input pin is reduced by $(V_{IN} - I_{IN} \times R_P)$.

Two cautions:

- The resistor must be able to dissipate the power P_{RP} generated by the worst-case current ($P_{RP} = I_{IN(max)}^2 \times R_P$)
- The voltage drop across R_P when $I_{IN(max)}$ flows through it must leave the LDO input above the minimum needed for regulation: i.e., $V_{IN} > V_{OUT} + V_{DO}$.

WHEN IT ALL GOES WRONG: OVERLOAD PROTECTION CIRCUITS

The design techniques discussed above are necessary, but not sufficient. As we've seen in the previous section, the temperature of an LDO depends on P_D, which in turn depends heavily on the current I_{OUT} supplied to the load. If the load demands more current than the LDO is designed to supply, or during an abnormal condition such as a shorted load, the LDO also contains internal circuitry to limit the current to a predefined value and prevent catastrophe.

Figure 4 shows the standard LDO current-limiting circuit. It works by measuring the output current, scaling it down, and comparing the scaled current to an internal reference

current I_{REF} that represents the maximum allowed value. If the scaled output current exceeds I_{REF}, it triggers the comparator, which shuts off the output, and the voltage drops to zero. This type of circuit is commonly referred to as a "brick-wall" current limit.

Another strategy is to limit the maximum current the LDO can supply to a fixed value I_{LIMIT} independent of output voltage. V_{OUT} isn't regulated when the device is in current limit: $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. If the load is shorted, the power transistor must be large enough to dissipate ($V_{IN} \times I_{LIMIT}$) indefinitely—or at least until the thermal protection circuit is activated.

Foldback current limiting is a third strategy in which the goal is to limit the total power dissipation rather than the output current. This approach keeps the output transistor within its safe power-dissipation limit by reducing the output current limit linearly while V_{OUT} decreases and V_{IN} remains steady. The advantage of this approach is that the foldback current is less than I_{LIMIT} above, so the power transistor must dissipate much less power, reducing the risk of damage. *Figure 5* compares the brick-wall and foldback waveforms.

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Basics of power supply in LDO's

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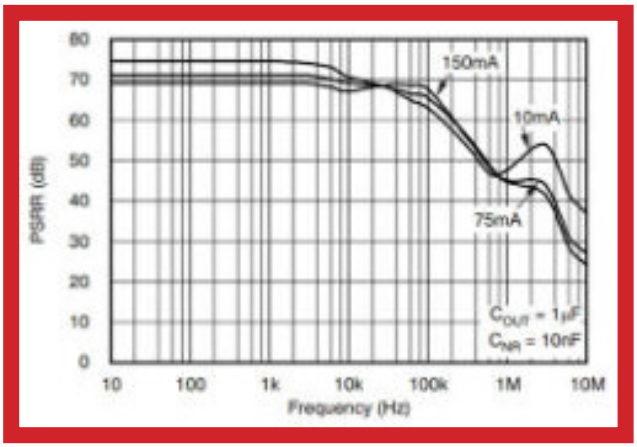


CHAPTER 5:

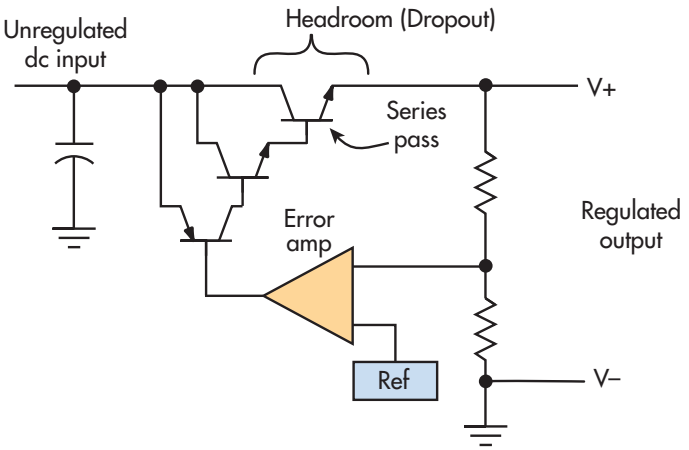
LDOs Bring High Efficiency and Low Noise Regulation to Industrial Automation

Switched mode or linear? Often times, the best solution for industrial equipment is a linear power supply that incorporates a low-dropout regulator with overcurrent and thermal protection.

LOU FRENZEL, Contributing Editor

Designing a power-supply system for industrial automation equipment requires a thorough understanding of the surroundings and conditions that affect the functionality of the wide range of equipment involved. The most important design decision is whether to use linear power supplies or switch-mode power supplies (SMPS).

Today, SMPS are the most popular because of their high efficiency. However, they do have downsides that make linear supplies more desirable. Linear supplies also have their disadvantages, but often turn out to be the best choice for industrial use. Even better is a "have your cake and eat it too" solution: Use a linear supply with low-dropout (LDO) regulators.



1. Often, a traditional linear IC regulator architecture will use a Darlington bipolar series pass transistor.

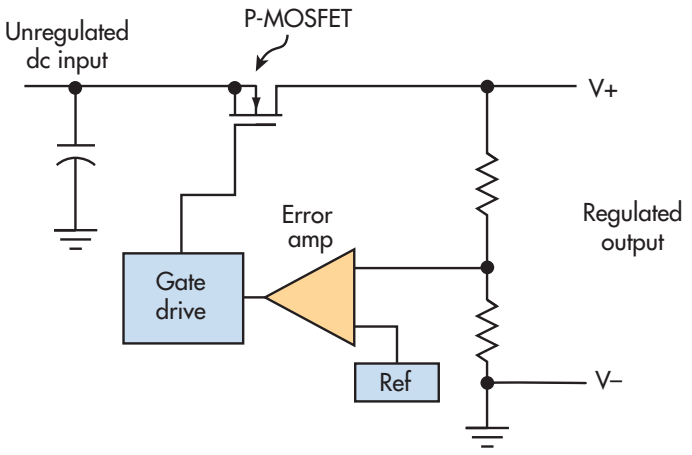
LINEAR VS. SMPS

As mentioned, the primary reason for using switch-mode supplies is their high efficiency. Typical figures vary with the application, but efficiencies of greater than 90% are typical. High efficiency translates into minimum power loss in the supply with its attendant low heat dissipation. In large complex industrial settings with lots of equipment efficiency, power usage and heat dissipation become critical factors in terms of operating costs.

The main disadvantage of the SMPS is its noise generation. High-frequency pulse-width-modulated (PWM) pulses are filtered to form the desired dc level, but the resulting ripple and radiated or conducted noise generated can negatively impact the powered equipment and nearby devices.

Linear supplies with linear regulators don't have the noise problem. Furthermore, ripple is greatly reduced by large capacitive filters and the feedback action of the regulator circuitry.

The big issue with these supplies, though, is that the efficiency is very poor *(Fig. 1)*. A series pass transistor between the dc input voltage and the regulated dc output requires a minimum amount of voltage drop in order to maintain regulation. This voltage, called the dropout or



2. Here's a typical IC LDO circuit with a P-type MOSFET pass transistor.

headroom voltage, is usually a minimum of 1.5 to 2.5 V or more.

Since the output current passes through the pass transistor, this device will dissipate a significant amount of power, all of which shows up as heat. As the input or output voltages vary, the feedback senses the change and drives the pass transistor to adjust its conductance to compensate from any variation. This linear operation requires the minimum overhead be observed to maintain regulation. The overall benefit is no noise generation traded off for efficiency.

One way to get the benefits of low noise and good efficiency concurrently is to use a LDO regulator.

LDO OPERATION AND BENEFITS

One definition of LDO is a regulator that operates with a series-pass-transistor voltage drop of less than 1 V. A dropout voltage of 1 V or more defines a conventional linear regulator.

A dropout of less than 1 V can be achieved with a PNP bipolar series pass transistor, but modern designs generally use a P-type MOSFET with very low dropout voltages of less than 100 mV (in addition to low on-resistance) *(Fig. 2)*. When working with low supply voltages of 3.3 V or less, low dropout levels become a significant percentage of the output, so less is more.

The regulation process is similar to other series regulators in that any output voltage change is sensed and the gate drive to the MOSFET is varied to correct for the variation.

Key benefits of an LDO include:

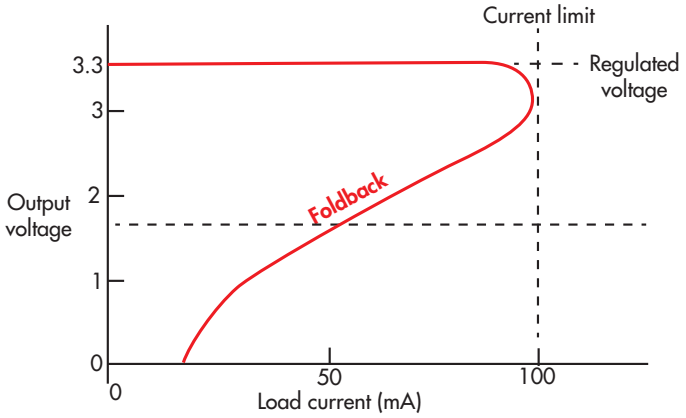
- *Low noise and ripple:* There are no switching transients. Ripple is greatly reduced by the feedback regulatory action, thus providing an excellent power-supply rejection ratio (PSRR).
- *Low quiescent current:* Minimal operational current makes LDOs a good choice for battery-operated devices.
- *Small packages:* Most housings are tiny and no external inductors are required.
- *Wide input-voltage range:* This accommodates large input transient voltages without protection or damage.
- *Good transient response:* Adapts rapidly to fast load changes.

The LDO is often used to power processors and field-programmable gate arrays (FPGAs) that require the fast transient response. And they're ideal for critical linear circuits like signal-conditioning amplifiers, oscillators, and PLL synthesizers. In industrial-automation applications, LDOs make good regulators for sensors, data converters, and wireless/communications/networking circuits.

THE CURRENT-LIMITING ISSUE

Some applications put excessive stress on power supplies, especially in industrial automation. High temperature and high voltages are very common. Another potential problem is excessive current draw or a short circuit. Sudden high current flow will typically damage the regulator unless it's compensated for. That problem can be handled by incorporating LDOs with internal overcurrent protection.

Two basic types of current limiting are used in LDOs: brick wall and foldback. In the brick-wall method, a current limit is set and if that limit is exceeded, the LDO abruptly shuts down. The regulator continues to supply current at the cutoff level, but the output voltage is no longer regulated.



3. Looking at a comparison of output voltage vs. load current, it shows that foldback reduces the output voltage as output current exceeds the limit of the device.

The output voltage becomes the product of the current-limit value and the load resistance. The series pass transistor will continue to dissipate power until the internal protection process of thermal shutdown turns off the device.

The foldback method of current limiting attempts to keep total power dissipation at a constant level. If overcurrent conditions occur, the circuitry reduces the output current and there's a decrease in output voltage *(Fig. 3)*. This keeps the power dissipation within the capability of the device. After that, thermal protection kicks in if elevated temperature conditions persist.

Different LDOs use different methods of current limiting, so you should choose one that fits your application. For example, Texas Instruments offers the TPS7A16 LDO with brick-wall current limiting and the TLV71P LDO with foldback current limiting. More details on current limiting can be found at this reference.

THERMAL ISSUES

While LDOs are more efficient than standard linear regulators, they still dissipate power. Most LDOs also include thermal-shutdown circuitry, which turns off the device if the temperature exceeds the limit—usually in the 150-170° range. In some applications, a heat sink may be needed.

In addition, careful attention should be given to the thermal conditions in the power supply. Besides the thermal specifications of the IC itself, you should consider other factors such as PCB design and component placement in regards to the interaction with other devices. The greater the copper area devoted to the LDO, the better the heat dissipation. Other factors to consider are ambient temperature and airflow ventilation.

You can learn more about thermal considerations from videos that shows you how to measure thermal properties and how to avoid damaging an LDO through thermal excess. This and other LDO videos are available from Texas Instruments.

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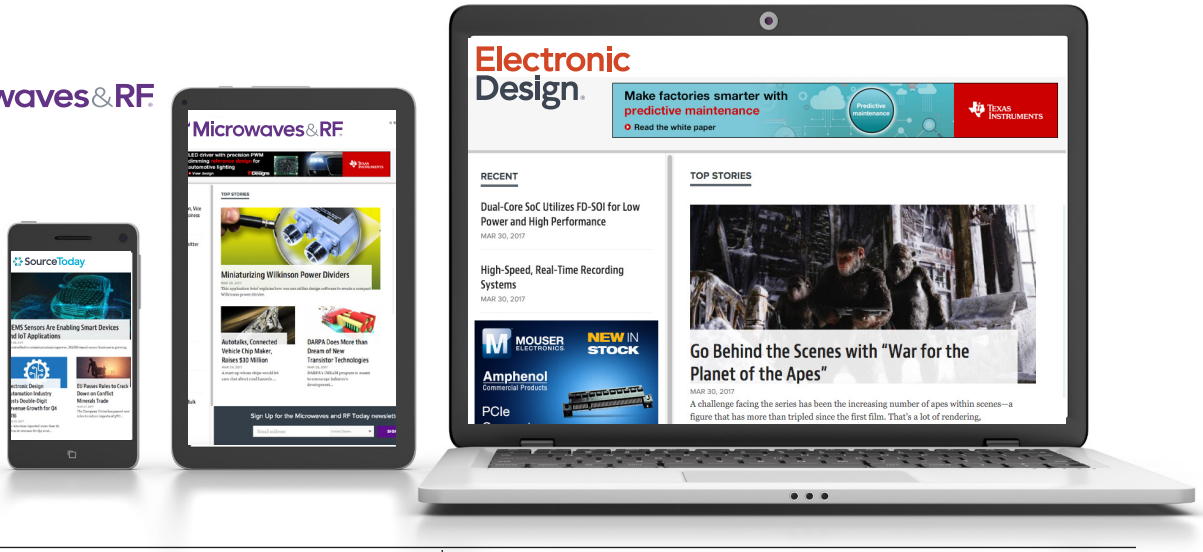

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