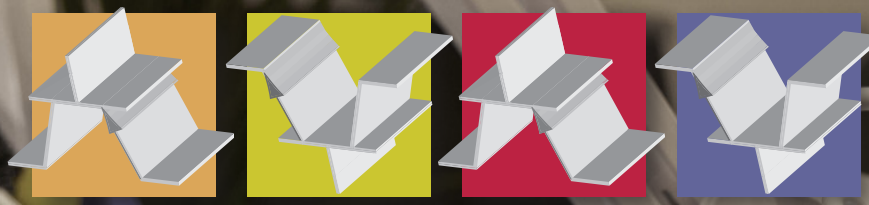
Electronic Design®

Volume 2

Ideas for Design



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Vol. 2, No. 1

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PWM-Based Analog Calculator Provides Four-Quadrant Multiplication, Division

You can build an analog calculator using a pulse-width modulator (PWM) to perform accurate four-quadrant multiplication and division. While this approach won't help you ace any math tests, it demonstrates some useful sub-circuits that extend the functionality of the LTC6992 TimerBloxvoltage-controlled PWM.

Driven Shield Enables Large-Area Capacitive Sensor

This low-cost, large-area capacitive sensor is the wide-scale complement to the ubiquitous, finger-operated touchscreen sensor and can detect presence through plywood or wallboard.

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KENG C. WU | SWITCHING POWER INC., kengchi.goah@ieee.org

Generate Realistic Models For LED Current Versus Voltage

LEDs ARE NONLINEAR devices with I/V curves that resemble the curves of rectifier diodes. Designers of lighting drivers require a good approach to modeling the LED device performance in the first quadrant of the I/V plane.

For engineering applications, there are three approaches to consider: the linear, bias-voltage plus resistor equivalent; a quadratic equation; and an exponential equation. Let's use the three techniques with Cree's XLamp XM-L LED as the LED to be modeled *(Fig. 1)*.

THE LINEAR MODEL

This model is the simplest, but the most inaccurate. It consists of a dc bias voltage plus a resistor *(Fig. 2a)*. The equivalent mathematical form is given by:

$$i_F(v_F) = a + \frac{1}{R}(v_F - b) = \frac{v_F - v_{bias}}{R}, \quad v_F \geq v_{bias} = b - a \cdot R \qquad (1)$$

You select two data points (v_F, i_F) in coordinate form (i.e., 3.28 V, 2.6 A and 2.71 V, 0.2 A). Then, R is evaluated and yields 0.2375. The selection also implies a = 0.2 and b = 2.71. With all three parameters (a, b, R) properly assigned, the linear model yields Figure 2b. Evidently, the linear model offers the advantage of simplicity, but suffers in accuracy.

THE QUADRATIC MODEL

The curve of Figure 1 has a concave portion that resembles one arm of a parabolic curve. It can be expressed with a quadratic equation of the form $a_2 v_F^2 + a_1 v_F + a_0$. The key is the determination of three coefficients: a_2, a_1, and a_0.

To determine these coefficients, you can use the well-known Least Square Polynomial Curve-fitting algorithm of linear algebra. To do this, select more than a dozen data points from Figure 1 (15 in this case) and place them in two matrixes.

One is a 3x15 rectangular matrix C *(Equation 2)*. The other is a 1x15 column vector i_F *(Equation 3)* where vF_j , for j = 0 to 14, are the corresponding LED forward voltages at the selected forward currents given in vector i_F. The three coefficients are then given by a column vector of:

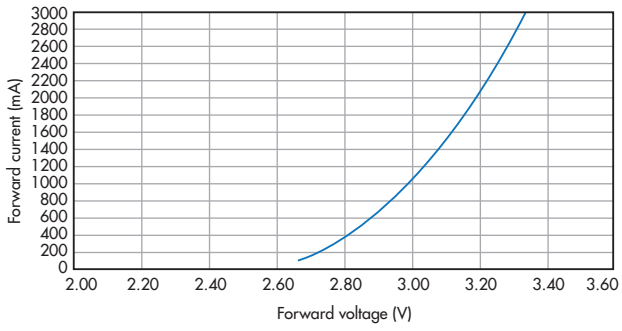
$$a = (C \cdot C^T)^{-1} C \cdot i_F^T \qquad (4)$$

Using software tools such as Matlab from the Mathworks or MathCAD from Mathsoft, you can easily compute Equation 4. For this example, we obtain:

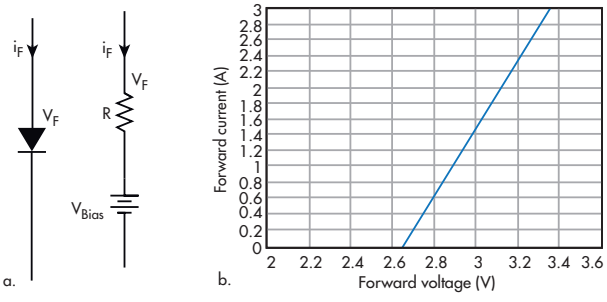
$$a = \begin{pmatrix} 24.849 \\ -20.093 \\ 4.058 \end{pmatrix} \qquad (5)$$

$$C := \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ vF_0 & vF_1 & vF_2 & vF_3 & vF_4 & vF_5 & vF_6 & vF_7 & vF_8 & vF_9 & vF_{10} & vF_{11} & vF_{12} & vF_{13} & vF_{14} \\ (vF_0)^2 & (vF_1)^2 & (vF_2)^2 & (vF_3)^2 & (vF_4)^2 & (vF_5)^2 & (vF_6)^2 & (vF_7)^2 & (vF_8)^2 & (vF_9)^2 & (vF_{10})^2 & (vF_{11})^2 & (vF_{12})^2 & (vF_{13})^2 & (vF_{14})^2 \end{bmatrix} \qquad (2)$$

$$iF := \left(200\,m \;\; 400\,m \;\; 600\,m \;\; 800\,m \;\; 1000\,m \;\; 1200\,m \;\; 1400\,m \;\; 1600\,m \;\; 1800\,m \;\; 2000\,m \;\; 2200\,m \;\; 2400\,m \;\; 2600\,m \;\; 2800\,m \;\; 3000\,m\right) \qquad (3)$$



1. Modeling the I/V curve of the Cree XLamp XM-L LED with increasing accuracy is the objective of this analysis.



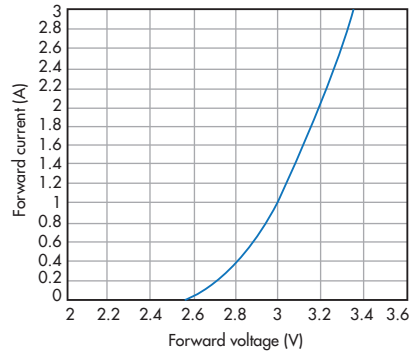
2. The linear model (terminal view) is simplest and easiest to understand, but also the least accurate (a). The linear model results in this "curve," which clearly has some shortcomings (b)

Note that the first element of vector a is coefficient a_0, etc., which leads to the quadratic model of Figure 3. This approach yields significant improvements in the model across the whole operating range of the LED.

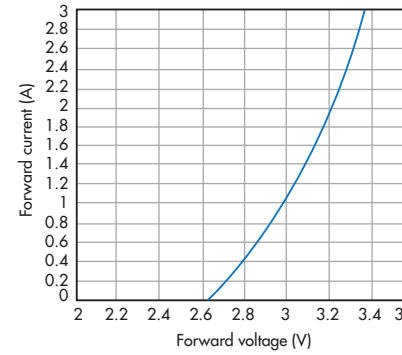
THE EXPONENTIAL MODEL

Figure 3 appears to bend more near the low current, which is where the exponential model may offer further improvement. This model comes in the form of $ae^{b \cdot vF} + c$ with three unknown parameters a, b, and c to be determined. Again, software tools such as MathCAD help you find those parameters numerically.

Under the specialized regression section, an exponential regression statement expfit (v_F, i_F, vg) can find all three parameters, given a data set in vectors and initial guess value vg, also a column vector. For this example, $a = 9.66 \cdot 10^{-3}$, b = 1.818, and c = –1.157 are obtained. This results in the exponential model of Figure 4.



3. The curve based on a quadratic model curve is much closer to the reality of the I/V curve for this LED.



4. The exponential model further refines the quadratic model and provides a better approximation in the low-current region of the LED.

Overall, the best fit near the low-current region may be found between the quadratic and the exponential models. It is unrealistic to expect a single, perfect prediction from any given model, since almost all such analytical efforts are an attempt to represent the complexities of nature.

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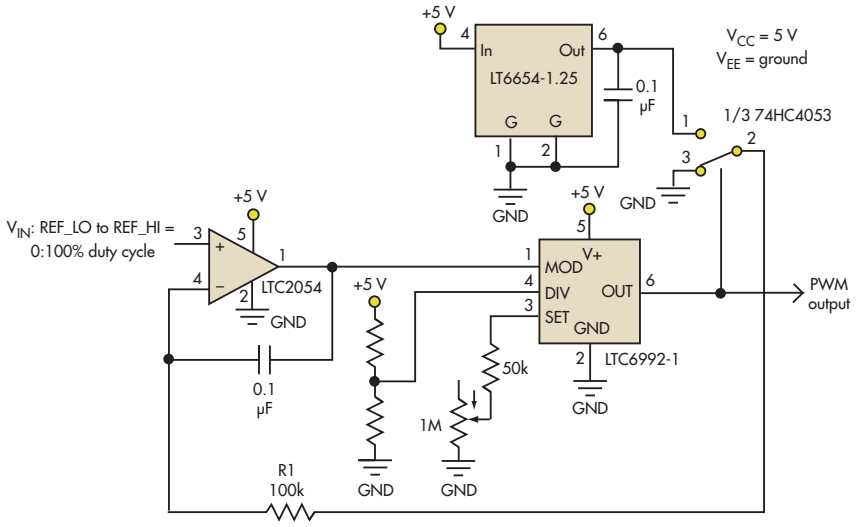
PWM-Based Analog Calculator Provides Four-Quadrant Multiplication, Division

YOU CAN BUILD an analog calculator using a pulse-width modulator (PWM) to perform accurate four-quadrant multiplication and division. While this approach won't help you ace any math tests, it demonstrates some useful subcircuits that extend the functionality of the LTC6992 TimerBlox voltage-controlled PWM.

The LTC6992-1 translates a 0-1 V input at the MOD pin into an output with a 0% to 100% duty cycle at a frequency of 3.81 Hz to 1 MHz. A resistor at the SET pin and a resistor divider at the DIV pin control this frequency. In some applications, the LTC6992 will be in the feed-forward path of a closed-loop control system (as in a motor-speed controller), so its 1% typical linearity provides consistent overall loop performance.



1. This basic linearized PWM generator, without an external feedback mechanism, can still provide accuracy of 0.1%.

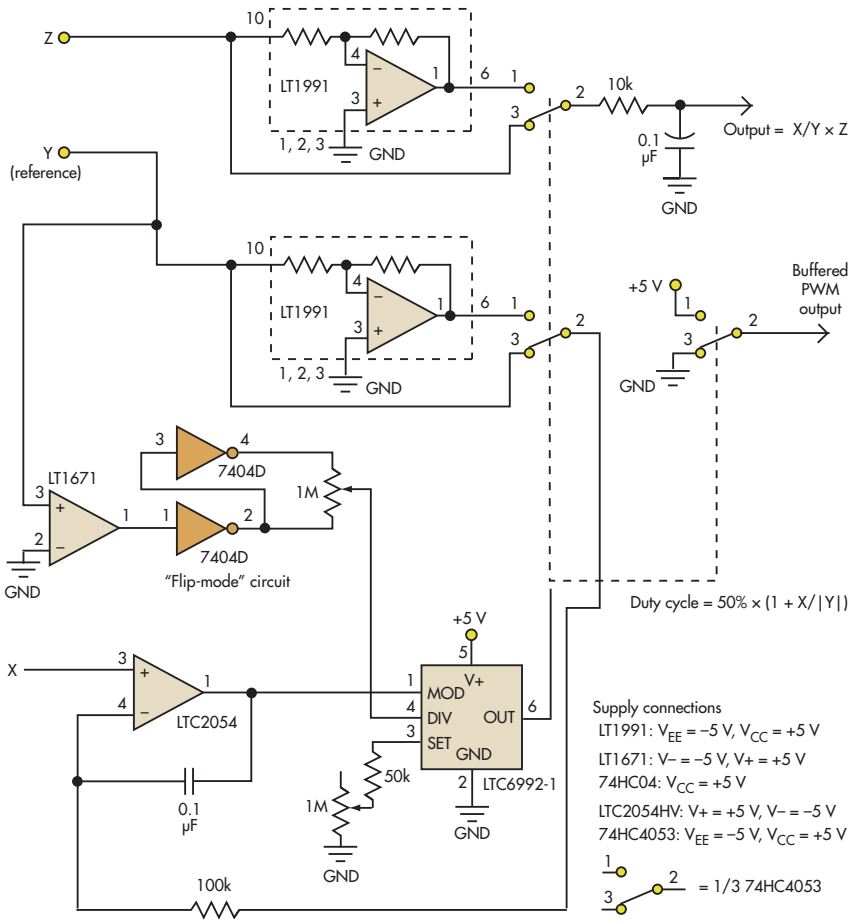
Figure 1 shows a basic linearized PWM generator for applications where accurate PWM is required without an external feedback mechanism. This circuit easily achieves 0.1% PWM accuracy. The output of the LTC6992 controls one section of a 74HC4053 triple single-pole double-throw (SPDT) analog switch whose output is switched between ground and an LT6654-1.25 reference. An integrator compares this signal to the control input. The output duty cycle will settle on a value that equals the fraction of the 1.25-V reference that's present at the input. The term "fraction" implies that this circuit performs division, as the output PWM duty cycle is V_{In}/V_{Ref}.

Figure 2 extends this concept, with X as the input (numerator) and Y as the reference (denominator). An LT1991 configured in a gain of –1 provides a precise negative copy of Y, extending operation to four quadrants (positive and negative X and Y), with duty cycle = 50% × [1 + (X/|Y|)].

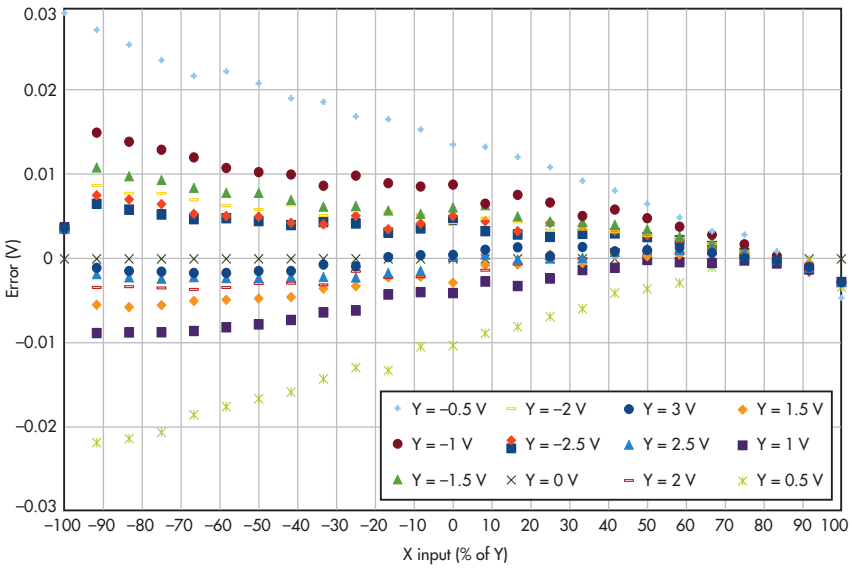
As with any physical realization of division, a zero value for the denominator (Y) will produce an undefined output. A negative voltage applied to the Y input inverts the polarity of the feedback signal to the integrator, which requires another inversion

DIVCODE PROGRAMMING

DIVCODE	POL	N_{DIV}	Recommended f_{Out}	R1 (kΩ)	R2 (kΩ)
0	0	1	62.5 kHz to 1 MHz	Open	Short
1	0	4	15.63 to 250 kHz	976	102
2	0	16	3.906 to 62.5 kHz	976	182
3	0	64	976.6 Hz to 15.63 kHz	1000	280
4	0	256	244.1 Hz to 3.906 kHz	1000	392
5	0	1024	61.04 to 976.6 Hz	1000	523
6	0	4096	15.26 to 244.1 Hz	1000	681
7	0	16384	3.815 to 61.04 Hz	1000	887
8	1	16384	3.815 to 61.04 Hz	887	1000
9	1	4096	15.26 to 244.1 Hz	681	1000
10	1	1024	61.04 to 976.6 Hz	523	1000
11	1	256	244.1 Hz to 3.906 kHz	392	1000
12	1	64	976.6 Hz to 15.63 kHz	280	1000
13	1	16	3.906 to 62.5 kHz	182	976
14	1	4	15.63 to 250 kHz	102	976
15	1	1	62.5 kHz to 1 MHz	Short	Open



2. This enhancement to the circuit of Figure 1 extends the analog multiplication/division to all four analog signal quadrants.



3. This plot of absolute error shows better than 0.1% for large values of Y.

somewhere in the loop to ensure feedback is negative.

The DIV pin also can invert the PWM polarity (a 0- to 1-V input = 100% to 0% duty-cycle output), in addition to selecting one of eight N_{Div} values to set the frequency. The N_{Div} magnitudes are mirrored around $V_{CC}/2$, where swapping values in the resistor divider inverts the transfer function while maintaining the same divider value *(see the table)*.

An LT1671 comparator detects the polarity of the Y input and sets the polarity by switching the divider potentiometer's excitation accordingly, maintaining correct operation. Note that a 10-turn potentiometer works well for experimentation. You could replace it with a fixed resistor once you have selected the desired N_{Div}.

The "Z" input is multiplied by the X/Y quotient by supplying the inputs to another switch with Z and –Z. (Once again, an LT1991 provides precision inversion.) This is a "pulse width/pulse height" multiplier, also with four-quadrant operation.

Figure 3 shows the absolute error of the circuit at a 1.5-kHz frequency, sweeping X from –Y to +Y for values of Y from –3 V to +3 V, while holding Z constant at 5 V. Even with Y at 0.5 V (where error sources are more significant), the worst-case error is about 0.6% and rapidly improves with larger values of Y. Error sources include the 0.04% error of the LT1991, mismatch in switch resistance between its two positions compared with the resistance of the downstream filter's resistance, and the response of the LT1991 outputs to switching transients, whose effect will vary with PWM frequency.

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Driven Shield Enables Large-Area Capacitive Sensor

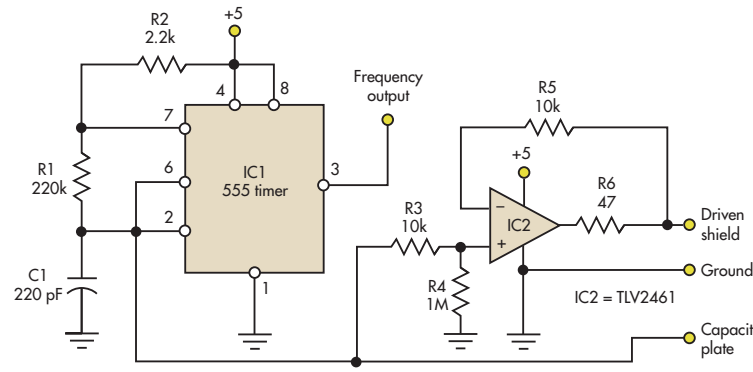
CAPACITIVE SENSORS ARE common in today's consumer electronics, since they are used in many touchscreen applications. Most of the circuits for such applications are designed for small-area capacitors and finger contact operation.

This circuit is designed for large-area touch plates that can be activated at a distance and hidden behind walls or inside other structures. It uses the "driven shield" concept that was popular in the early days of audio engineering, when high-impedance sound sources such as crystal microphones were used. Shielded cables are needed to connect these devices, but the cable capacitance limits the high-frequency response.

The solution to this problem is to go back to the physics of a capacitor to find a way to reduce the cable capacitance. Driving a conductor between the outer shield and the inner, signal conductor with the same voltage as the signal conductor largely eliminates the capacitance. NASA used this driven-shield idea in a large-area capacitive sensor two decades ago (John M. Vranish, et al., US Patent No. 5,116,679).

The circuit in Figure 1 performs the main capacitance-sensing task, while leaving detection to a microcontroller. IC1 is a 555 timer wired as an astable multivibrator with as small a timing capacitance as possible. With the component values shown, the frequency is slightly above 10 kHz. IC2 buffers the voltage on this capacitor to drive a shield plate.

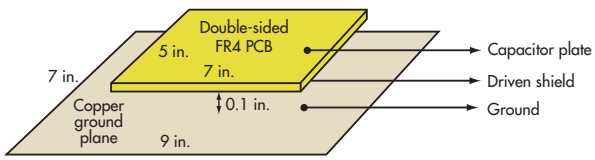
For IC2, resistors R3 and R4 decrease the buffered voltage by about 1%. This prevents oscillation that may occur because of the external capacitance. R6 is included since some operational amplifiers have difficulty driving a capacitive load. IC2 should have a high gain-bandwidth product to allow a faithful representation of the signal voltage without phase shift.



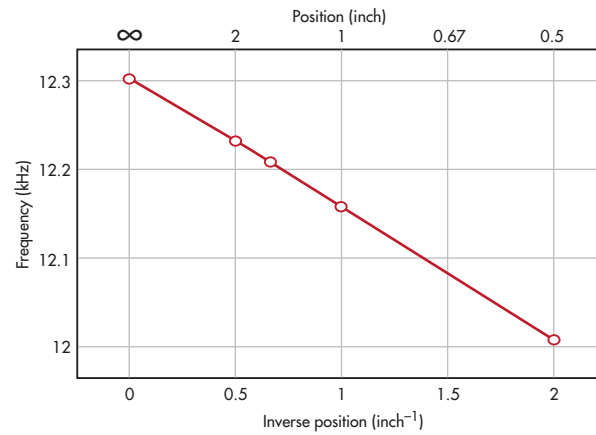
1. In this large-area capacitive sensor, C1 and any parallel capacitance set the frequency of the 555 astable multivibrator IC1, while IC2 buffers the voltage at the capacitor to drive the shield plate. (The pin-outs for IC1 are for the "N" package.)

Figure 2 shows the construction of the sensing plate. These are the dimensions used in the author's tests, but quite a lot of variation is permissible. A practical implementation would be to build the circuitry onto an edge of the ground plane.

The frequency response decreases in a nearly linear fashion with respect to inverse position *(Fig. 3)*. In the author's test, hand contact reduced the frequency to 10.47 kHz. Hand contact through a 0.375-in. (10 mm) thick piece of plywood or gypsum wallboard resulted in a frequency change of 10%, which is easy to detect. Although frequency-detection ICs are available, a simpler, less expensive solution is to use a microcontroller to detect a change in signal period.



2. In the constructed sensor, a double-sided printed-circuit board (PCB) has one conductor as the signal plate and the other as the driven shield. The semi-infinite ground plane, which is slightly larger in area than the sensing or shield plates, can be another PCB or an aluminum plate.



3. The circuit response is a close-to-linear inverse-position relationship between hand position and the sensing plate.

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Electronic Design

Ideas for Design

Vol. 2, No. 2

Test Setup Checks Transistors' h_{FE}s When Tight Control Is Important

This circuit uses pulsed current to check transistor hFE on an oscilloscope. The circuit creates the biasing conditions specified by the transistor's manufacturer..

Multiple Power Supplies Fortify High-Side Gate Control

A switching power supply was devised to ensure high-side FET gate control, particularly in light of a wildly floating high-side rail. The design's "VeeDrive" delivers a sharp and muscular square-wave that's robust enough to drive several charge pumps.

High-Side Switch Provides Overvoltage Protection With Only Four Components

Low-voltage microcontrollers often need to control higher-voltage loads via high-side switching. This simple two-transistor circuit enables that control and provides over-voltage protection.

Add Short-Circuit Protection, Diagnostics To Automotive High-Side/Low-Side Driver

Smart switches for automotive applications are costly, may not be readily available for 24-V operation, and often come in unneeded dual and quad configurations. By adding a few standard, low-cost components to a basic driver, you can make a smarter one which includes short-circuit protection and built-in diagnostics.

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We look forward to seeing your ideas.

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Test Setup Checks Transistors' h_{FE}s When Tight Control Is Important

THE SPREAD OF h_{FE} values in a batch of transistors may be wide enough to cause unreliable performance during mass production of a system. Consequently, bench evaluation of h_{FE} may be required during the system's development stage. Designers may have to screen samples over a spread of several years of date codes. Sometimes these measurements are made using pulsed collector current.

This idea describes how to make such measurements. For example, the QSZ2 transistor (2SB1695) specification states three biasing requirements on h_{FE}: I_C = 0.1 A, V_{CE} = 2 V, and Δt_w = 1 ms. The circuit in Figure 1 meets these requirements for h_{FE} measurement for a QSZ2 pnp transistor.

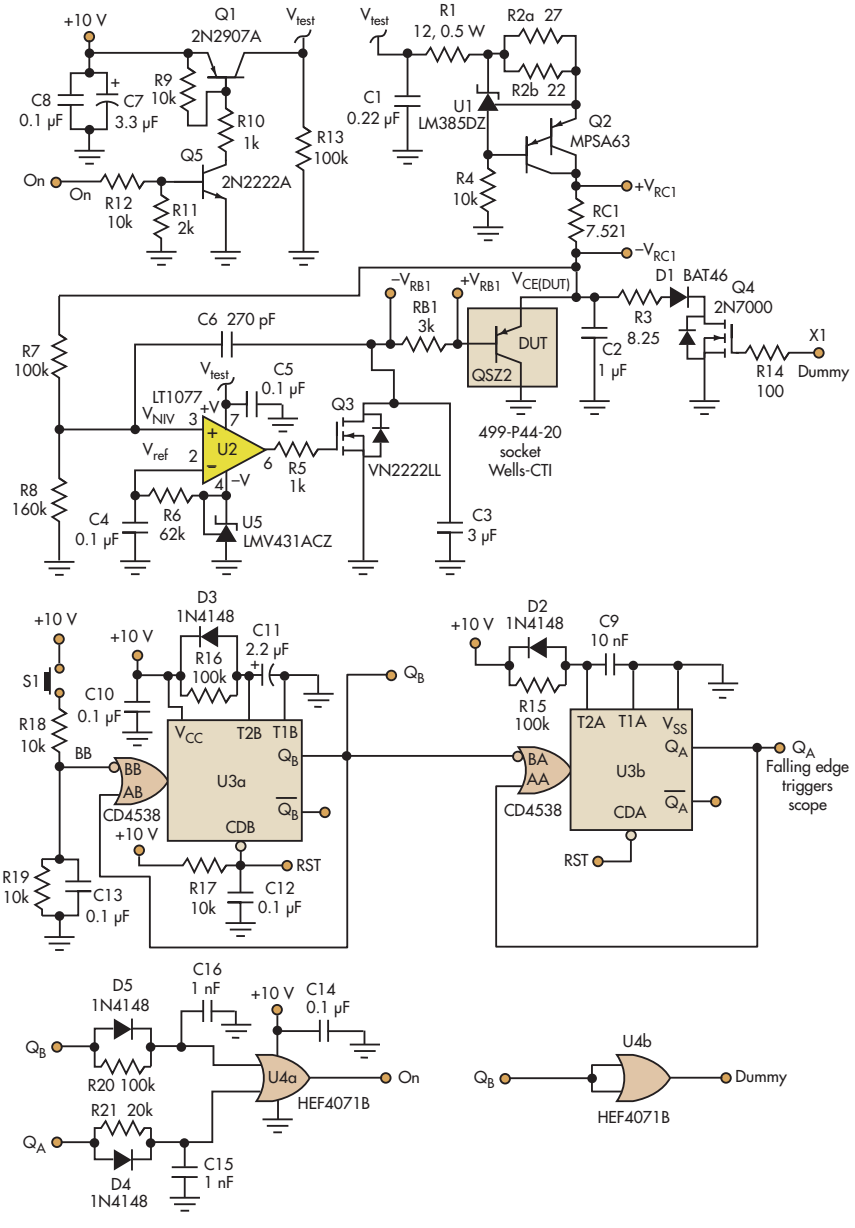
Zener U1 and its associated components form a current regulator that sources 0.1 A to the succeeding stage. During the test period (Δt_W in Figure 2), U2's feedback mechanism trims the base resistance of the device under test (DUT) while maintaining its V_{CE} at the required 2 V. This is expressed in Equation 1, in which R_{DSQ3} is automatically tuned against $I_{B(DUT)}$ and, therefore, h_{FE} and $V_{BE(DUT)}$ variations:

$$V_{CE(DUT)} = V_{BE(DUT)} + V_{RB1} + V_{DSQ3} = 2\ V$$
$$V_{BE(DUT)} + I_{B(DUT)}\left(R_{B1} + R_{DSQ3}\right) = 2\ V \qquad (1)$$

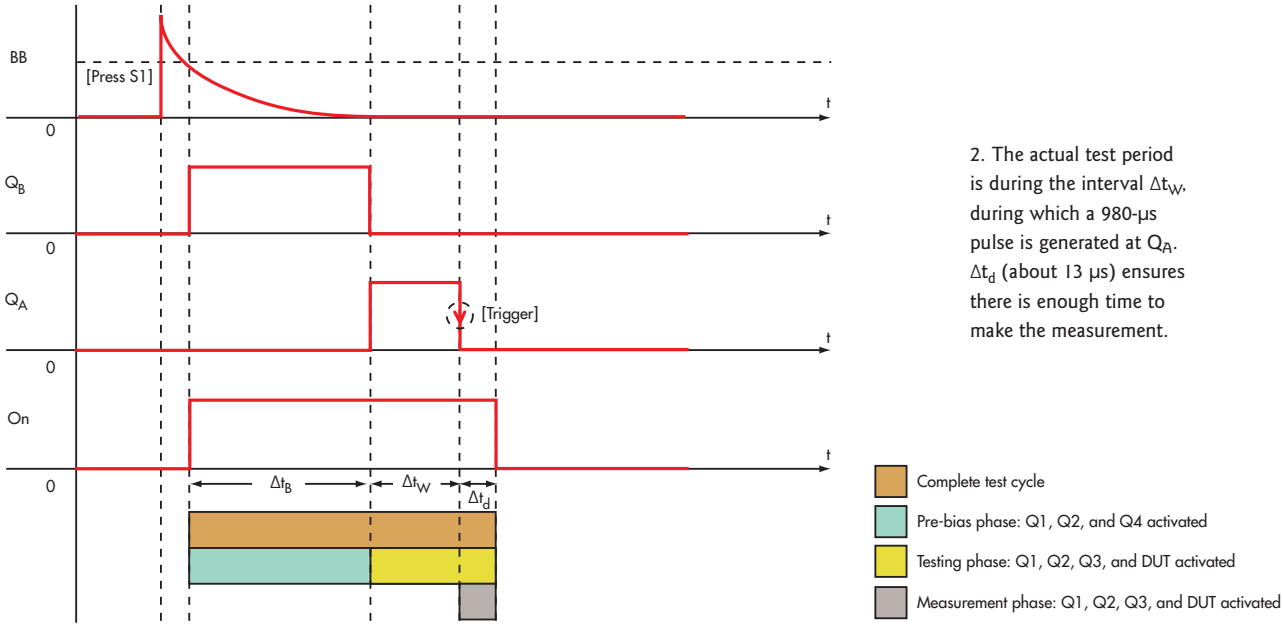
Equation 2 then allows you to determine the value of the DUT's h_{FE} by monitoring V_{RB1}:

$$\frac{I_E}{I_B} = \left(h_{FE} + 1\right) \approx h_{FE} \text{ if } h_{FE} \gg 1$$
$$h_{FE} = \frac{0.1\ A}{\frac{V_{RB1}}{3 \times 10^3}} = \frac{300}{V_{RB1}} \qquad (2)$$

Basically, resistor RB1's value is set as large as possible to minimize the oscillation of $I_{B(DUT)}$ upon transition and to



1. This test circuit provides the biasing conditions needed to evaluate a transistor's h_{FE} according to the manufacturer's criteria. In this example, the device under test is a QSZ2 (2SB1695), and the values chosen are specific to that device.

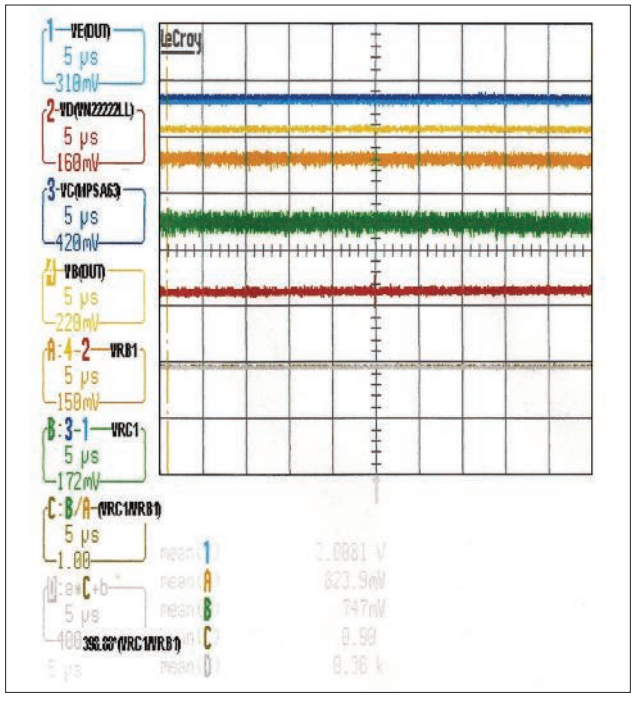


2. The actual test period is during the interval Δt_W, during which a 980-µs pulse is generated at Q_A. Δt_d (about 13 µs) ensures there is enough time to make the measurement.

maximize the signal level to ease V_{RB1} monitoring. The h_{FE} of a QSZ2 ranges from 270 to 680, so $I_{B(DUT)}$ falls between 147 µA and 370 µA.

Next, assume the worst-case $V_{BE(DUT)}$ variation of 0.5 V to 0.8 V. Then:

$$R_{B(min)} = \frac{\left(V_{CE(DUT)} - V_{BE(max)}\right)}{I_{B(max)}} = \frac{(2-0.8)}{370\ \mu A} = 3.243\ k\Omega \quad (3)$$



3. The falling edge of Q_A triggers an oscilloscope, which uses V_{RB1} (trace A) and V_{RC1} (trace B) to calculate h_{FE} (trace D).

$$R_{B(max)} = \frac{\left(V_{CE(DUT)} - V_{BE(min)}\right)}{I_{B(min)}} = \frac{(2-0.5)}{147\ \mu A} = 10.204\ k\Omega \quad (4)$$

Choose RB1 so that it is slightly below $R_{B(min)}$.

The circuitry around U3 forms two cascading one shots that, when triggered by S1, generate a 220-ms pulse ($\Delta t_B \approx R16 \times C11$) at the Q_B output. This is followed by a 980-µs pulse, Δt_W (determined by R15 and C9), at Q_A. The first pulse pre-biases and stabilizes the current source while the second one provides the needed test pulse for the DUT.

During Δ_{tB}, Q_4 is activated to sink the 0.1 A of U1, and R3 is selected so the effective voltage drop across R3, D1, and Q4 (and thus $V_{CE(DUT)}$) is slightly less than 2 V (about 1.7 V in this example). This forces U2's output and the DUT to stay "low" and "off," respectively.

At the end of Δt_B, Δt_W starts and Q4 is turned off, transferring the test current to the DUT. U2 then raises $V_{CE(DUT)}$ to 2 V and regulates it.

The high-to-low transition at the Q_A output after Δt_W triggers the measuring device (in our example an oscilloscope) *(Fig. 3)*. V_{RC1} and V_{RB1}, which correspond to I_C and I_B of the DUT, are recorded upon Q_A's trigger. R21 and C15 create Δt_d (about 13 µs), which ensures enough time to make the measurement before Q1 is gated "off."

For more, see "Anoop's Analysis" with the online version of this article at electronicdesign.com.

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Multiple Power Supplies Fortify High-Side Gate Control

FOR A RECENT design project, a robust power supply was needed to control the gates of high-side FETs. Optocouplers readily translate the logic signals up to the correct control voltages to drive the FETs. However, to ensure that the FETs turn on and off cleanly, the design required a solid –15 V relative to a wildly floating high-side rail.

A simple Zener diode and resistor, possibly with a FET buffer to ensure adequate current, might do the job under some conditions. In certain circumstances, though, the required gate drive would dip slightly below the lowest other supply rail in the system, which is in this case GND, since there are no negative supplies. At other times, it could be almost 100 V above all other supply voltages. Since the design in question was to be used in a production scheme, the solution had to stay away from proprietary, expensive, single-source parts.

The design already included a switching supply to efficiently convert from an incoming supply at approximately 12 V, down to an internal logic supply at 4 V *(Fig. 1)*. The switch node of that supply, at the junction of U610 pin 3, L610, and D611, swings between the incoming 12-V rail and a diode drop below ground—approximately –0.5 V. This could provide the feed for a charge pump. However, the 4-V supply can't be lightly loaded, which would cause insufficient drive at this point to support a charge pump.

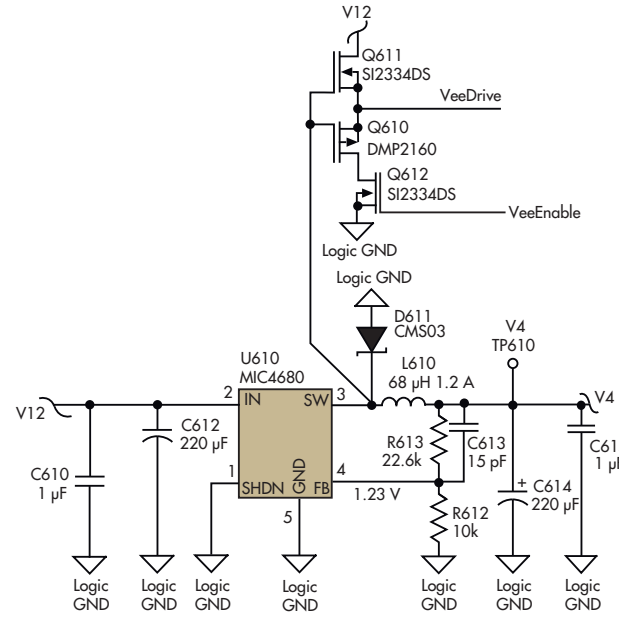
To guarantee a solid drive for the charge pump, power is derived directly from the 12-V supply and ground using transistors Q610 and Q611. Note that these aren't configured in a traditional inverter configuration, which could suffer from shoot-through when both are turned on simultaneously during the gate's voltage transition.

Instead, transistors Q610 and Q611 are simple source-followers. As the gate voltage rises more than about a volt above the present value of net VeeDrive shown in Figure 1 at the source terminals of Q610 and Q611, Q611 turns on, pulling up VeeDrive so it remains about 1 V below the gate voltage all the way up. On the falling edge at the switch node, the gate voltage falls, Q611 is turned solidly off, and Q610 begins to turn on as the gate voltage falls about 1 V below VeeDrive. Therefore, VeeDrive follows the gate voltage down to within about 1 V of Logic GND.

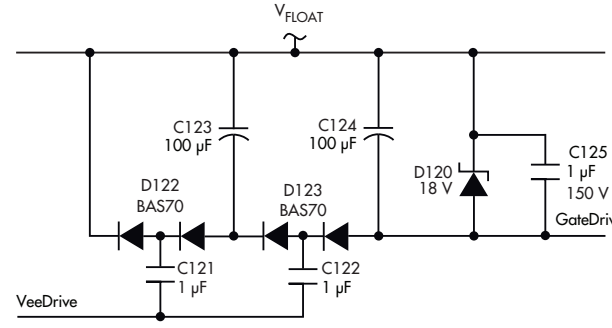
As a result, VeeDrive provides a sharp and muscular square-wave that swings between about 1 V and 11 V (relative to Logic GND), for a total of 10 V p-p. It's robust enough to drive several charge pumps, if the need arises for multiple supplies. In fact, this one square-wave provided all four supplies required by the design at hand.

Q612 is an optional component. Raising net VeeEnable, the gate drive to Q612, to a logic high voltage turns on Q612 and enables the charge pump action. Lowering VeeEnable back to Logic GND turns off Q612 and disables the low-side drive, allowing VeeDrive to settle to a steady state just below V12. This will save power during those times that don't require the GateDrive supply.

Figure 2 shows one of the four charge pumps using VeeDrive to provide a floating supply that follows a specific floating rail V_{FLOAT}. Because the gate drive must be at least 10 V below V_{FLOAT}, and some drops occur in the diodes, a two-stage



1. The 12-V downswitcher, which is already in the design, provides a square-wave to generate VeeDrive from V12 with about a 10-V swing.



2. The charge pump generates a robust supply that always tracks 15 V below V_{FLOAT}, even if that voltage is below ground. The voltage also can be placed above V_{FLOAT} by simply reversing the diodes and the polarized capacitors.

charge pump is employed. My actual design includes four copies of the charge pump shown in Figure 2 to produce GateDrive relative to each of four different floating supply rails. A single VeeDrive drives all four rails.

Starting with accumulators C123 and C124 discharged, when VeeDrive goes low (1 V), C121 charges up through C123 and the right half of dual diode D122 to approximately V_{FLOAT} – 1.5 V (after accounting for an approximate 0.5-V drop of the diode). When VeeDrive goes high (11 V), C121 discharges through the left half of D122 to V_{FLOAT} – 10.5 V (11 V – the 0.5-V drop in the diode). As cycling continues, charge continues to be drawn through C123, gradually charging up C123. In steady state, with no current being drawn off, C123 will charge up to 9 V, leaving its negative end at V_{FLOAT} – 9 V.

The second-stage charge pump, consisting of C122, D123, and C124, operates similarly to produce an additional 9-V offset. As a result, GateDrive is 18 V below V_{FLOAT}. In actual practice, of course, some current is being drawn off and there are more resistive drops, so the actual voltage settles close to 15 V. Should the voltage somehow exceed 18 V, Zener D120 clamps the voltage to no more than 18 V, which guarantees that the GateDrive's 20-V maximum limitation isn't surpassed. C125 helps to suppress switching noise caused by sudden loads on the supply during switching.

This arrangement can be readily adapted to many situations. If V_{FLOAT} can change, even fairly rapidly, the large size of accumulators C123 and C124 relative to flying capacitors C121 and C122 ensures that GateDrive maintains a fairly constant offset from V_{FLOAT}. This will hold true while the flying capacitors rapidly charge or discharge to the appropriate levels to continue the charge pump action.

Because the flying capacitors are ceramic (and thus unconcerned about polarity), GateDrive will remain 15 V below V_{FLOAT}, even if V_{FLOAT} should fall all the way to Logic GND or below. The flying capacitors must, however, have a sufficient voltage rating so that the highest value of V_{FLOAT} can occur in practice.

The output voltage at GateDrive is very consistent in practice and nicely matches the theoretical values after accounting for the various drops in the feed. There are several ways to adjust this voltage, though. Stages can be easily added to or removed from the charge pump to produce different multiples of the input voltage. If the input voltage is adjustable, finer granularity is possible.

It's easy to configure GateDrive when it must be above rather than below V_{FLOAT}. Simply flip the polarized accumulator capacitors to allow for the new state, and reverse the diodes. With those simple changes, the design will produce GateDrive at approximately V_{FLOAT} + 15 V.

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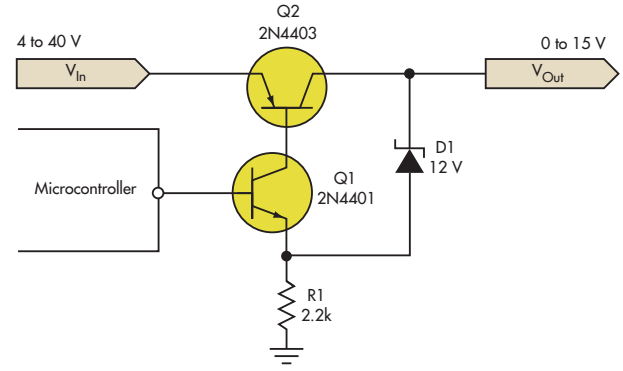
High-Side Switch Provides Overvoltage Protection With Only Four Components

ALTHOUGH MICROCONTROLLERS GENERALLY run at low voltages, such as 3.3 V, they often need to control loads running at higher voltages like 12 V. If switching the low side isn't an option, the microcontroller needs a way to control a high-side switch from its low-voltage output.

The circuit in the figure provides a simple solution. Besides using few components, it provides overvoltage protection as a bonus. As long as the input voltage stays below approximately 15 V, the output voltage will equal the input voltage (minus the tiny V_{CE} drop across transistor Q2).

Once the input voltage exceeds that limit, however, the circuit begins acting as a low-dropout regulator (LDO), limiting the output voltage to 15 V. This feature is useful if the input voltage occasionally exceeds the rated load voltage, but the load switch needs to remain efficient otherwise.

Transistor Q1 and resistor R1 form a current sink. The microcontroller's output voltage (V_{OH}) and Q1's base-emitter drop (V_{BE}) create a stable voltage across the resistor, producing a current of (V_{OH} – V_{BE})/R1, or about 1.2 mA for a 3.3-V microcontroller. Most of this current flows through Q2's base,



The microcontroller turns the load off by controlling a high-side switch formed by Q1 and Q2. The current-sink action of Q1 controls the load voltage.

which controls the load. This current drops to zero when the microcontroller output goes low, switching the load off.

Zener diode D1 provides an alternative path for R1's current. If the diode's breakdown current is V_Z, it will begin to conduct when the output voltage exceeds $V_Z + V_{OH} - V_{BE}$, or about 14.6 V for a 12-V diode and a 3.3-V microcontroller. Since the voltage across R1 is constant, the diode effectively "steals" current from the base of Q2, reducing the amount of current flowing into the load. This negative feedback causes the circuit to act like a voltage regulator.

To apply this circuit to your application, adjust R1 so Q2's base current equals the maximum load current (I_{MAX}) divided by Q2's gain (β), or $R1 = \beta \times (V_{OH} - V_{BE})/ I_{MAX}$. Be sure to select a transistor for Q2 that can dissipate the heat generated during an overvoltage event.

There is no straightforward way to calculate the exact output voltage, so the quickest approach is to try a few Zener diode voltages and pick the one that works. A good starting point is to pick Zener voltage V_Z to equal to the desired output voltage minus the microcontroller voltage. This is just an overvoltage protector, so great accuracy should not be necessary.

If the overvoltage protection isn't important, simply remove the Zener diode. The resulting load switch uses only three components and retains the advantage of driving Q2's base with an actual current source. Even if the input voltage changes, Q2's base current remains constant.

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Add Short-Circuit Protection, Diagnostics To Automotive High-Side/Low-Side Driver

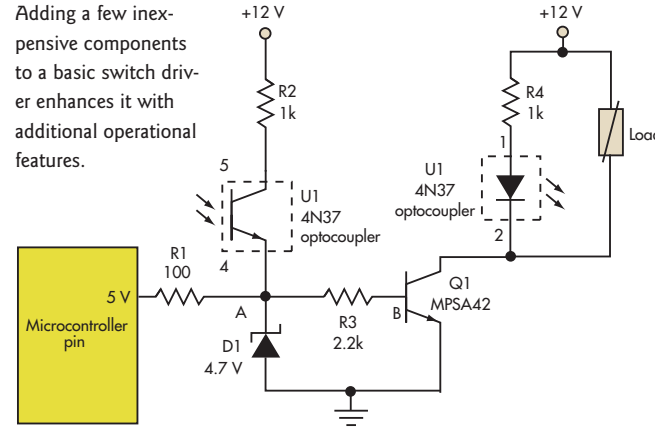
AUTOMOTIVE APPLICATIONS NEED "smarter" drivers for their switches, which handle loads ranging from a fraction of an ampere to several amperes. Not only are these smart chips costly, but many times, they also aren't available for the 24-V applications used in this application area. Further, they usually come in quads and pairs, so designers are paying for unused switches.

The simple circuit in the figure adds a few low-cost components to a "dumb driver" to make it a smart one, with added short-circuit protection and built-in diagnostics *(see the figure)*. Transistor Q1 is an inexpensive driver that can withstand a few hundred volts and drive a few hundred milliamps. The microcontroller output goes high to latch the transistor on via the phototransistor of optocoupler U1. It next configures the output pin into an input, while U1 keeps the transistor on by supplying its base current through R2.

U1 has its LED in the load circuit of Q1 for detecting the short circuit. Under short-circuit conditions, it is "starved" of current, turning off the phototransistor driving power-switch Q1's base and protecting it. The CPU input pin can sample the occurrence of the short circuit at its convenience as needed, such as every few seconds.

The voltage at point A changes from a few hundred millivolts during short circuit to 4.7 V during normal operation, providing a clear indication to the CPU's input port. For retry-based recovery from short circuit, the CPU may turn itself into an output again at its leisure for restoring the "on" status and recovering the switch from its "trip-off" condition. The CPU pin again now goes into input mode to sense if the external short is persisting. Depending on the application, a suitable retry regime can be worked out based on the end application.

Adding a few inexpensive components to a basic switch driver enhances it with additional operational features.



During normal operation, the CPU can easily turn off the switch by pulling the output low. The CPU can issue a logic low by turning the pin into output again whenever it needs to switch Q1 off during normal operation.

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Electronic Design

Ideas for Design

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SPI Eases Interfacing For 5-By-5 Dot-Matrix Display

The circuit interfaces a display that features four 5-by-5 dot-matrix characters by using the display's serial peripheral interface and a programmable system on a chip (PSoC). The SPI reduces firmware overhead and enhances clock stability.

Use An LED Dot-Graph Display To Complement Your DVM Readout

The digital voltmeter is a great tool, but it can show confusing results when the input voltage is unstable or erratic; by adding an auxiliary circuit driving a string of LEDs, you can easily also get a sense of the variations in input voltage.

Lamp Eliminates Need For Limit Switches In Flap-Motor Control

A flap controller needs current limiting to protect the motor when the flap reaches full closure. A small incandescent lamp can perform this task without the need for more costly limit switches or a microcontroller.

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SPI Eases Interfacing For 5-By-5 Dot-Matrix Display

WHEN DISCUSSING DISPLAYS, seven-segment displays and LCDs are among the first that come to mind. Each type has its pros and cons. But generally, seven-segment displays cannot display letters, and LCDs tend to be bulky. Recently, I came across a four-character 5-by-5 dot-matrix, serial-input display (the SCDV5542 from Osram) that has several advantages.

The display can display alphanumeric characters and measures 10.16 by 19.91 mm (0.400 by 0.784 in.) with 3.12-mm (0.123-in.) characters. It has a serial peripheral interface (SPI) and allows high-speed data input. It features eight levels of dimming, an internal/external clock capability, and decoders, multiplexers, and an LED driver.

The device consists of a CMOS IC with control logic and drivers for the four 5-by-5 characters *(Fig. 1)*. Each individual LED dot is addressable, so the user can create special characters. The device requires only four lines from a microcontroller. The IC accepts decoded serial data that is stored in internal RAM. Asynchronously, the RAM is read by the character multiplexer at the rate defined by the strobe.

The microcontroller supplies a string of bit-mapped characters *(Fig. 2a, b, and c)*. Each character consists of six 8-bit words. The first word is the character address. It's followed by the row data, which represents the on/off status of each LED in the column. Each bit of the 8-bit word consists of a 3-bit opcode (D7-D5) and 5 bits (D4-D0) of column data or character address or control word data.

To load data, bring the $\overline{\text{Load}}$ line low, which puts data in the serial register *(Fig. 2d)*. The shift action occurs on the low-to-high transition of the serial clock (SDCLK). The least significant bit (D0) is loaded first. After one word is transferred, the $\overline{\text{Load}}$ line is set to high for opcode decoding. The decoded opcode latches D4-D0 in the character address register. The time between loads must be at least 600 ns. The character address register bits (D0-D4) and row address register bits (D7-D5) direct the column data bits (D4-D0) to a specific RAM location.

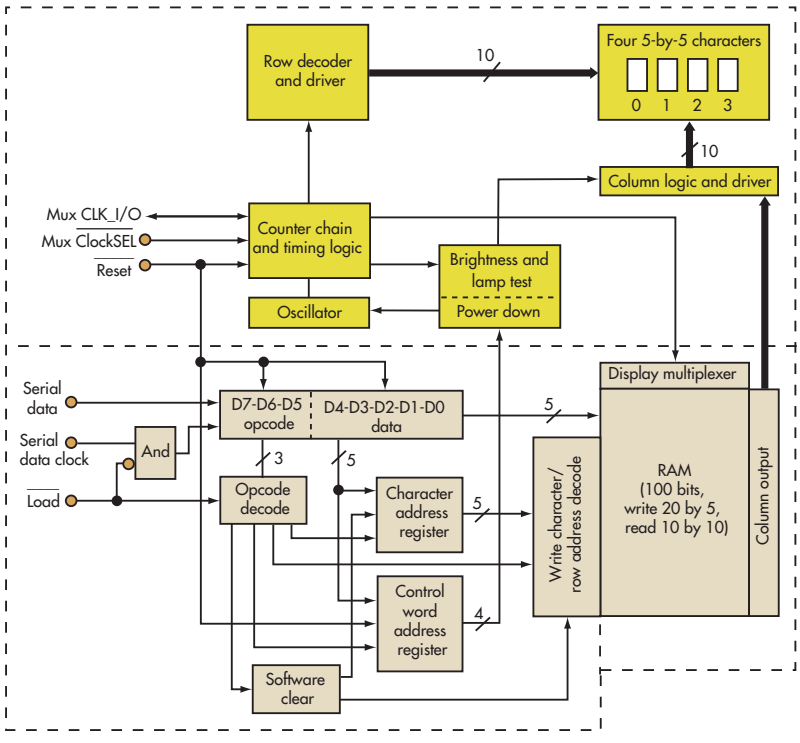
The load character address tells the display the location *(Table 1)*. The load column data controls the individual LED dot *(Table 2)*. This feature allows you to create your own special symbols.

The display has seven brightness levels, defined by the percentage of full brightness that can be achieved: 100% (0xF0), 53% (0xF1), 40% (0xF2), 27% (0xF3), 20% (0xF4), 13% (0xF5), and 6.6% (0xF7). To control the brightness level, change the duty factor of the strobe pulse. Table 3 shows an example line.

In the power-down mode, the display brightness is set to 0% and the clock to the internal multiplexer is stopped, reducing the quiescent current, I_{CC}, to 50 µA *(Table 4)*. The display is reactivated by loading a new brightness level control word into the display. During power-down mode, data can be written to RAM.

Table 5 illustrates the operation of the lamp test mode, which sets all the LEDs to 53% brightness. This operation can be cleared by loading a brightness level control word.

Finally, the software-clear mode clears the address register and the RAM *(Table 6)*. The



1. The SCDV5542 four-character 5-by-5 LED dot-matrix display stores decoded serial data in a 100-bit internal RAM. Users can address each dot individually so they can generate custom characters.

TABLE 1: LOAD CHARACTER ADDRESS

Opcode			Character address					Hex	Operation load
D7	D6	D5	D4	D3	D2	D1	D0		
1	0	1	0	0	0	0	0	A0	Character 0
1	0	1	0	0	0	0	1	A1	Character 1
1	0	1	0	0	0	1	0	A2	Character 2
1	0	1	0	0	0	1	1	A3	Character 3

TABLE 2: LOAD COLUMN DATA

Opcode			Column data					Operation load
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	C0	C1	C2	C3	C4	Character 0
0	0	1	C0	C1	C2	C3	C4	Character 1
0	1	0	C0	C1	C2	C3	C4	Character 2
0	1	1	C0	C1	C2	C3	C4	Character 3

TABLE 3: DISPLAY BRIGHTNESS

Opcode			Control word					Hex	Operation load
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	1	1	0	0	0	1	F1	53%

TABLE 4: POWER DOWN

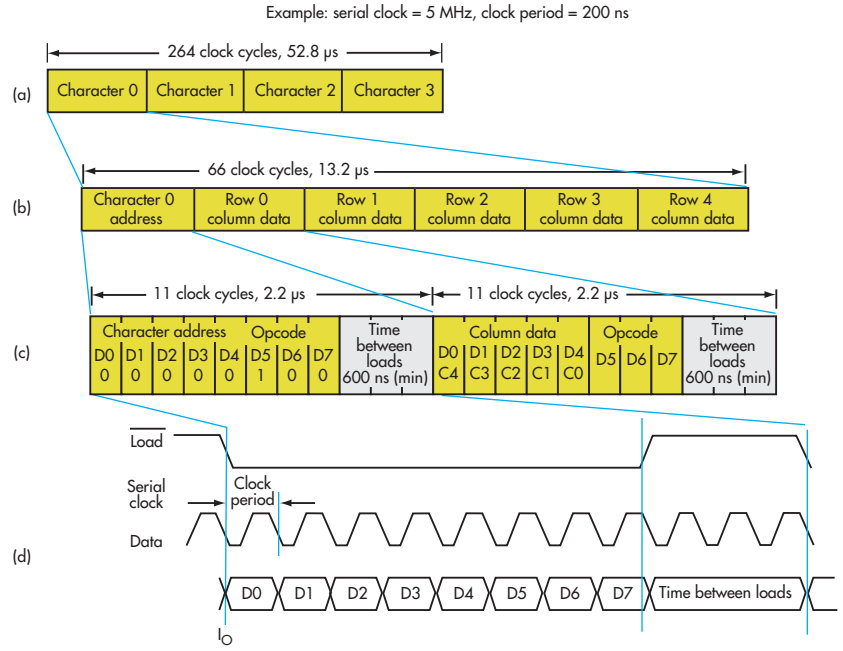
Opcode			Control word					Hex	Operation Level
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	1	1	1	1	1	1	FF	0% brightness

TABLE 5: LAMP TEST

Opcode			Control word					Hex	Operation Level
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	1	1	1	0	0	0	F8	Lamp test

TABLE 6: SOFTWARE CLEAR

Opcode			Control word					Hex	Operation Level
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	0	0	C0	Clear



2. The bit-mapped characters supplied by the microcontroller occur within certain timing specifications. The times in this example are based on the use of a 5-MHz clock (a period of 200 ns).

display is blanked and the character register address is set to character 0. The internal counter and control word register are unaffected.

The example circuit uses a Cypress CY8C27443-24PXI programmable system-on-chip (PSoC) and a program written in C. I chose the PSoC because it enables designers to select individual hardware blocks. The serial interface to the display is straightforward and easy.

There are two ways to interface the display. The first is to connect a microcontroller via the serial port in mode 0. The serial port control register will be a simple shift register. Serial data enters and exits through the RXD pin, and the TXD pin outputs the clock.

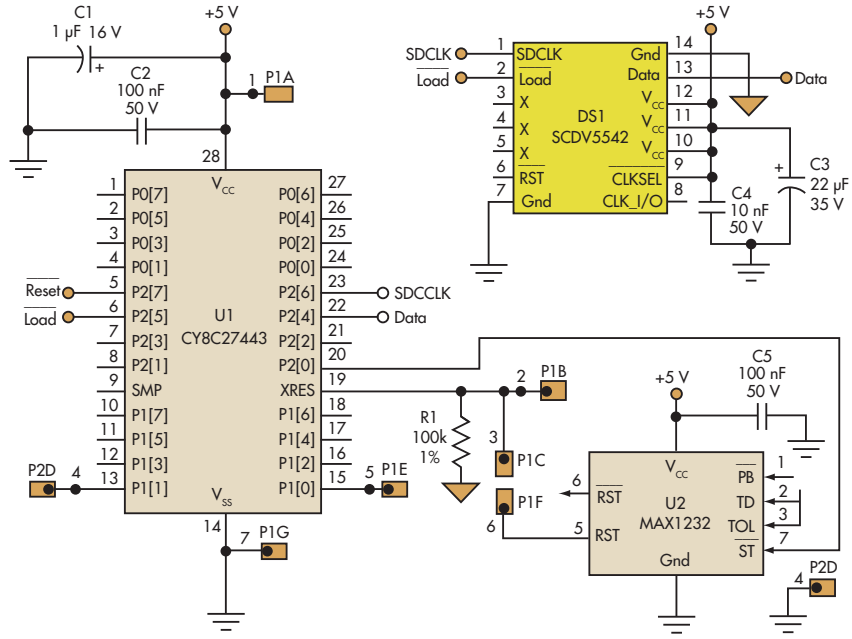
The second method interfaces the display via the SPI in mode 0. Besides MISO (master in slave out) and clock, the display needs $\overline{\text{Reset}}$ and $\overline{\text{Load}}$ control lines. I chose SPI for this project because of its inherent advantages over serial port *(Fig. 3)*. The circuit uses a MAX1232 as a reset controller, but you can choose any other method for properly resetting the microcontroller.

As noted, the PSoC enables you to choose your own hardware modules, which speeds development. For this project I opted for the SPI hardware instantiation to reduce firmware overhead. This choice also ensures the clock is stable and isn't influenced by other priority events.

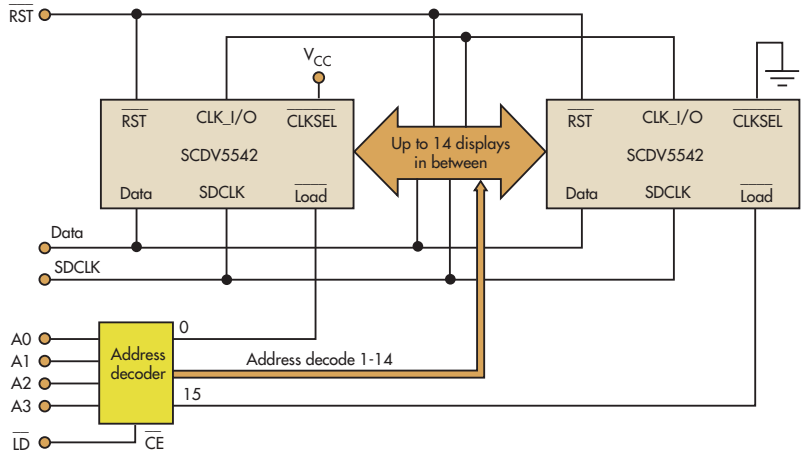
Instantiating SPI simplified the display's communication block. Below is the flow chart for firmware implementation. (The code for the demo project can be downloaded from the online version of this article at *electronicdesign.com*.)

- Power up the display.
- Bring $\overline{\text{Reset}}$ low (for at least 600 ns) to clear the multiplex counter, address register, control word register, user RAM, and data register. The display will be blank. The display brightness will be set to 100%.
- If different brightness is desired, load the proper display brightness control word from Table 4.
- Load the character address into the display *(Table 1)*.
- Load column data into the display *(Table 2)*.
- Repeat steps 4 and 5 for rest of the digits.

Finally, one display CLK_I/O line can drive 15 slave CLK_I/O lines, so you can cascade displays to increase the



3. The author opted to use a SPI instantiation for the display because it reduced the firmware overhead required.

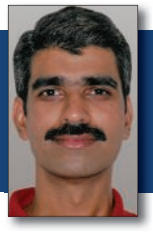


4. The display's CLK_I/O line can drive up to 15 slave CLK_I/O lines, so designers can easily cascade multiple units.

project's display capabilities. Figure 4 shows the block diagram for interfacing multiple displays.

SOURCES

1. Osram SCDV5542 display, catalog.osram-os.com/media/_en/Graphics/00034132_0.pdf
2. Cypress Semiconductor CY8C27443-24PXI, www.cypress.com/?mpn=CY8C27443-24PVXI
3. Cypress Semiconductor PSoC Designer, www.cypress.com/?id=2522
4. Maxim Integrated MAX1232, www.maximintegrated.com/datasheet/index.mvp/id/1286



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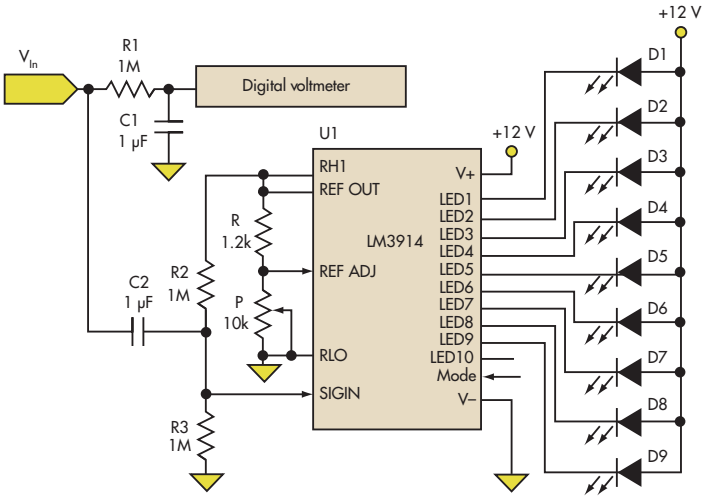
Use An LED Dot-Graph Display To Complement Your DVM Readout

LEDS OFTEN ARE used to form a dot/bar graph display.[1-4] You also can use an LED dot-graph display as a complement to a digital voltmeter (DVM) with the LM3914 dot/bar display driver and nine LEDs.[5] This is useful where the input voltage is unstable, so the voltmeter indications are variable and the result is hard to read and understand.

By adding an associated circuit, the DVM measures and displays the approximate mean value of the input voltage, while the LED dot-graph provides information about the voltage's stability. This approach is suitable for rapidly testing power supplies.

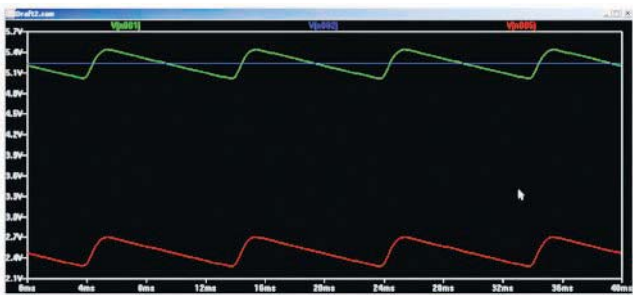
The input signal passes through low-pass filter R1C1 to a digital voltmeter *(Fig. 1)*. The filter's output is the mean value of the input signal, so the voltmeter indicates it is stable, and it is easy to read. (If the digital voltmeter has a built-in averaging option, the low-pass filter is not required.) Capacitor C2 passes the variable component of the input voltage to U1, and the LED dot graph that U1 drives indicates the intensity of these variations.



1. The LED dot-graph display uses a standard display driver preceded by a high-pass filter. It visually complements a digital voltmeter's numeric output.

Figure 2 (obtained by simulation) shows how the low-pass and high-pass filters pass the mean and variable components of the input signal, respectively. If the input voltage is stable and doesn't have any ripple, only central LED D5 lights up.

As voltage ripples increase, the adjacent diodes begin to flicker. For larger ripples, more of the adjacent diodes light. Potentiometer P controls the LED dot-graph's sensitivity, with maximum sensitivity of 0.125 V when P is set to 0 Ω. Nine of the 10 available LED outputs are used.



2. The simulation of the waveforms of V_{In} (V[n001]) as well as the voltage at the low-pass filter output (junction of R1/C1) (V[n002]) and at the high-pass filter output (junction of R2/R3/C2) (V[n003]) show how the low-pass and high-pass filters pass the mean and variable components of the input signal, respectively.

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5. "LM3914 Dot/Bar Display Driver," National Semiconductor, February 2003, http://bit.ly/naDCR

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ZORAN MIJANOVIC has been working as a professor with the electro-technical faculty at the University of Montenegro. He has designed many microcontroller devices for automation and control. He has a PhD in electronics from the University of Belgrade.

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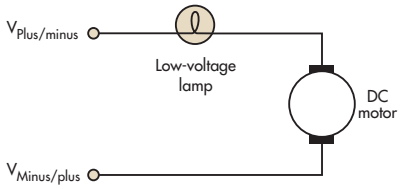
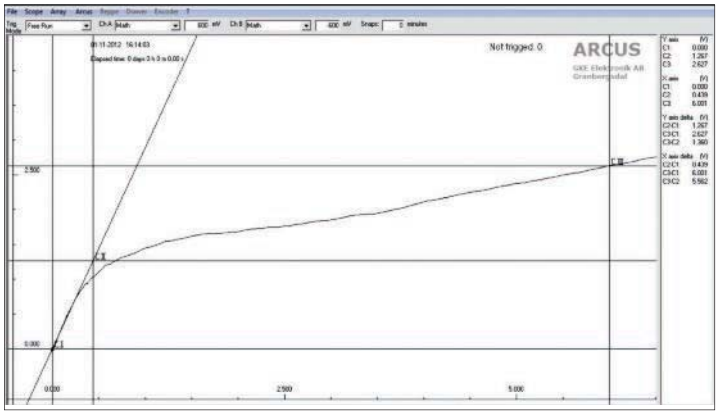
Lamp Eliminates Need For Limit Switches In Flap-Motor Control

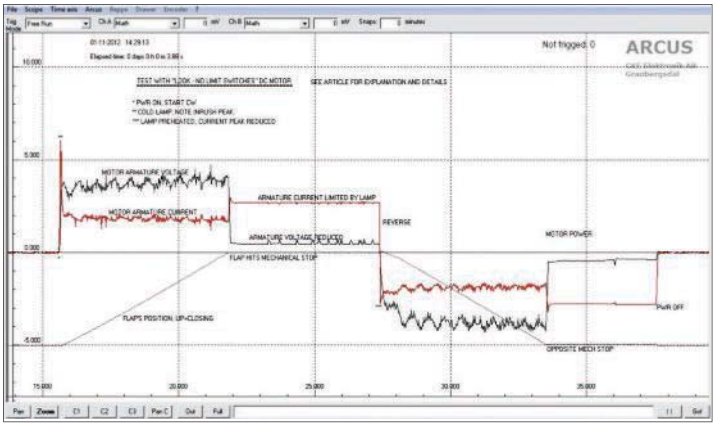
A FRIEND OF a friend asked me how to best open and close a flap at the end of a tube: pneumatics, hydraulics, electrical, or what? It was an automotive application and no hydraulic system or compressor was available. So, the answer seemed obvious: a 12-V dc, small-gear motor.



1. A low-wattage, low-voltage incandescent lamp in the flap's motor-control circuit eliminates the need for limit switches or a microcontroller.



2. The lamp's current-voltage curve (vertical versus horizontal) illustrates the nonlinearity that makes this solution possible.



3. A plot of the circuit's operation shows the smooth, well-defined movement of the flap despite the variations in the motor's current.

The friend said he had tried that already, but he ran into problems with limit switches. The need for a constant closing force at the end of travel was another complication. Adding a microcontroller was too complicated, he said.

There seemed to be no simple answer. But eventually a solution came to me. And all it requires is a low-wattage, low-voltage incandescent lamp added to the motor circuit *(Fig. 1)*.

The relationship between voltage and current in a small incandescent lamp is very nonlinear *(Fig. 2)*. The tungsten wire in the lamp has a low resistance when cold. That's in the region up to around half a volt. Cursors CI and CII indicate that the slope in that region is 0.439/1.267 = 0.35, while the slope between the origin and CIII (nominal voltage and current) is 2.12.

So, the lamp acts as an automatically changing resistor with a low resistance when the load is low and a resistance six times higher when fully loaded. That's exactly what we need to run an actuator without limit switches, microcontroller, transistors, or whatever.

Figure 3 shows flap position, motor voltage, and motor current in a close/rest/open/rest/power-off cycle. The motor current's variations (red trace) reflect a badly aligned coupling and noise in the commutator. That is always present in small dc motors. But the motor used in this application is worse than most other motors in that respect. Despite that, the movement (grey) is smooth and well-defined.

When the flap hits the mechanical stop (flap closed), the motor stops and the back electromagnetic field (EMF) drops to a low value, which means that current would have risen to perhaps five or 10 times the running current, depending on which motor and which supply is chosen. That, of course, would destroy the motor and is why limit switches and controllers are needed to switch off, or reduce, current.

By adding a simple low-wattage and low-voltage incandescent lamp to the circuit, you can avoid this problem and keep the motor current at a low level that the motor can tolerate indefinitely. You can even use the lamp as a visual indicator that the flap has reached its closed (or open) position. And, the reduced current needed to keep the flap tightly closed comes without even asking for it.

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Electronic Design

Ideas for Design

Vol. 2, No. 4

Single-Cell Regulated Charge Pump Draws Low Quiescent Current

A charge pump (or Q pump) uses a flying-capacitor architecture to boost a single cell's voltage to a regulated 2.5V, yet operates at low quiescent current. This approach is a good fit for microcontroller applications where the load is usually in sleep mode and quiescent battery drain is more important than efficiency at higher loads. The two-stage design has efficiency in the 40 to 70% range—comparable to an LDO—yet consumes just microamps when the load is not active.

Hex Buffer, MOSFETs Build A High-Power, Lossless, Virtual Ground

This circuit uses a standard hex inverter to create an oscillator and Class-D amplifier, which in turn drives MOSFETs that can efficiently supply the bipolar rails and sink the ground current.

Graphical, Numerical Techniques Size LED Array's Drive

The nonlinear relationship between forward voltage and current in an LED makes it difficult to properly size the drive current and current-limiting resistor, but useful analysis can be derived from the exponential diode model.

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Single-Cell Regulated Charge Pump Draws Low Quiescent Current

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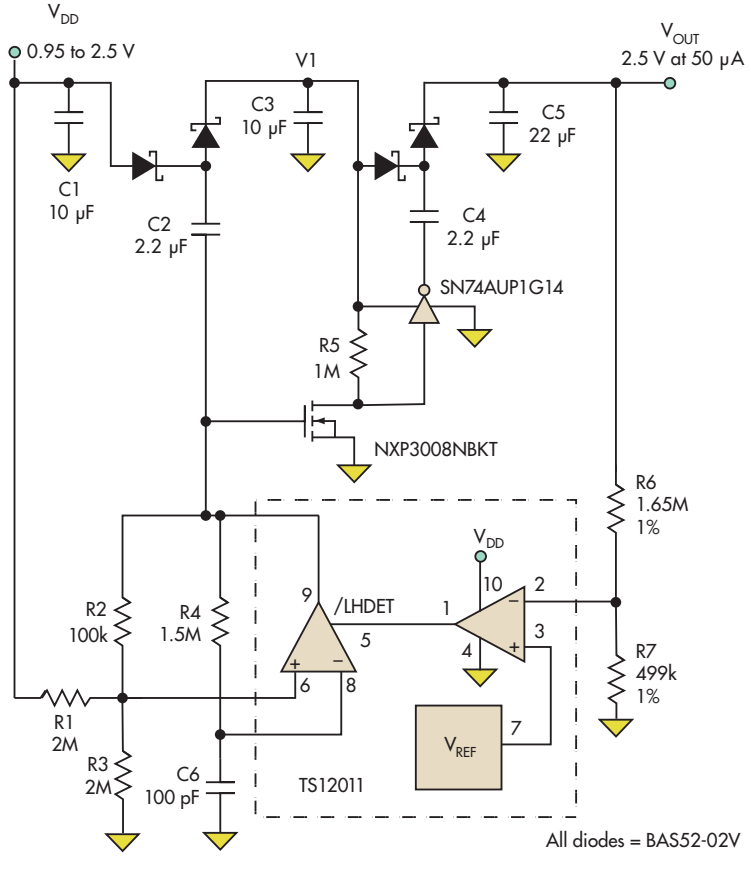
CAPACITOR-BASED CHARGE PUMPS (OR Q-pumps) generally aren't useful for sourcing large amounts of current, but they work well in niche micropower applications where space is at a premium. They work best in applications where the output voltages are integer multiples of the input voltage. The integer multiples, then, are operating points that result in peak efficiency.

However, Q-pumps can also work well when they are powered from a variable input such as a battery, particularly when quiescent battery drain is more important than heavy-load efficiency. This might be the case when powering a microcontroller that spends most of its time in sleep mode.

Low-voltage microcontrollers such as those in the PIC24 or MSP430 families are generally powered from a regulated supply voltage such as 2.5 V. If clocked slowly, they might draw as little as 25 µA or 50 µA. In standby mode with only the real-time clock running, the current can be vanishingly small, often less than a microamp. This is a good application for the regulated two-stage Q-pump described here, which boosts a single alkaline or nickel-metal-hydride (NiMH) cell to 2.5 V.



1. The low-voltage regulated charge pump uses the "flying capacitor" topology (C2 and C4) to "stack" and thus increase the output voltage.

The "wings" of a Q-pump, called "flying capacitors," connect first to the input and then to the output. If the capacitor is stacked on the input voltage, it forms a voltage doubler. In the case of a regulated charge pump with a fixed output voltage, the voltage across the flying capacitor may differ significantly from the voltage across the output-filter capacitor.

When you connect two capacitors that are initially charged to different voltages, you get a spark or power dissipation in the switches as the capacitors equalize in voltage. This is why a simple voltage doubler typically exhibits better efficiency than a regulated Q-pump.

This regulated Q-pump has an on-demand oscillator, a feedback regulation loop made from an op amp and reference, and a two-stage pump circuit, plus two flying capacitors, C2 and C4 *(Fig. 1)*. The first pump stage is driven directly by the Touchstone Semiconductor TS12011 comparator, which forms the oscillator, while the second stage is driven by an inverter powered from the output voltage of the first stage. The full-load efficiency varies from 70% to 40% over a 1- to 2.5-V input range, which is comparable to a linear regulator.

The TS12011 analog building block requires very low supply currents (3.2 µA typical) and

operates well down at the sub-1-V levels needed for single-cell operation. The comparator output stage has good drive-current capability down below 0.8 V V_{DD}, which is an uncommon feature that allows us to drive the first stage directly from the oscillator.

The SN74AUP family of logic gates similarly uses super-low power. The MOSFETs were also carefully chosen for low-voltage operation, with low gate-threshold voltage specifications and low gate-charge characteristics for low switching losses. Using these high-performance components, the no-load quiescent current is a mere 8 µA.

The RC oscillator is stopped when the output is in regulation via its /LHDET latch input *(Fig. 2)*. When the output is above the regulation threshold set by the reference and feedback divider, the op-amp output drives the latch input low, latching the comparator output in the high state and stopping the oscillator.

A large hysteresis band was chosen for the oscillator, resulting in a large signal swing on the timing capacitor C6. This achieves the most efficient size-versus-current operating point for the oscillator. The maximum frequency is nominally set at 1 kHz with the component values shown, but can be adjusted up to about 3 kHz, where it becomes limited by the propagation delay through the comparator.

The amount of charge transferred with each cycle and the switching frequency determine the output current. Accurate calculations for the output impedance or output current from a regulated two-stage pump are complex and need a large spreadsheet, but you can make some oversimplifications to get into the right range. Assuming the capacitor is completely charged and discharged with each cycle (which obviously isn't true), then:

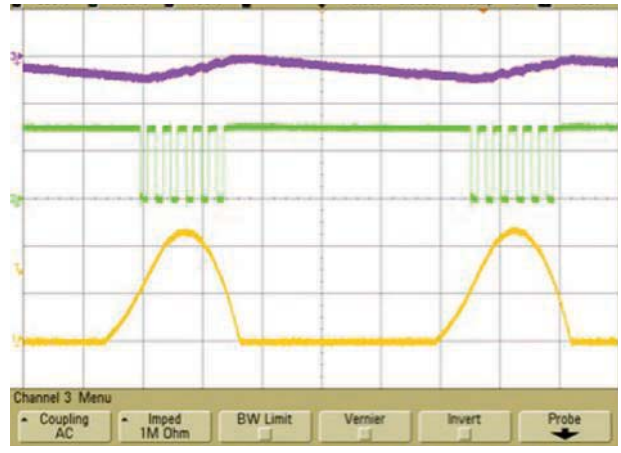
$$Q = C \times V$$
$$I = Q \times f$$

so:

$$I = C \times V \times F$$

where C is the flying capacitor value, V is the applied voltage during the charging phase, F is the oscillator frequency, and I is the output current you'd get if you could remove all the stored charge during the discharge phase (roughly equivalent to a short-circuit load current).

The modified Dickson Multiplier two-stage pump topology used here is a quadrupler, and both stages must be designed to transfer the needed amount of charge at the worst-case low-battery voltage. The first stage is the most important, because the voltage applied to the capacitor is low. Any drop across the first rectifier subtracts from the applied voltage with a resulting loss in headroom, a problem when trying to multiply up to 2.5-V output levels.



2. The oscillator controls how much charge is pumped and thus the output voltage: V_{OUT} (top waveform), comparator output (middle), and op-amp output (bottom).

The rectifier choice is further complicated in this low-quiescent application by leakage currents, which effectively load down the pump and increase idling current. The BAS52-02V Schottky diode has a good combination of low reverse leakage, low forward drop, small packaging, and wide availability.

Reverse leakage current at high temperature is the weakness of Schottky diodes, but lab measurements show that the typical BAS52 is very good on this parameter, at less than 1 µA at 50°C. For even lower reverse leakage, there is the BAS40-02V, but the tradeoff is about 75-mV higher forward-voltage drop.

The capacitor values and switching frequency are chosen to be somewhat excessive for charge transfer, so they don't get in the way of the voltage-drop/headroom issues. As a result, the frequency is low and the capacitors are relatively large, which also keeps switching losses in check. More importantly, a long on-time allows the voltage across the diode to reach a minimum, with the tail end of the forward voltage/current curve being a little less than 0.2 V for the BAS52.

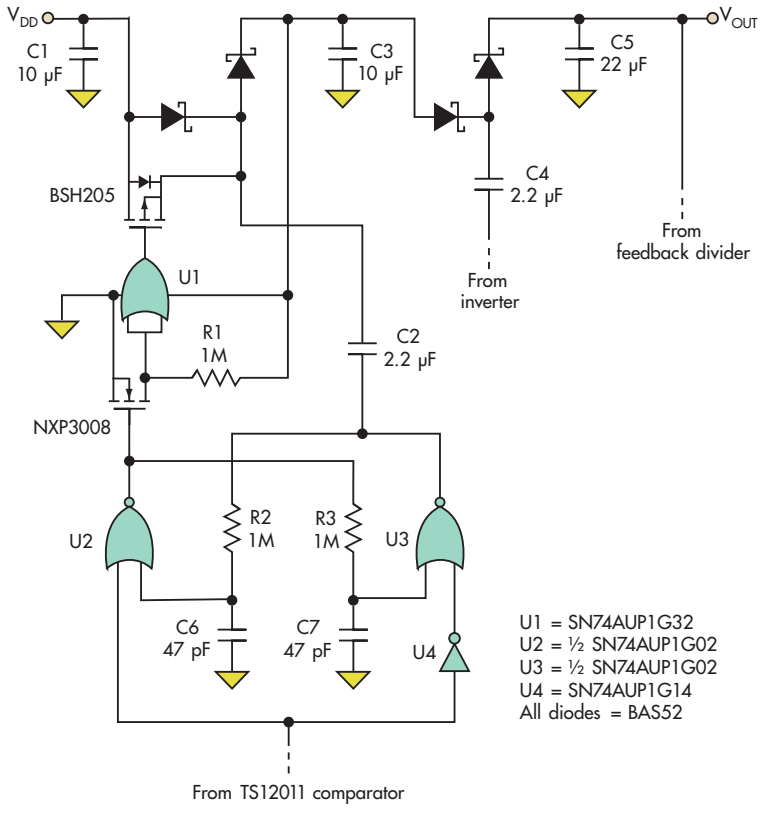
From the simplified charge-transfer equations above, an overly optimistic estimate for first-stage current is:

$$(V_{DD} - V_{FWD} - V_{SAT1}) \times C3 \times F =$$
$$(0.95\ V - 0.2\ V - 0.05\ V) \times 2.2\ \mu F \times 1\ kHz = 1.5\ mA$$

which is more than sufficient to meet a 50-µA load-current requirement. The best-possible peak-output voltage that you can achieve for the intermediate V_1 tap is:

$$2V_{DD} - 2V_{FWD} - V_{SAT1(high)} - V_{SAT1(low)}$$

Similarly, the second-stage peak voltage for V_{OUT} is:



3. To achieve operation below 0.9 V, the first stage is modified by adding a synchronous rectifier across the first diode.

$$2V_1 - 2V_{FWD} - V_{SAT2(high)} - V_{SAT2(low)}$$

Thus, the best-possible peak-load voltage at the minimum input voltage is:

$$V_{OUT} = 4V_{DD} - 4V_{FWD} - 4V_{SAT} =$$
$$(4 \times 0.95\ V) - (4 \times 0.2\ V) - (2 \times 0.05\ V) - (2 \times 0.1\ V) = 2.7\ V$$

where V_{SAT1} and V_{SAT2} are the voltage drops across the comparator and the AUP inverter output stages in the ON state, respectively. Again, this analysis is oversimplified but points out the limits of operation.

This math shows that there is not a lot of room for temperature variation and component tolerances when trying to quadruple the lower end of the voltage range of a single cell. We can improve this, and get to sub-0.9 V operation, by several means: adding another pump stage; changing the output voltage to 2.2 V (but the microcontroller may not be able operate this low); or adding a synchronous rectifier across the first diode.

The third option is chosen here, due to its good efficiency at the operating "sweet spots" *(Fig. 3)*. A low-threshold P-channel MOSFET with low gate charge shunts the first pump diode, reducing the forward drop from 0.2 V to approximately 0.01 V. This adds a few hundred extra millivolts right at the front end, where it's needed most.

A NOR-based logic circuit provides nonoverlapping gate-drive signals to the synchronous switch. The goal is to be certain that the MOSFET gate is never driven high when the flying capacitor is high. The amount of dead time is set by the 1 MΩ × 47 pF RC time constants. Here, the dead time is very long since the 1-kHz oscillator is so slow.

Charge pumps offer an alternative to inductor-based boost regulators and can fit nicely with the dual nature of many microcontroller loads, with their low-current RTC mode versus heavier but infrequent run mode. The challenge of designing them for low input voltages can be met by using the right low-voltage components, choosing sensible switching frequencies, and taking full advantage of the V-I characteristics of the rectifiers.

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Hex Buffer, MOSFETs Build A High-Power, Lossless, Virtual Ground

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A VIRTUAL GROUND IS useful whenever you need to create a bipolar supply but the dc source is unipolar, as is often the case with battery-operated equipment. Sometimes, the solution is as easy as using a high-ohm resistive divider to provide a mid-supply potential. But if the ground impedance needs to be lower, the simple approach can be enhanced by using a buffer amplifier.

When the ground created this way sees high imbalance currents, though, things become more complicated. The buffer not only needs to be a power buffer, it will also have to dissipate the result of any imbalance. This is wasteful, and it may even require bulky, inconvenient heatsinks.

This circuit addresses these issues simply, cheaply, and effectively *(see the figure)*. It retains the resistive divider plus buffer configuration, but with a big difference. The buffer is now a self-oscillating Class D amplifier, capable of providing many amperes of ground current and of "recycling" any imbalance back to the supply. The circuit is compact and efficient, while providing a stiff, accurate, and powerful ground.

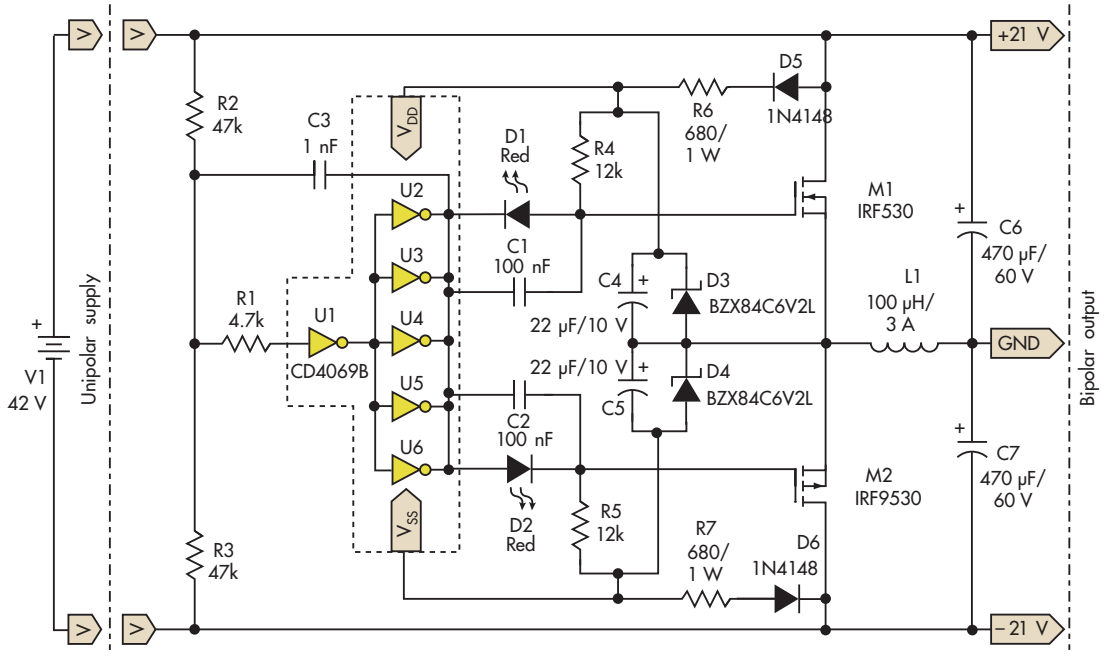
The oscillator is built around a simple CD4069 CMOS hex buffer. Most of its inverters act as gate drivers for the power MOSFETs. Inverter U1 provides the non-inverting input of the amplifier, as the inverting input is implicit and is represented by the CD4069's mid-supply potential. Capacitor C3 provides positive feedback and allows the circuit to self-oscillate.

The entire control circuit has a floating supply referenced to the output. Diodes D3 to D6 and resistor pair R6/R7 generate this supply from the dc input. R2 and R3 create the virtual ground potential. In this example, they are equal, as will generally be the case, but asymmetrical supplies also can be created.

For greater accuracy, a trim potentiometer can be added to the midpoint of R2/R3. With the values shown, the pulse-width modulation (PWM) frequency is approximately 45 kHz, which can be modified by changing C3.

The power MOSFETs and inductor must be sized according to the expected output current. If a very clean ground is required, an additional LC filter can be used after L1 and C6/C7 to clean up the remaining switching residues.

LOUIS VLEMINCQ works as a design engineer in Physcial Layer Engineering at Belgacom, Evere, Belgium.



Although it requires more components than the conventional resistor-divider approach, this Class D oscillator/amplifier (based on a CD4069 hex inverter) drives power MOSFETs that make the virtual ground much more efficient.

ideas for design

Graphical, Numerical Techniques Size LED Array's Drive

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LED-BASED LIGHTING IS REPLACING incandescent and gas-discharge lamps in many situations. As practical lighting sources, and considering their directional nature, LED fixtures usually use multiple LEDs arranged in an array, with "m" LEDs in a serial string and "n" such strings in parallel *(Fig. 1)*. For the array configuration and the exponential I-V characteristics model of a single LED,[1] it's additionally possible to have a similar model representing the loading of such an array.

Since the single LED is a diode with a nonlinear forward-voltage/current, driving it with a fixed voltage source is generally not recommended. Rather, a serial (current-limiting) resistor is needed to equalize the power source and the load *(Fig. 2)*. However, sizing this resistor requires a significant analytical manipulation. Using the single-LED exponential model, a Kirchoff's voltage law (KVL) equation around the circuit loop gives:

$$R_x\left(ae^{bV_F}+c\right)+V_F=V_s \quad (1)$$

which can be rearranged to:

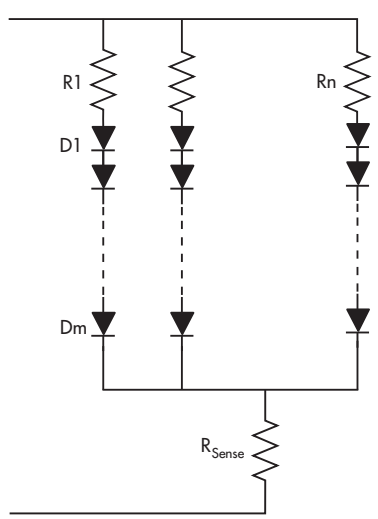
$$R_x=\frac{V_s-V_F}{ae^{bV_F}+c} \quad (2)$$

where a, b, and c are model parameters for a selected LED, as defined in the reference.

This is a challenge to solve symbolically, but it can be solved numerically with mathematical software tools. Alternatively, it can be solved graphically by separating the two key I-V relationship equations, $v+R_xI_F=V_s$ and $I_F=ae^{bv}+c$.

For example, using a Lumileds Luxeon Rebel ES LED with a 3.2-V dc source and a desired drive current of 0.5 A, the horizontal current line intercepts the LED curve at 2.92 V *(Fig. 3)*. Therefore, the series resistor will be $R_x = (3.2 - 2.92)/0.5 = 0.56\ \Omega$.

However, the graphical approach would not handle an LED array effectively, and the numerical method works better. To represent the array current i_A, the exponential model for the (m × n) array is modified, since voltage drops across current-limiting resistor R_n and sense-resistor R_{Sense} are usually small compared with driving-source V_s:



1. Establishing the correct resistor size for each string of an array of n strings, where each strings has m LEDs, is challenging due to the nonlinear nature of the diodes.

$$i_A=n\left(ae^{b\frac{V_s}{m}}+c\right) \quad (3)$$

With the array model, the switch-mode buck-regulating current driver in a closed-loop configuration *(Fig. 4)* can be described by a set of equations starting at the feedback point, circling around the control loop, and ending at the driver output:

- Current sensing:

$$V_f=i_A\bullet R_{Sense} \quad (4)$$

- Error amplifier:

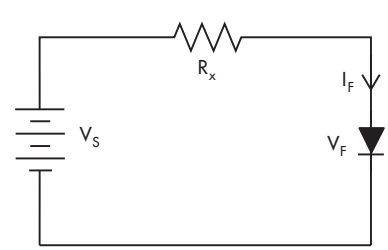
$$V_{er}=A(V_{Ref}-V_f) \quad (5)$$

- Effective error:

$$V_{ef}=\frac{V_{er}-V_F}{R_d}\bullet CTR\bullet R_e \quad (6)$$

- PWM ramp:

$$V_{Ramp}(t)=V_{Min}+\frac{V_{Max}-V_{Min}}{0.95\bullet T_s}t \quad (7)$$



2. Even for a single LED driven by a voltage source, the exponential current-voltage relationship complicates selection of the series-resistor value.

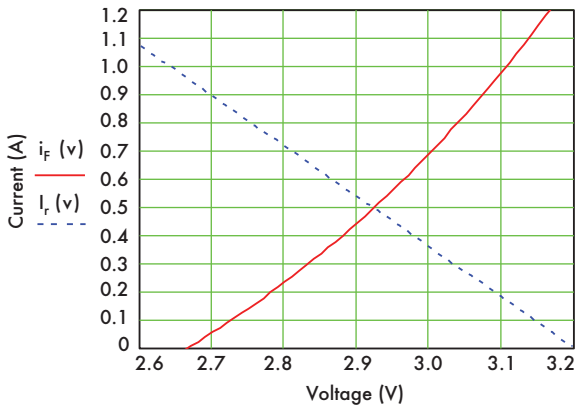
• Duty cycle, D:

$$V_{Ramp}(D \bullet T_s) = V_{ef} \quad (8)$$

• Power stage:

$$\frac{V_{In}}{N_p} \bullet N_s \bullet D = V_s \quad (9)$$

With effort, all the equations can be consolidated into a single, closed-loop equation. Equation 10 is a transcendental equation with an exponential term that prevents us from solving it analytically, but it can be solved using computational techniques and software tools.



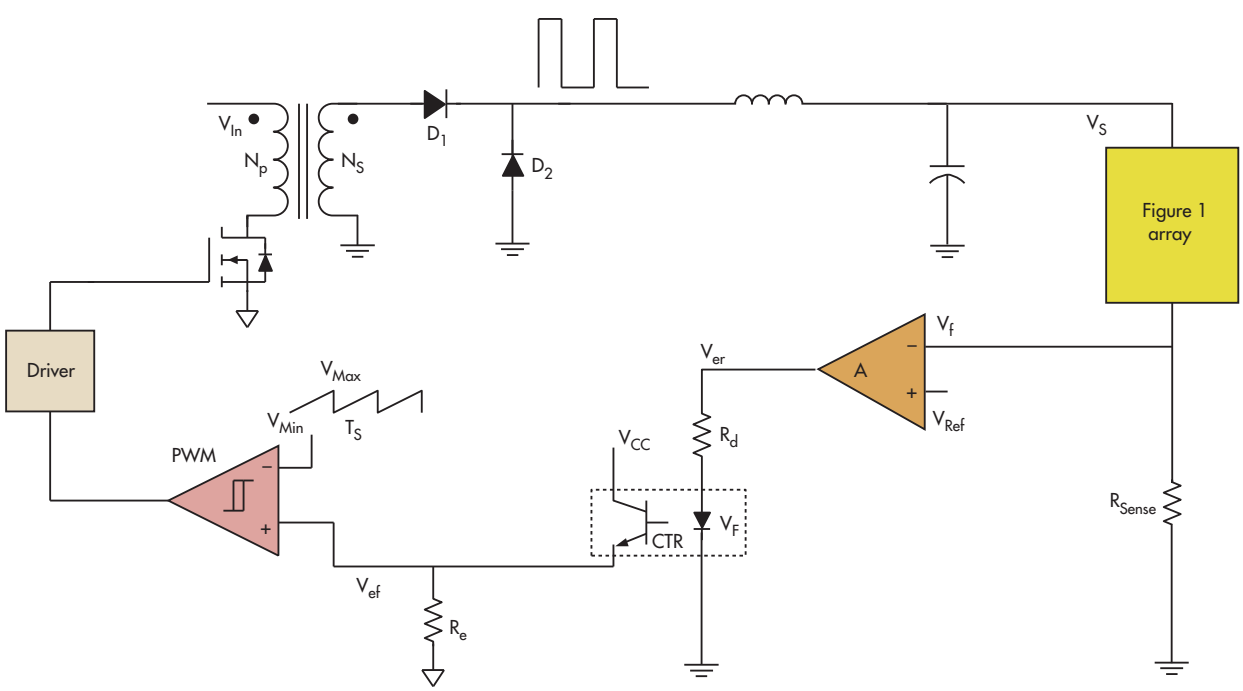
3. The intersection of the desired current line and the forward current/voltage curve (red) leads to the unique solution to the nonlinear equations of the LED model. (The blue line is the reverse-bias current/voltage relationship.)

Reference

1. "Generate Realistic Models for LED Current Versus Voltage," Keng C. Wu; Electronic Design, Vol. 61, No. 1, p. 52, Jan. 10, 2013, http://electronicdesign.com/power/generate-realistic-models-led-current-versus-voltage

$$\frac{V_{In}}{N_p} \bullet N_s \bullet \frac{0.95\left(\frac{A\left(V_{Ref} - n\left(ae^{b\frac{V_s}{m}} C\right) \bullet R_{Sense}\right) - V_F}{R_d} \bullet CTR \bullet R_e - V_{Min}\right)}{V_{Max} - V_{Min}} = V_s \quad (10)$$

KENG C. WU has a BS from Chiaotung University, Taiwan, and an MS from Northwestern University, Evanston, Ill. He has published four books and holds seven U.S. patents.



4. Analysis of the switch-mode buck-regulating current driver in a closed-loop configuration for driving an array yields a set of equations that are better solved using numerical computation rather than an analytical, closed-form approach.

Electronic Design

Ideas for Design

Vol. 2, No. 5

Simple Addition Permits Voltage Control Of DC-DC Converter's Output

This article presents apples-to-apples test results for noise densities for several low-noise discrete, SMT n-JFETs. The tests used the same operating conditions so that designers can make a fair comparison for their applications.

Simple NiCd Battery Charger Includes Charge Indication

This circuit uses a microcontroller and simple algorithm managing voltage regulator ICs and discrete components to control charging of nickel-cadmium batteries. It provides a steady charging current matched to the battery capacity while avoiding overcharging; it also includes LEDs that indicate the status of the charging process to the user.

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ideas for design

Simple Addition Permits Voltage Control Of DC-DC Converter's Output

EUGENE PALATNIK | ITEC ENGINEERING epalatn@itecengineering.com

IN A STANDARD DC-DC converter, a resistor divider typically defines a fixed output voltage. However, applications like programmable output voltage power supplies and motor control circuits require dynamic control of the dc-dc converter's output voltage. The circuit described here allows control of the converter's output voltage, V_{Out}, with a control voltage, V_C.

In a conventional dc-dc buck converter, V_{Out} is:

$$V_{Out} = V_{fb}\left(\frac{R1 \quad R2}{R2}\right) \quad (1)$$

so V_{Out} is fixed by the values of R1 and R2 *(Fig. 1)*.

The added circuitry in Figure 2 enables users to control the same dc-dc converter's output voltage using V_C. In this case, R2 is not connected to the ground but, rather, to V_r. Equation 1 then becomes:

$$V_{Out} - V_r = \left(V_{fb} - V_r\right)\left(\frac{R1 \quad R2}{R2}\right) \quad (2)$$

Since R1 = 20 kΩ and R2 = 10 kΩ, Equation 2 can be simplified to:

$$V_{Out} - V_r = 3(V_{fb} - V_r) \quad (3)$$

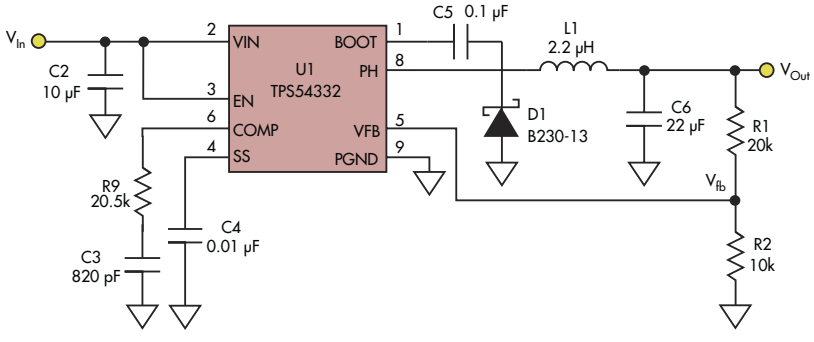
or:

$$V_{Out} = 3\,V_{fb} - 2\,V_r \quad (4)$$

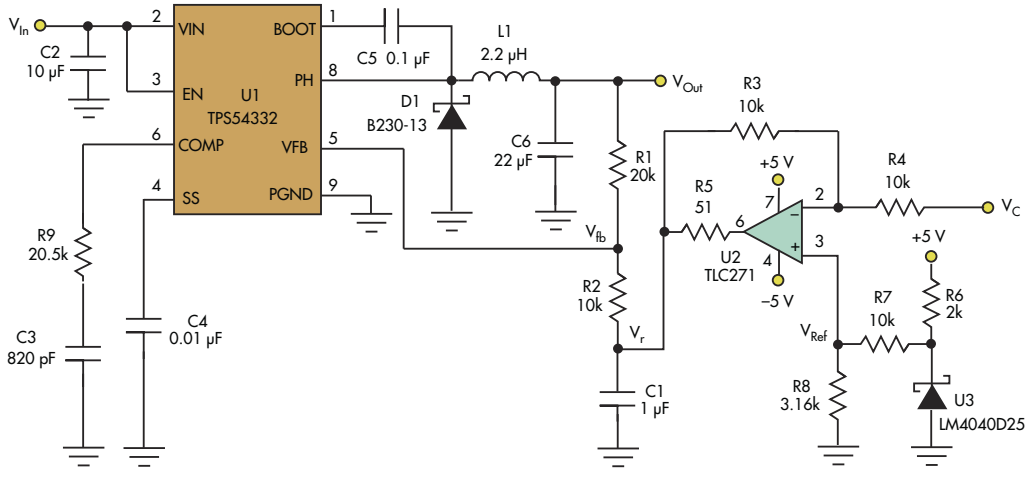
R3 and R4 have the same value, 10 kΩ, so amplifier U2's output voltage is:

$$V_r = 2\,V_{Ref} - V_C \quad (5)$$

where V_{Ref} is the reference voltage generated by U3 after resistor divider R7/R8.



1. The output voltage in a conventional dc-dc buck converter is fixed and depends on the resistor divider, R1/R2.



2. The added circuitry in this version of the dc-dc converter permits control of V_{Out} by varying a control voltage, V_C.

Combining Equation 4 and Equation 5:

$$V_{Out} = 3\,V_{fb} - 4\,V_{Ref} + 2\,V \quad (6)$$

To simplify Equation 6, choose components that make:

$$3\,V_{fb} = 4\,V_{Ref} \quad (7)$$

Then Equation 6 becomes:

$$V_{Out} = 2\,V_C \quad (8)$$

The internal voltage reference of U1 is 0.8 V. By choosing R7 = 10 kΩ and R8 = 3.16 kΩ, V_{Ref} = 0.6 V, satisfying Equation 7. Finally, C1 lowers U2's output impedance at high frequencies, maintaining the stability of U1's feedback loop.

The added circuitry allows users to control the buck converter's output voltage, V_{Out}, in the range of 0 to 5 V with a control voltage, V_C, in the range of 0 to 2.5 V. Similar circuitry can be designed for use with a boost converter, or any other dc-dc converter, as long as its feedback voltage pin is accessible.

EUGENE PALATNIK is an electrical engineer and president of ITEC Engineering LLC. He is active in the design of electronics for medical, scientific, and industrial applications.

Simple NiCd Battery Charger Includes Charge Indication

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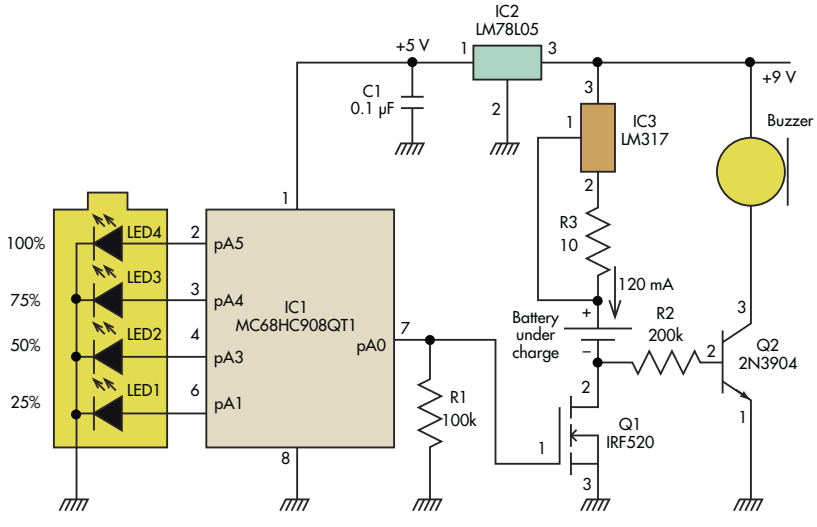
RECHARGEABLE NICKEL-CADMIUM (NICD) BATTERIES are widely used in consumer electronics because of their high energy density, long life, and low self-discharge rate. Standard NiCd cells can be charged at different rates: a fast charge with high current, or overnight with low current.

Regardless of the charge speed, a steady current should be provided to the battery during charging. Also, more energy must be supplied to the battery than its actual capacity to compensate for energy loss during charging.

However, two problems must be addressed when designing a charger for them: how to set the proper charging-current value, and how to stop the charging process when the battery is full, to avoid overcharging. This simple and inexpensive charger overcomes both problems. The cheapest and safest way to charge a NiCd battery is to charge at 10% of its rated capacity per hour for 16 hours. The battery pack used contained two AA-size 1200-mAh NiCd cells, so the battery should be charged with 120-mA current.



1. The constant charging current is produced by an LDO and resistor and gated by Q1, which in turn is managed by an output of the microcontroller. A quartet of LEDs, also microcontroller-driven, indicates charge status to the user.

In the charging circuit of Figure 1, a constant charge current is generated by a current regulator comprising IC3 (an LM317 LDO) and resistor R3, where R3 is 1.25 V/120 mA, about 10 Ω. Switching MOSFET Q1 (IRF520) was chosen because of its very low open-state (conductive) impedance of 0.3 Ω.

The best charging practice is to use a timer to prevent overcharging to continue past 16 hours. This approach does not require an end-of-charge sensor, and it ensures a full charge. The timing function is performed by microcontroller IC1, which also reports the state of charge via the LEDs.

Any microcontroller could be used in this project. Here, the inexpensive eight-pin Motorola (Freescale) MC68HC908QT1 microcontroller was used.

Each charging step is indicated by lighting a corresponding LED. The number of steps is determined by the number of available outputs of the microcontroller, without adding any extra components. Since the microcontroller has five outputs, one of them is used for charge triggering, and so the four can be used for charge indication. To minimize the number of components, LEDs with built-in resistors are used (WP710A10YD5V, *www.kingbrightusa.com*).

To make the process more visual, these LEDs should be located in line with the outline of the battery drawn around them, so lighting the LEDs one by one will clearly indicate the progress of charging. It is reasonable to choose the time intervals to be equal, with the LEDs indicating 25%, 50%, 75%, and 100% of battery-charge time.

The program starts blinking the corresponding LED at the beginning of each time interval and up to the end of each interval. After that, it lights the LEDs steady on. When charging is over, all four LEDs are on, so the user knows the charge status at any time. (As an optional feature, a buzzer could be added to provide an audio signal when charging is over.)

The microcontroller program of Figure 2 is straightforward. The assembler code listing can be found with the online version of this article at *http://electronicdesign.com/power/simple-nicd-battery-charger-includes-charge-indication*.

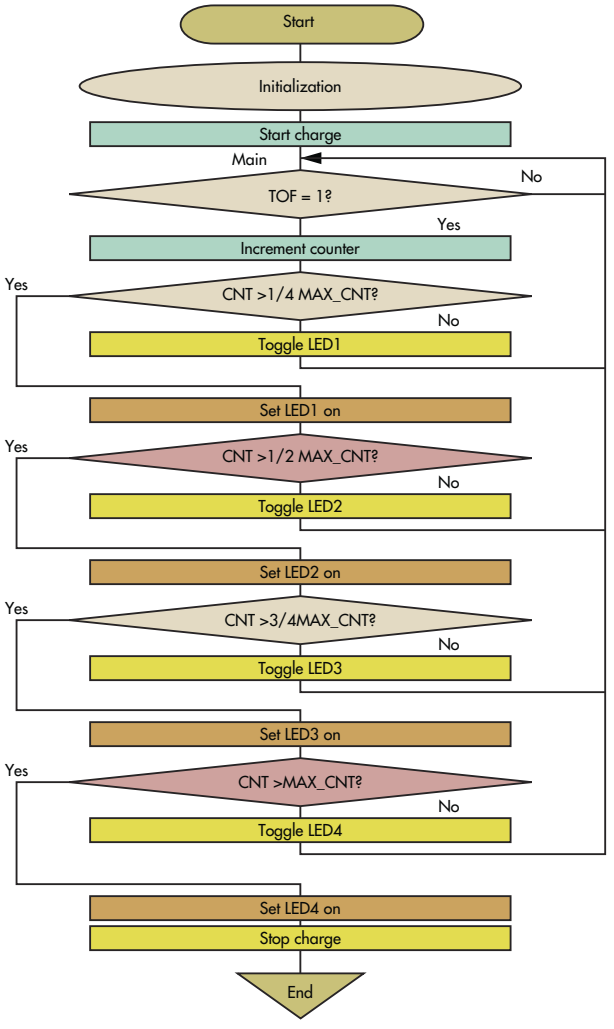
The LED blinking period is set at one second. The built-in oscillator of the microcontroller generates a frequency of 12.8 MHz and provides a one-cycle duration of 312.5 ns. By setting the timer prescaler to 64 and timer modulo register to 50,000 (C350H), the timer overflow (TOF) period is equal to one second (0.3125 μs × 64 × 50,000). The program toggles the LED at each TOF period.

The overnight "long" charge lasts 16 hours, with counter constant MAX_CNT calculated as 16 × 60 × 60 = 57,600 (E100H). Any maximum charge time can be set in the same way. Obviously, it's not convenient to wait for 16 hours to test the program, and a period such as 20 minutes, for example, would be more practical.

For that shorter period, constant MAX_CNT should be set to 20 × 60 = 1200 (04B0H). The duration of each of four time intervals will then be automatically set by firmware once the maximum charge time is entered.

This approach is very flexible and can be applied to charge any NiCd battery by choosing resistor R3 accordingly. In addition, nearly any type of microcontroller can be used, because the program is simple and uses only standard instructions.

ABEL RAYNUS is an engineer with Armatron International Inc., Malden, Mass.



2. The flowchart shows the straightforward level-check/step-through iteration sequence of the code for driving the charge-indication LEDs.

Electronic Design

Ideas for Design

Vol. 2, No.6

Circuit Generates High-Frequency Sine/Cosine Waves From Square-Wave Input

Direct digital synthesis ICs can convert square waves to sine/cosine waves but their complexity is a disadvantage. This circuit uses simple CMOS logic and two switched-capacitor filters to perform the conversion.

Determine Equivalent ESR, Ripple Voltage, And Currents For Unequal Capacitors In Parallel

Capacitors are used in parallel to provide special performance attributes; however, it's difficult to determine critical performance specifics of ESR, high-frequency ripple voltage, and individual RMS currents when they have unequal values. This numerical approach provides a straightforward solution to calculating the values based on published specifications.

Graphically Determine The Output Signal Level Of An RC Filter

The need to know what the output filter's value will be is especially important for variable switching power supplies operating at different duty cycles. This discussion provides a method for calculating that output.

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ideas for design

Circuit Generates High-Frequency Sine/Cosine Waves From Square-Wave Input

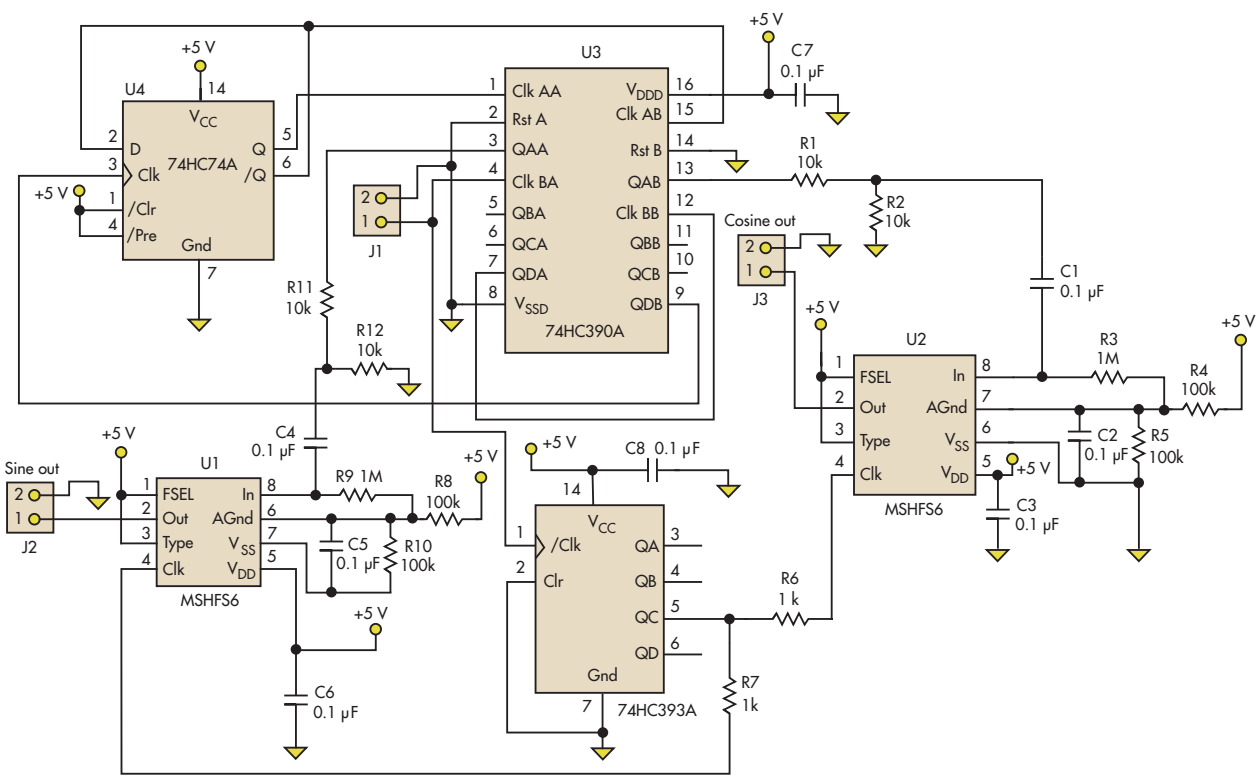
JOHN R. AMBROSE | MIXED SIGNAL INTEGRATION CORP. john@mix-sig.com

ALTHOUGH QUITE A FEW direct digital synthesis (DDS) ICs can generate high-frequency sine waves, their complexity excludes them from many designs. However, designers can use simple high-frequency CMOS logic and two switched-capacitor filters to create a sine/cosine generator. With newer filters, a 1-MHz output at 1.7 V p-p is possible.

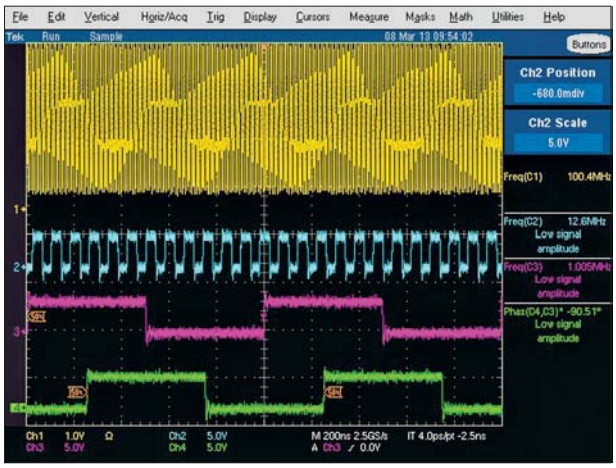
The example circuit uses an MSHFS6 5-V, low-power 12.5:1 switched-capacitor filter with selectable Butterworth, Bessel, or elliptic filters in the lowpass mode and full-, 1/3-, or 1/6-octave filters in the bandpass mode. Since the lowpass mode would cause a 3-dB loss of the signal output, the circuit uses the 1/6-octave bandpass filter, which is selected by tying pins 1 and 3 high on the MSHFS6 *(Fig. 1)*.

Two separate divider circuits are used. The 74HC393A divides the 50-MHz clock to 12.5 MHz. The 74HC390A is a dual divide-by-2 and divide-by-5 device. By combining the 74HC390 with the 74HC74A dual flip-flop, the 50-MHz clock can be divided to 500 kHz.

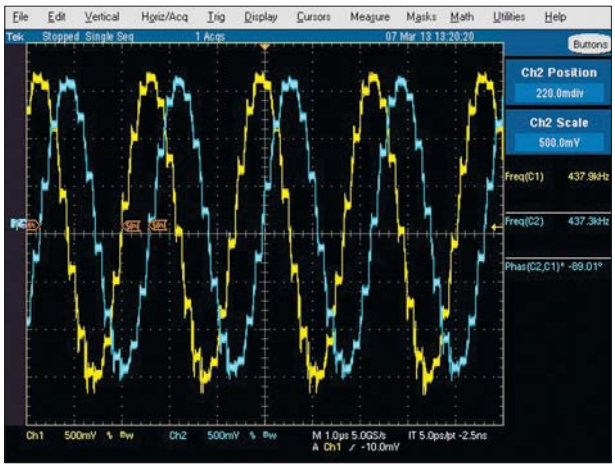
The 74HC74A provides a Q and /Q output at half the frequency of the divide-by-25 output of the 74HC390A. Dividing the 74HC74A output by 2 with the divide-by-2 blocks in the 74HC390A creates two square waves –90° apart. Figure 2 shows a 100-MHz square-wave input, a 12.5-MHz output for the filter clock, and 1-MHz sine and –cosine square-wave output before the dividers. Resistor-divider circuits reduce the amplitude from rail to rail to prevent generation of distor-



1. Instead of a DDS IC, the sine/cosine generator uses simple CMOS logic and two switched-capacitor filters to provide a 1-MHz output at 3.0 V dc.



2. The 1-MHz sine and –cosine outputs of the generator (channels 3 and 4) result from the 100-MHz square-wave input (channel 1).



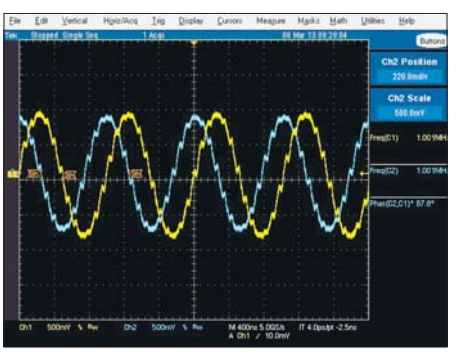
3. Channels 1 and 2 show the outputs of the two switched-filter capacitors with an input clock of nearly 50 MHz.

tion in the filters. The use of ac coupling at the MSHFS6 filter inputs ensures smoothed square waves centered around the filters' analog ground.

Figure 3 shows the output of the two filters with an input clock of nearly 50 MHz. If the inverted cosine is not acceptable, an op amp at the cosine filter output or the inverter at pin 13 of the 74HC390A can correct it.

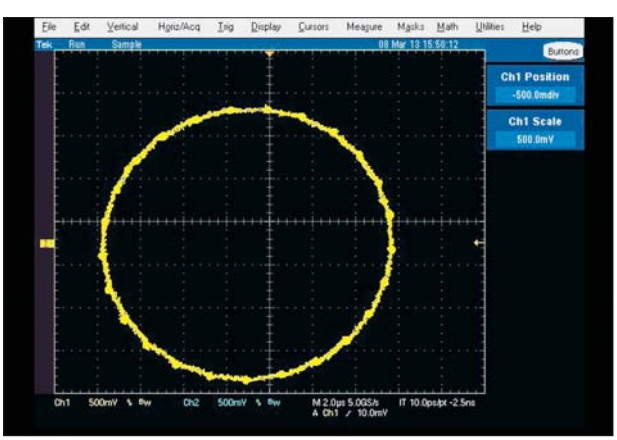
The Lissajous curve for the two outputs *(Fig. 4)* indicates that the phase circle matches the 89.1° reading in Figure 3. Using a Krohn-Hite 6900B distortion analyzer and a 1-MHz Krohn Hite lowpass filter (to remove the clock), the circuit's total harmonic distortion on the sine output was only 0.1%. Although the 74HC390A and 74HC393A have a guaranteed maximum operating frequency of 50 MHz at 6 V, Mixed Signal Integration Corp. and other companies have found that spec to be very conservative.

In this application, a 100-MHz input clock achieved the desired divide-by-4 and divide-by-100 needed to operate the newer MSVHFS6 switched-capacitor filter at 3.3 V. The only change needed was to reduce V_{DD} to 3.3 V and replace the 5-V MSHFS6 filters with the 3.3-V MSVHFS6. The input clock was increased to 100 MHz. Figures 5 and 6 show the filter outputs' phase relationship in time and as a Lissajous curve.



5. The original circuit used the MSHFS6 switched capacitor, but it also works with the newer MSVHFS6 version, which runs on 3.3 V rather than 5.0 V. This screen shows the two outputs' phase relationship in time.

JOHN R. AMRBOSE is the vice president of applications and system engineering at Mixed Signal Integration Corp.



4. The Lissajous curve for the circuit's two outputs shows that the phase circle matches the 89.1° found in Figure 3.

6. The Lissajous curve for the circuit using the MSVHFS6 3.3-V filters shows the outputs' phase relationship.

Determine Equivalent ESR, Ripple Voltage, And Currents For Unequal Capacitors In Parallel

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CAPACITORS OFTEN ARE CONNECTED in parallel in power electronics to decrease high-frequency ripples, current stress, power dissipation, and operating temperature, as well as to shape frequency response and boost reliability. Yet designers have three critical questions about this technique:

- What are the equivalent values of capacitance C_{se} and equivalent series resistance (ESR) R_{se}?
- What is the high-frequency ripple voltage?
- What are the individual RMS currents?

If all N capacitors in the parallel connection are identical *(Fig. 1)*, with equal capacitance values $C_{sk} = C$ and equal ESR values $R_{sk} = R_s$, then for k = 1, 2, . . . N the answers are clear:

- C_{se} is directly proportional to the number of capacitors N: $C_{se} = NC$, and R_{se} is inversely proportional to N: $R_{se} = R_s/N$.
- Ripple voltage V (RMS value) is:

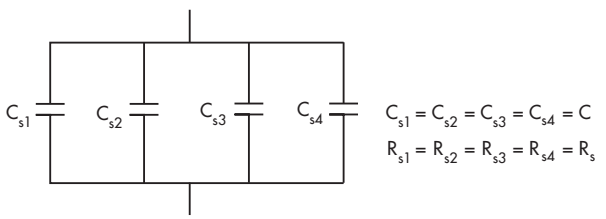
$$V = I\sqrt{R_{se}^2 + X_{se}^2} \qquad (1)$$

for a sinusoidal current excitation $i(t) = I\sqrt{2}\sin(2\pi ft)$ with frequency f, where $X_{se} = 1/(2\pi fC_{se})$ is the reactance of the equivalent capacitor C_{se} and RMS value I, and individual RMS currents in the capacitors are identical: $I_k = I/N$.

When the capacitors in the parallel connection aren't identical, with different capacitance C_{sk} and ESR R_{sk} values, the solution to the problem isn't trivial. The direct approach is to obtain an analytical expression for the input impedance of the parallel connection in the algebraic form $Z = \mathrm{Re}\,Z - j\,\mathrm{Im}Z = Z_{se}\,Z$ and use the formulas $R_{se} = \mathrm{Re}\,Z$, $X_{se} = \mathrm{Im}\,Z$, and $C_{se} = 1/(2\pi f X_{se})$.

A less complicated approach is based on the conversion of series C_{sk}, R_{sk} connections to equivalent parallel C_{pk}, R_{pk} connections. To obtain relationships between R_{pk} and R_{sk}, and also between C_{pk} and C_{sk}, set the admittance Y_{pk} of the parallel C_{pk}, R_{pk} pair and admittance Y_{sk} of the series C_{sk}, R_{sk} pair connections equal to each other: $Y_{pk} = Y_{sk}$, $\mathrm{Re}\,(Y_{pk}) = \mathrm{Re}\,(Y_{sk})$, and $\mathrm{Im}\,(Y_{pk}) = \mathrm{Im}\,(Y_{sk})$. Then:

$$C_{pk} = \frac{C_{sk}}{1 + \left(\frac{R_{sk}}{X_{sk}}\right)^2} \qquad (2)$$



1. For an array of N identical capacitors in parallel, determining the total equivalent capacitance and ESR values is straightforward. For unequal capacitors, the calculation can be difficult.

$$R_{pk} = \frac{R_{sk}^2 + X_{sk}^2}{R_{sk}} \qquad (3)$$

where:

$$X_{sk} = \frac{1}{2\pi fC_{sk}} \qquad (4)$$

is the reactance of the individual capacitor.

After individual parallel capacitances C_{pk} and resistances R_{pk} are calculated according to Equations 2 and 3, equivalent parallel capacitance C_{pe} can be easily found as the sum of C_{pk}:

$$C_{pe} = \sum_{k=1}^{N} C_{pk} \qquad (5)$$

The real part of equivalent admittance can be found as the sum of admittances $1/R_{pk}$. R_{pe} can be obtained as a reverse value of that sum:

$$R_{pe} = \frac{1}{\sum_{k=1}^{N} \frac{1}{R_{pk}}} \qquad (6)$$

The system's equivalent series capacitance C_{se} and ESR R_{se} can be found by conversion of the parallel C_{pe}, R_{pe} connection to the equivalent series connection C_{se}, R_{se}. To obtain relationships between C_{se} and C_{pe} and also between R_{se} and R_{pe}, set impedance Z_{pe} of the parallel C_{pe}, R_{pe} and impedance Z_{se} of the series C_{se}, R_{se} connections equal to each other: $Z_{pe} = Z_{se}$, $\mathrm{Re}\,Z_{pe} = \mathrm{Re}\,Z_{se}$, $\mathrm{Im}\,Z_{pe} = \mathrm{Im}\,Z_{se}$. Then:

$$C_{se} = C_{pe}\left[1 + \left(\frac{X_{pe}}{R_{pe}}\right)^2\right] \qquad (7)$$

$$R_{se} = \frac{R_{pe}}{\left[1 + \left(\frac{R_{pe}}{X_{pe}}\right)^2\right]} \qquad (8)$$

where:

$$X_{pe} = \frac{1}{2\pi f C_{pe}} \qquad (9)$$

is the reactance of the equivalent parallel capacitor C_{pe} *(Equation 5)*.

Based on this analysis, the calculation procedure for equivalent series capacitance C_{se}, ESR R_{se}, voltage ripples V, and RMS currents I_k in the capacitors is:

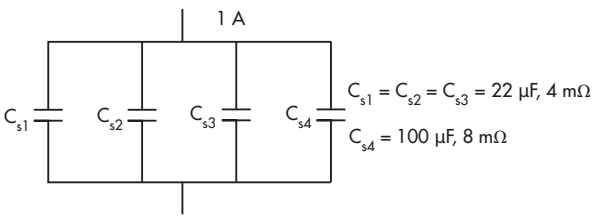
- Calculate reactances of individual capacitances according to Equation 4.
- Determine equivalent parallel parameters C_{pk}, R_{pk} of the capacitors based on Equations 2 and 3.
- Calculate equivalent parallel capacitance C_{pe} of the structure, its reactance X_{pe}, and equivalent parallel resistance R_{pe} according to Equations 5, 9, and 6.
- Calculate equivalent series capacitance C_{se} and ESR R_{se} of the structure according to Equations 7 and 8.
- Obtain RMS ripple voltage V using Equation 1.
- Calculate RMS currents I_k in the capacitors based on:

$$I_k = \frac{V}{\sqrt{R_{sk}^2 + X_{sk}^2}} \qquad (10)$$

Note that ESR values R_{sk} are strong functions of frequency. A designer should use ESR data specified by capacitor manufacturers at a given frequency of operation, such as the data for ceramic and polymer aluminum electrolytic capacitors from Murata Manufacturing Co. Ltd. (MMC) *(http://ds.murata.co.jp/software/simsurfing/en-us/index.html)*.

To illustrate the calculation procedure, let's determine equivalent parameters, voltage ripple, and current distribution for a parallel connection of three ceramic capacitors (GRM-21BR60J226ME39L) and one polymer capacitor (ESASD-40J107M015K00) from MMC *(Fig. 2)*. Using the data f = 200 kHz, $C_{s1} = C_{s2} = C_{s3} = 22$ µF, $R_{s1} = R_{s2} = R_{s3} = 4$ mΩ, $C_{s4} = 100$ µF, $R_{s4} = 8$ mΩ, I = 2 A, then:

- For reactance of each individual capacitance according to Equation 4, we have $X_{si} = X_{s2} = X_{s3} = 3.6$ mΩ, $X_{s4} = 0.8$ mΩ.
- Equivalent parallel parameters C_{pk}, R_{pk} of the capacitors based on Equations 2 and 3 are $C_{p1} = C_{p2} = C_{p3} = 21.7$ µF, $R_{p1} = R_{p2} = R_{p3} = 331$ mΩ, $C_{p4} = 49.7$ µF, $R_{p4} = 16$ mΩ.



2. This example of four capacitors, with three identical and one different, illustrates how the computation scheme works in practice.

- For equivalent parallel capacitance C_{pe}, its reactance X_{pe} and equivalent parallel resistance R_{pe} of the structure according to Equations 5, 9, and 6, we calculate $C_{pe} = 115$ µF, $X_{pe} = 6.9$ mΩ, $R_{pe} = 13.9$ mΩ.
- According to Equations 7 and 8, the equivalent series capacitance C_{se} and ESR R_{se} are $C_{se} = 143.4$ µF, $R_{se} = 2.76$ mΩ.
- For RMS ripple voltage V based on Equation 1, we obtain V = 12.4 mV.
- RMS currents according to Equation 10 in ceramic and polymer capacitors are respectively: $I_1 = I_2 = I_3 = 341$ mA, $I_4 = 1.1$ A.

This shows the technique can easily determine the parameter values in each of the capacitors.

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Graphically Determine The Output Signal Level Of An RC Filter

GREGORY MIRSKY | ATLAS-MATERIALS TESTING COMPANY mirsky@usa.net

WHEN DESIGNING FILTERS, engineers very often need to know what the filtered value at the output will be. This is especially important for variable switching power supplies operating at different duty cycles. The analysis presented here discusses the calculation of the filtered output for RC filters, which are common in feedback circuits, current transformers, output devices, and other circuits. However, the analysis easily can be extended to other kinds of filters.

It's well known that for rectangular-pulse inputs the rms values of the unfiltered output parameters, like voltage and current, are proportional to the square root of a duty cycle. But the designer of a feedback filter for a switching power supply must consider that the filter output is not an rms value but rather proportional to the pulse's duty cycle. You can adjust the filter's parameters to obtain an rms value, but it would be valid only for one duty-cycle value.

The analysis employs several assumptions:

- The filter works in a continuous-conduction mode, which means the filter's time constant is much greater than the pulse's repetition rate (period).
- The filter capacitor's charge and discharge time constants are the same. That means the impedance sourcing signal to the filter is much lower than the filter resistance and the filter's load impedance is much higher than the filter's resistance, which you can easily obtain by using an operational amplifier as a decoupling component.
- The filter's voltage grows in exponential steps (charging and discharging) that become smaller as the output voltage approaches its limit value.
- The filter is loaded with an impedance that is so high that it can be ignored.

We did the analysis with MathCAD 15, and anyone with the appropriate license can reproduce the results.

The expressions for the nth values of the filtered voltage's maximum, Vh, and minimum, Vlow, are:

$$Vh_n = Vlow_n + \left(V_A - Vlow_n\right)\cdot\left(1 - e^{\frac{-\tau_1}{\tau}}\right) \quad (1)$$

$$Vlow_n = Vh_{n-1}\left[e^{\frac{-(T-\tau_1)}{\tau}}\right] \quad (2)$$

where τ is the filter's time constant and τ_1 is the pulse duration *(Fig. 1)*. For simplicity, define:

$$\alpha = e^{\frac{-(T-\tau_1)}{\tau}} \quad (3)$$

$$\beta = 1 - e^{\frac{-\tau_1}{\tau}} \quad (4)$$

$$\gamma = e^{\frac{-\tau_1}{\tau}} \quad (5)$$

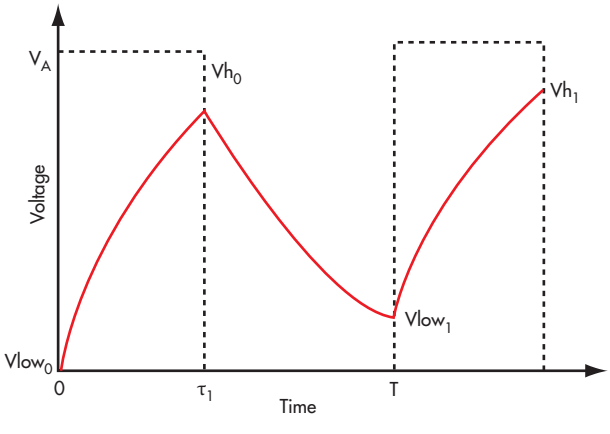
$$\tau_1 = DT \quad (6)$$

where D is the duty cycle of the input pulse train;

$$\tau = kT \quad (7)$$

where k is the number of periods for the filter time constant. So, Equations 1 and 2 become:

$$Vh_n = V_A\beta + Vlow_n\gamma \quad (8)$$



1. The plot of the input pulses (dashed lines) and filter output (solid lines) indicates the definition of the parameters used in the calculations.

$$Vlow_n = Vh_{(n-1)}\alpha \quad (9)$$

To derive the equation for the limit value of the filter output, you must use the recurrent equations for the low and high values and calculate the average, which is based on the initial parameters only. The equations for six high/low pairs are:

$Vh_0 = V_A\beta$
$Vlow_0 = 0$

$Vh_1 = V_A\beta(\gamma\alpha + 1)$
$Vlow_1 = V_A\beta\alpha$

$Vh_2 = V_A\beta(\gamma^2\alpha^2 + \gamma\alpha + 1)$
$Vlow_2 = V_A\beta\alpha(\gamma\alpha + 1)$

$Vh_3 = V_A\beta(\gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$
$Vlow_3 = V_A\beta\alpha(\gamma^2\alpha^2 + \gamma\alpha + 1)$

$Vh_4 = V_A\beta(\gamma^4\alpha^4 + \gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$
$Vlow_4 = V_A\beta\alpha(\gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$

$Vh_5 = V_A\beta(\gamma^5\alpha^5 + \gamma^4\alpha^4 + \gamma^3\alpha^3 + \gamma^2\alpha_2 + \gamma\alpha + 1)$
$Vlow_5 = V_A\beta\alpha(\gamma^4\alpha^4 + \gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$

Note from the above equations that:

$$Vlow_n = V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right] \quad (10)$$

and:

$$Vh_n = V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right] \quad (11)$$

The average for the output voltage is:

$$V_{limit_n} = Vlow_n + \left(\frac{Vh_n - Vlow_n}{2}\right) \quad (12)$$

You can calculate the limit for the normalized output voltage using MathCAD tools:

$$Limit = \frac{V_A + V_A e^{\frac{D-1}{k}} - V_A e^{-\frac{1}{k}} - V_A e^{-\frac{D}{k}}}{V_A\left(2e^{-\frac{1}{k}} - 2\right)} \quad (13)$$

or:

$$Limit = \frac{e^{-\frac{D}{k}} - e^{\frac{1}{k}(D-1)} + e^{-\frac{1}{k}} - 1}{2e^{-\frac{1}{k}} - 2} \quad (14)$$

(See the derivation of Equations 13 and 14 in "Normalized Output Voltage Limit Derivation," p. 91.)

Equation 14 is a transcendent equation with two variables, which is hard to solve symbolically. But you can find the limit value graphically by fixing the value of k and plotting the limit as a function of the duty cycle, D. If k = 100.0:

$$Limit(D) = \frac{e^{-D\frac{1}{k}} - e^{D\frac{1}{k}}e^{-\frac{1}{k}} + e^{-\frac{1}{k}} - 1}{2\left(e^{-\frac{1}{k}} - 1\right)} \quad (15)$$

A plot of this function shows that the limit of the normalized RC filter output is the duty cycle, D *(Fig. 2)*. To create an example, assign values to the variables in Figure 1:

$V_A = 1$ V

$D = 0.6$

$T = 20$ µs

$\tau_1 = DT$

$k = 50$

$\tau = kT$

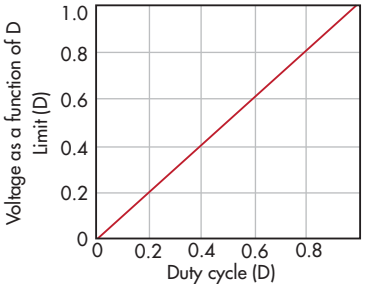
Then:

$\alpha = e^{-(T-\tau 1)/\tau} = 0.992$

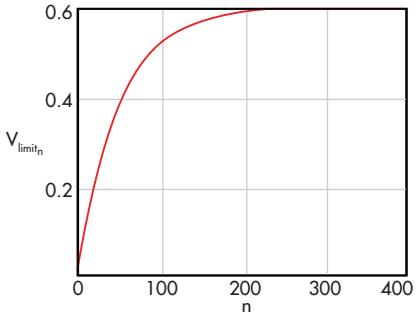
$\beta = 1 - e^{-\tau 1/\tau} = 0.012$

$\tau = e^{-\tau 1/\tau} = 0.988$

Then:



2. The normalized output voltage of the RC filter is the duty cycle value of the rectangular input pulses. The result does not depend on the value of k.



3. The limit value of the filtered voltage is equal to the input voltage's amplitude times the duty cycle.

$$\lim_{n\to\infty}\left[V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]+\frac{\left[V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right]-V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]\right]}{2}\right]\to 0.59999840001834787879(V) \quad (16)$$

To plot the graph for the limit, assign n = 1…400. Then:

$$Vlow_n = V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right] \quad (17)$$

$$Vh_n = V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right] \quad (18)$$

$$V_{limit_n} = \left[Vlow_n + \left(\frac{Vh_n - Vlow_n}{2}\right)\right] \quad (19)$$

Figure 3 shows the resulting plot.

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NORMALIZED OUTPUT VOLTAGE LIMIT DERIVATION

Equation 12 can be interpreted as:

$$\lim_{n\to\infty}\left[V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]+\frac{\left[V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right]-V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]\right]}{2}\right] \quad (1)$$

Its solution is:

$$\begin{cases}\text{signum}(V_A\beta,0)(\infty) \text{ if } \alpha=\dfrac{1}{\gamma}\\ \lim_{n\to\infty}\left[\dfrac{V_A\beta\left(\gamma\gamma^n\alpha\alpha^n-1\right)}{2\gamma\alpha-2}+\dfrac{V_A\beta\alpha\left(\gamma^n\alpha^n-1\right)}{2\gamma\alpha-2}\right] \text{ if } \alpha\neq\dfrac{1}{\gamma}\end{cases} \quad (2)$$

Only the lower expression is of interest:

$$\lim_{n\to\infty}\left[\frac{V_A\beta\left(\gamma\gamma^n\alpha\alpha^n-1\right)}{2\gamma\alpha-2}+\frac{V_A\beta\alpha\left(\gamma^n\alpha^n-1\right)}{2\gamma\alpha-2}\right] \quad (3)$$

Its solution is:

$$\begin{cases}0 \text{ if } \alpha=\dfrac{1}{\gamma}\\ \dfrac{V_A\beta\left(\alpha-\alpha\infty+1\right)}{2\gamma\alpha-2} \text{ if } 1<\gamma\alpha\\ \dfrac{V_A\beta\left(\alpha+1\right)}{2\gamma\alpha-2} \text{ if } \gamma|\alpha|<1\end{cases} \quad (4)$$

Again, only the lower expression is of interest:

$$-\left[\frac{V_A\left[1-e^{\frac{-DT}{kT}}\right]\left[e^{\frac{-(T-DT)}{kT}}+1\right]}{2\left(e^{\frac{-DT}{kT}}\right)\left(e^{\frac{-(T-DT)}{kT}}\right)-2}\right] \quad (5)$$

which can be converted into Equation 13.

Electronic Design

Ideas for Design

Vol. 2, No.7

Specialized Circuit Drives 150-V Piezoelectric Motor Using Low-Voltage Op Amp

Use a basic op amp and discrete components to drive a piezoelectric motor and provide circuit protection.

Model Diacs And Triacs For AC-Line Control

Diacs and triacs are often used for control of ac lines and are seeing increasing use in Internet-enabled line switches. However, the traditional approach of modeling them using bipolar transistors and diodes, and table-based models, can be confusing and offers limited success. This article explores functional models based on the LTspice simulator for improved results.

Microcontroller Solves Complex Temperature Polynomial Equations

This fast-executing program and simple circuit allows a PIC MCU to linearize a thermistor and accurately determine and display the temperature from its measured resistance.

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We look forward to seeing your ideas.

Specialized Circuit Drives 150-V Piezoelectric Motor Using Low-Voltage Op Amp

ALAN STUMMER | UNIVERSITY OF TORONTO astummer@physics.utoronto.ca

A PIEZOELECTRIC MOTOR is a linear motor with bidirectional motion. It uses friction to grip the armature while a voltage is ramped to warp the piezoelectric material and move the armature. The voltage then is quickly removed.

As the material springs back, it breaks away from the armature and returns to its zero position, leaving the armature a few micrometers further along its track. Repeat this at a kilohertz rate and for thousands of times.

While each of the motions is very small, after several seconds you may see that the armature has moved, if you look carefully. (Full disclosure: I had never heard of piezo motors before being asked to make a driver for one.)

There are two drive waveforms, one for forward and the other reverse: a sawtooth waveform with a slow linear rise followed by a fast fall, and its complement with a fast rise and slow linear fall. This was done using an op-amp triangle-wave oscillator at 1 kHz, with diodes switched in to speed up either the rising or falling edges to about 5% of the cycle. The driver's required bandwidth is only 10 to 15 kHz.

The problem is the voltage. Fortunately, it is unipolar. Unfortunately, it is +150 V (peak). The required current is quite small. It has to be only enough to charge and discharge the 20-nF piezo element. A calculation using charge transfer (Q) shows that during the ramp phase:

$$Q = It = CV$$

where:

$$t = 1\ \text{ms}$$
$$C = 20\ \text{nF}$$
$$V = 150\ \text{V}$$

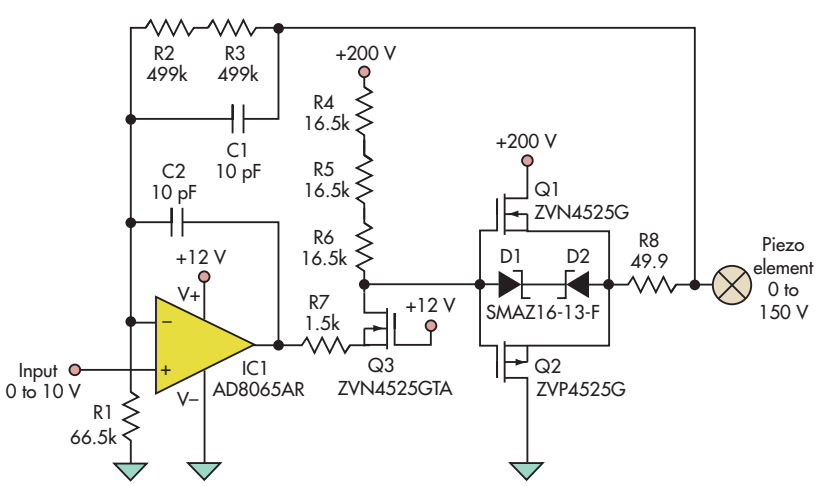
therefore:

$$I = CV/t = 3\ \text{mA}.$$

A 600-mW boost converter can be used to switch the +12 V up to +200 V with a 3-mA load requirement. The most straightforward circuit uses an op amp rated to at least 200 V. Op amps are available with this voltage rating, but they are meant for high-current applications and are quite expensive.

The circuit in the figure is much cheaper and based on a common op amp used as a non-inverting amplifier. The heart of the circuit is the current mirror of R7, N-channel FET Q3, and series-connected R4, R5, and R6. (The reason for using three resistors in series is explained below.)

With Q3 in a common-gate configuration and the gate at +12 V, its source voltage remains reasonably constant at +10 V (from +12 V less the $V_{gs(on)}$). Any output of op-amp IC1 less than that +10 V causes a voltage drop across R7, with the



A low-voltage op amp can be used to drive a higher-voltage piezoelectric motor. D1 and D2 protect the circuit against load shorts, while resistors in series strings are used to reduce individual resistor dissipation and minimize their voltage coefficient of resistance.

current coming from R4 to R6. Since R7 has the same current as R4 to R6, there is a voltage gain of the ratio of (R4 to R6)/R7 or 33. The voltage at the bottom of R4 to R6 (the Q3 drain) now has the required voltage swing but a high impedance.

A pair of complimentary FETs acts as followers to lower the output impedance and boost current output. Negative feedback is provided via R2 and R3, along with bandwidth limiting by C1. The overall closed-loop gain is set by (R2 + R3)/R1 + 1 = 16.

There are a few subtleties to the circuit. If something happened to the piezo motor, such as the user shorting it, Zener diodes D1 and D2 would protect the FET gates. The current-mirror high-side resistance provided by R4 through R6 is split into three distinct devices to handle the power levels so 0805/2012 surface-mount (SMT) resistors can be used. The feedback resistance composed of R2 and R3 is split into two devices to reduce the voltage coefficient of resistance. This is a somewhat obscure effect, where a component's resistance actually changes slightly at higher voltages.

There is a small feedback capacitor directly on the op amp to provide stability. Without it, the parasitic capacitances (most notably the Miller capacitances C_{dg} and the piezo's capacitance) would cause enough phase shift for the op amp to oscillate. Crossover distortion is not a problem because the piezo element could not react to that bandwidth and does not require a perfect waveform.

Another problem would be the infinite pole caused by a purely capacitive piezo element. By taking the feedback directly from the sources of Q1 and Q2, resistor R8 would add a more deterministic pole to the load and increase loop stability.

Once the somewhat finicky piezo motor was adjusted, the final circuit worked well. The armature would move back and forth with incredibly fine resolution.

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Model Diacs And Triacs For AC-Line Control

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DIACS AND TRIACS often are used for line-voltage control. They also are getting additional interest as part of Internet- and cell-phone-controlled power-line switches such as the Belkin WeMo Home Automation Switch.

The traditional approach has been to model them using bipolar transistors and diodes.[1] Table-based models have been used with varying success.[2] The functional model approach shown here works well and has been used extensively with the LTspice simulator (free, from Linear Technology).

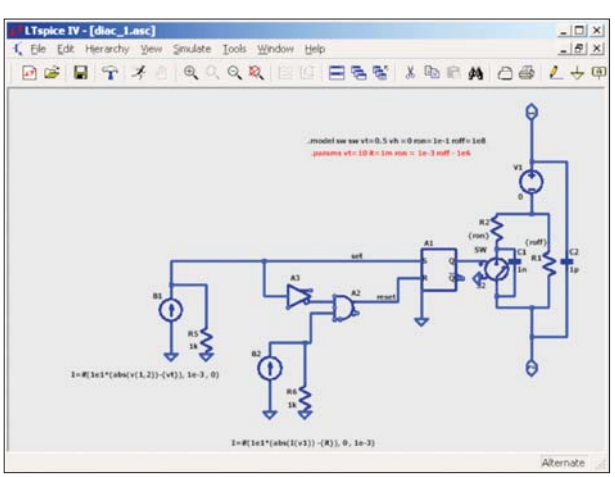
In the diac schematic of Figure 1 and associated Listing 1, there are four parameters *(Listing 1a is for the diac macromodel; Listing 1b is the diac symbol; listings are available with the online version of this article at electronicdesign.com)*:

V_t: voltage at which the diac triggers
I_t: current at which it turns off
R_{on}: resistance when it is on.
R_{off}: resistance when it is turned off

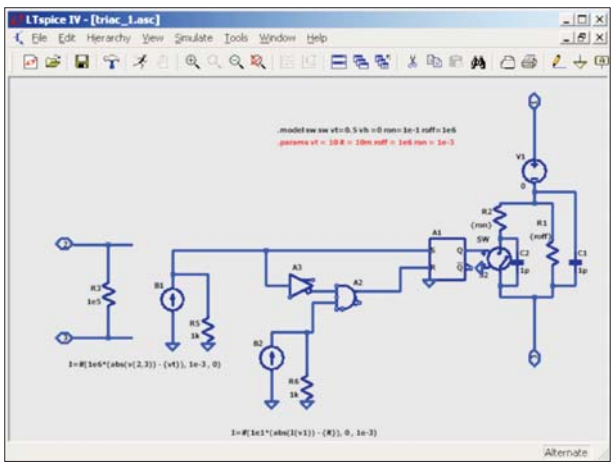
To turn on, the diac needs the voltage to exceed V_t. Once it turns on, it needs the current to go below I_t to turn off. In operation, the device starts as an open circuit. When the voltage across it exceeds V_t, the flip-flop is set, putting the device in its on state with a low resistance of R_{on}.

The device continues in this state until the current through it falls below I_t. At that point the flip flop is reset and the device switches once again to its off state, with a resistance R_{off}. (Note that the device is bi-directional.)

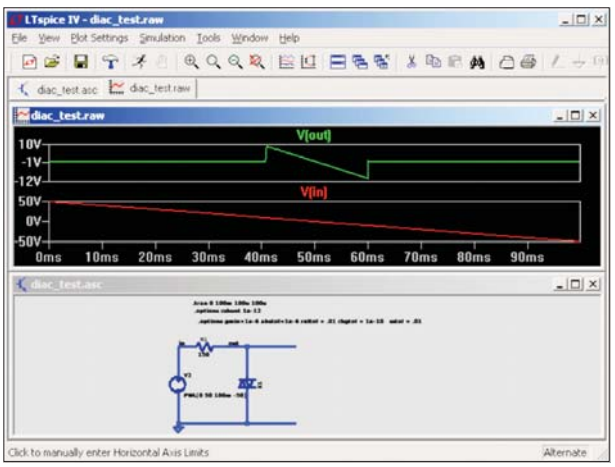
The triac is modeled in a similar manner *(Figure 2 and Listing 2; Listing 2a is for the triac macromodel; Listing 2b is the triac symbol)*. It has the same four parameters as the diac



1. In the diac circuit, the device starts as an open circuit and remains open until the voltage across it exceeds V_t



2. For the triac, the trigger voltage is on an independent port, in contrast to the diac.

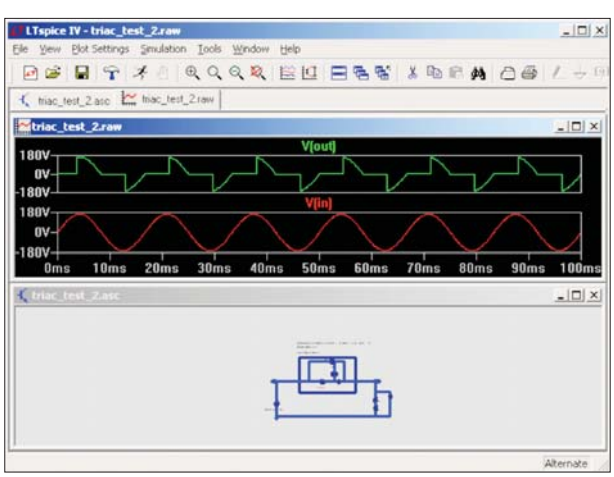


3. The results (top) of the diac test circuit (bottom) show the symmetrical operation of the circuit and allow for user modifications.

component, and it needs the voltage to exceed V_t to turn on. Once it turns on, it needs the current to go below I_t to turn off. The difference between the diac and the triac is that the triac trigger voltage is on an independent port.

It is difficult to design test circuits for these devices because, as a result of their negative resistances, they usually oscillate or provide limit cycles, which in turn makes it difficult for programs such as Spice to converge. The main diac characteristics of interest are breakover voltage, voltage symmetry, breakback voltage, breakover current, and power dissipation.[3]

In the output file for the diac test circuit, V_{In} is initially at its negative extreme, and V_{Out} is low, as the device is in its on state *(Figure 3 (top) and Listing 3a, and corresponding schematic*



4. The results (top) of the dimmer circuit (bottom) using a diac and triac show the operation possible with a standard resistive load.

Figure 3 (bottom) and Listing 3b). As V_{In} goes lower, the device turns off once the current falls below I_t. It again reaches its on state once the voltage exceeds V_t. The device is bidirectional and inherently symmetric. Also, the model can be modified to include current limits on voltages, as well as asymmetries.

For the triac, the popular dimmer circuit is used for test, with output file Figure 4 (top) and Listing 4a along with corresponding schematic Figure 4 (bottom) and Listing 4b. The load is a typical 100-W bulb, and the RC-time constant determines when the triac is triggered.

The diac in series with the gate is chosen to ensure the triac turns off completely. The model can be modified to include current limits, voltage asymmetries, dV/dt effects, and more. By varying the RC-time constant, the duty cycle of the output can be varied from 5° to about 170°, nearly spanning the full 0° to 180° theoretical limit. The device as modeled produces identical results in the positive and negative half cycles.

REFERENCES
1. "A Spice Model for Triacs," A.F. Petrie and Charles Hymowitz, www.readbag.com/intusoft-articles-triac
2. "Model for Diac in Orcad 9.2," www.edaboard.com/thread241914.html
3. "Diac Tutorial," American Microsemiconductor, www.americanmicrosemi.com/information/tutorial/index.php?t_id=2#ixzz2eObwolgW

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ideas for design

Microcontroller Solves Complex Temperature Polynomial Equations

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WHEN YOU NEED TO measure temperature using thermistors, you face the challenge of linearizing their response to get accurate readings. One of the best methods for linearizing a thermistor is the polynomial "Steinhart-Hart" equation (S-H), which has an error of 0.1°C. The temperature range for this design is from 0°C to 100°C.

Three thermistor coefficients—a, b, and c—are required to implement the S-H equation. If the manufacturer does not provide the coefficients, you can obtain them by solving the S-H equation *(Equations 1, 2, and 3)* for three different temperature points. In this design, a PIC MCU will solve such equations to provide accurate readings in 40 ms *(Fig. 1)*.

To illustrate, we will use the negative-temperature-coefficient (NTC) LM103 thermistor, which has the resistance at three different temperatures shown in Table 1. With these three measurements, the temperature is converted to the Kelvin scale and substituted into three Steinhart-Hart equations:

$$T_1 = \frac{1}{a + b\ln(R_1) + c[\ln(R_1)]^3} \quad (1)$$

$$T_2 = \frac{1}{a + b\ln(R_2) + c[\ln(R_2)]^3} \quad (2)$$

$$T_3 = \frac{1}{a + b\ln(R_3) + c[\ln(R_3)]^3} \quad (3)$$

Solving these three equations yields the coefficients a, b, and c *(Table 2)*. Substituting the coefficients in the Steinhart-Hart equation, we get the thermistor equation:

$$T_t = \frac{1}{2.501\times10^{-4} + 3.505\times10^{-4}(\mathrm{Ln}(\mathrm{Rt})) - 1.415\times10^{-7}[\mathrm{Ln}(\mathrm{Rt})]^3} \quad (4)$$

or:

$$T_t = \frac{10\times10^6}{(2501 + 3505\ln(\mathrm{Rt}) - 1.415\mathrm{Ln}(\mathrm{Rt})^3)/10} \quad (5)$$

The challenge for the PIC 16F887 microcontroller is to use Equation 4 to get true temperature readings. This project consumes 1227 words of the microcontroller's memory. Input AN0 is declared as analog, and the rest of the I/O lines are declared digital outputs. The analog-to-digital converter (ADC) is configured for 10 bits, with a sampling time of 50 µs.

The thermistor's voltage reading is stored in binary format in the variable "volt" with the instruction ADCIN 0, volt. Then, this reading is multiplied by 48,828 to convert it to decimal, and it is stored in a new variable called "v1." To obtain each decimal digit from variable "v1," the commands DIG3, DIG2, and DIG1 are used to store these readings in three variables called dig3, dig2, and dig, respectively.

The code, available with the online version of this article at *electronicdesign.com*, shows the software program where the following variables are declared for processing and storing the readings: B, A, C, L, volt, v1, v2, pattern, pattern2, pattern3, I, digit3, digit2, and digit. Two variables (conv1 and conv2) are required for binary-to-decimal conversions. They include the 10-bit resolution ADC's least significant bit (LSB), which is equal to 4.8828 mV.

The algorithm that was developed to get a temperature reading using the Steinhart-Hart equation requires several steps.

First, compute the power supply voltage (v1), which is equal to 48828 × volt2. Variable volt2 is read with the PIC's 10-bit ADC. If the power supply is correct, volt2 = %1111111111, and then v1 = 49,951,044. Now with the instruction DIV32,

TABLE 1: THERMISTOR RESISTANCE

Temperature (°C)	Resistance (kΩ)
2.7	23
27.5	8.8
66	2.7

TABLE 2: LM103 COEFFICIENTS

Coefficients	Value
A	2.501×10^{-4}
B	3.505×10^{-4}
C	-1.415×10^{-7}

the variable volt2 is divided by 10,000, giving a result equal to 4995, which represents the approximate value of 5 V from the power supply.

Second, the thermistor's voltage drop is computed with the same process from the first step, but with another analog-to-digital channel. Let's say we have a reading in the ADC of 2.5 V (adc = 1000000000). The voltage read is then 24,999,936, which is divided by 10 with DIV32 for a result of 2499, which approximates to 2.500 V.

Third, we proceed to find the resistor's value with:

$$R_2 = \frac{R_1 \times v_2}{E - v_2} \quad (6)$$

To achieve that, we store in a variable called "dif" the power's supply voltage minus the thermistor's voltage. Then we multiply the thermistor's voltage by the 10-kΩ fixed resistor, and we apply DIV32 to divide this last product by "dif," resulting in the thermistor's resistance value.

Fourth, we now compute the base 2 logarithm from the thermistor's resistance with Equations 7, 8, and 9:

$$M_1 = \left(\frac{M}{2^{a_0}}\right)^2 \quad (7)$$

$$M_2 = \left(\frac{M}{2^{a_1}}\right)^2 \quad (8)$$

$$M_3 = \left(\frac{M}{2^{a_2}}\right)^2 \quad (9)$$

where a_0, a_1, and a_2 are the next-digit mantissa in base 2.

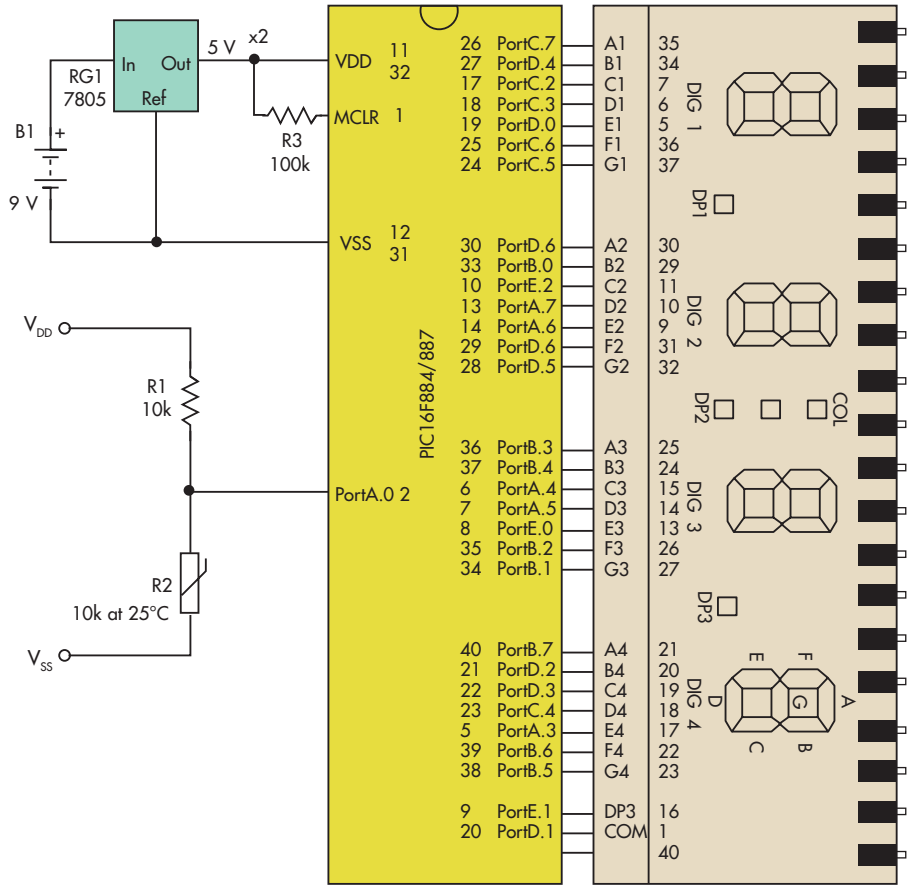
Next, we find the characteristic a_0 or logarithm's integer with the function NCD, which delivers the most significant bit (MSB) of a number. If we decrement it by 1, we get the base-2 logarithm characteristic. We know, for example, that the base-2 logarithm for number 47 is 5.554 using four significant digits. Thus, NCD (47) = 6, where 47 in binary is 00101111, and the MSB is in the sixth position from left to right. If we decrement it by 1, we get number 5, which is the logarithm's characteristic.

To get the logarithm, we need the Mantissa (fractions part). To compute it, we need the result of the successive divisions "wu" by 2 (). Nonetheless this operation or process cannot be applied directly, since dividing 47/2 results in 23.5, and we lose the fractions part. (PIC Basic Pro does not work with fractions.) Therefore, to keep the fractions part, we create a special subroutine that performs the following series:

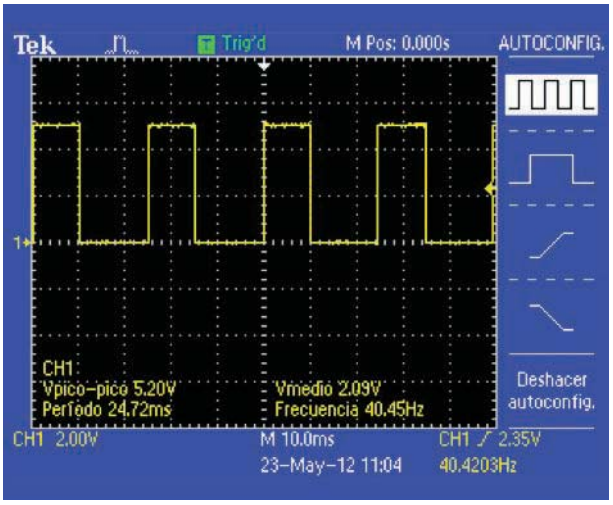
47/2 = 23.5, 23.5/2 = 11.75,
11.75/2 = 5.875, 5.875/2 = 2.9375, 2.9375/2 = 1.46875

When dividing 47/2 = 23, with a remainder of 1, this "1" appears in the first division of the five that will be performed. Therefore, the fraction $1/2^5 = 0.03125$. We cannot work with fractions, though, so instead of dividing by 1 by 2^n, we take the number 10,000 as a numerator, and we create a subroutine that computes the denominator depending on the number of division where appears a remainder of 1.

Then, we sum all the results of the divisions. To continue with this example, we have the following five steps:



1. This simple circuit for a high-precision thermometer drives a glass LCD with high efficiency, using the PIC 16F887 microcontroller.



2. A signal at 40-Hz delivered by RC2 is used for driving the LCD's common pin.

- 47/2 = 23, with a remainder of 1; this is the first division of 5, $10{,}000/2^5 = 312.5 = 312$
- 23/2 = 11, with a remainder of 1; this is the second division of 4, $10{,}000/2^4 = 625$
- 11/2 = 5, with a remainder of 1; $10{,}000/2^3 = 1250$
- 5/2 = 2, with a remainder of 1; $10{,}000/2^2 = 2500$
- 2/2=1, with a remainder of 0; there is no portion to add

In this case the variable "Ja" is equal to 4687, and it still needs to be incremented by one. Therefore, we divide "Ja" by 1000 and then we add up 1000. Therefore, Ja = 1468, obtaining approximately the original quantity mentioned above, multiplied by 1000 with four significant digits.

Once we have obtained M, we need to get the mantissa using the process described in Figure 1. The division by 2^{an} is not complicated because we are working in base 2, and the division is performed by 2^0 or 2^1. When raising to the square power, we must account for where we will multiply M_a by M_a, and then we use that division by 1000 with DIV32 because the result is greater than 16 bits.

After this process is performed a required number of times, we need to convert a_n to a decimal base. To achieve this, we multiply by the respective weight, 5, 25, 125, and so on sequentially. And because we cannot work with fractions, we multiply by 5000, 2500, etc.

Finally, we add all the elements to the Mantissa a_n in decimal format and divide the sum of all of them by 10. We sum $a_0 \times 1000$ and we save it in variable "l2," so "l2" stores the value of the logarithm in base 2 of the thermistor's impedance. The last step to obtain the natural logarithm is to apply the equation shown below to change its base:

LINEARIZATION INSPIRES A SOLUTION

WE ORIGINALLY CONCEIVED of this idea as a solution to the problem faced by engineers in trying to linearize a thermistor's response. We know there are analog methods to achieve this, such as putting a parallel resistor across the thermistor, constant current bias, or a combination of both. Then you get an almost linear response defined by a straight line. In this case, you have to design a signal conditioning circuit based on op amps, which adds more hardware to the project. Another option we had was using the thermistor's characteristic equation, but it is not accurate over the entire temperature range. Therefore, we decided to use the venerable Steinhart-Hart equation.

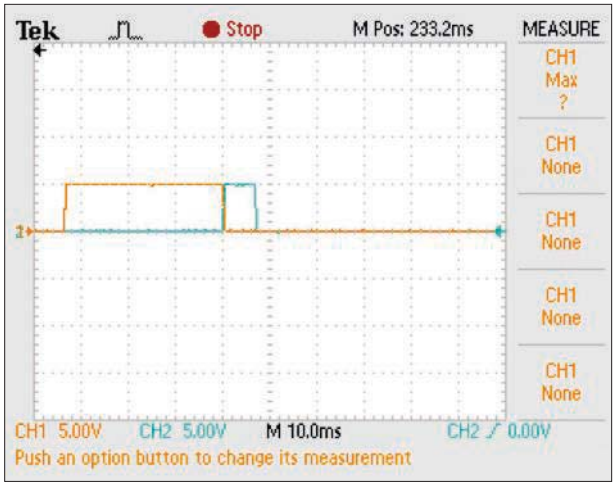
With this in mind, we faced a new challenge: how to get the logarithm of a voltage reading. This had to be done without getting overflow errors in the microcontroller. After trying with different methods (Taylor series, Babylonian, etc.), we found that the most appropriate algorithm for this project was the one from Dr. G. Mayer in his paper "computing logarithms digit-by-digit." So the method was developed in base two, and at the end of the process, it was converted to base 10. Once this was achieved, the final step was to substitute the resulting Ln values into the S-H equation to get accurate temperature readings.

The total algorithm's processing time was 32 ms with the internal microcontroller's oscillator set at 4 MHz. Some readers have been asking how to reduce the processing time. It can be reduced to less than 10 ms by selecting a higher oscillator's frequency in the algorithm itself.

We decided to drive a numerical LCD directly without external decoders for energy-saving applications. You can choose other types of displays to free the microcontroller's ports for other control applications. We are currently working with tiny eight-pin based microcontrollers driving serial displays. The advantage of designing algorithms is that you can transfer them to any microcontroller, and you don't need to be tied to a specific structured language.

CORRECTION

"BUILD A HIGH-FREQUENCY Portable Spectrum Analyzer Using Two Filter ICs" by in our Oct. 17 issue repeated Figure 2 as Figures 3 and 4. See http://electronicdesign.com/test-amp-measurement/build-high-frequency-portable-spectrum-analyzer-using-two-filter-ics for the correct figures.



3. The yellow signal is the logarithm's processing time of 33 ms. The 7-ms blue line is the time required to get a true reading by the MCU. Thus, the total processing time is 40 ms.

$$\log_2 x \, (\ln 2) = \ln x$$

We know that ln(2)= 0.6931, so we just need to multiply "l2" by 6931 and then divide it by 10,000 using the DIV32 command to store it in variable "lm," which is the natural logarithm of the resistor multiplied by 1000.

To drive the common pin of the LCD, a for-next loop enables the output RC2 to be "1" *(Fig. 2)*. Then the subroutine "D" is invoked to convert the decimal data to a seven-segment code. The LOOKUP function decodes the decimal value of digit3 to a seven-segment format that is stored in variable pattern3. Now the value of RC2 (stored as a byte in variable L) is XORED with pattern3 to drive the LCD in phase.

This process is repeated with the other two digits while a 10-ms pause is added. Then, RC2 is turned off and stored as a byte in variable L. Subroutine D is invoked again and the process is repeated with the phase output (RC2) changed for another 10 ms. After every LOOKUP function, every pin is assigned to the corresponding port's pin dedicated to drive each LCD segment. Total time required is 40 ms *(Fig. 3)*.

Reference

Computing Logarithms Digit-by-Digit, Mayer Goldberg, BRICS RS-04-17. ISSN: 0909-0878

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