Electronic Design

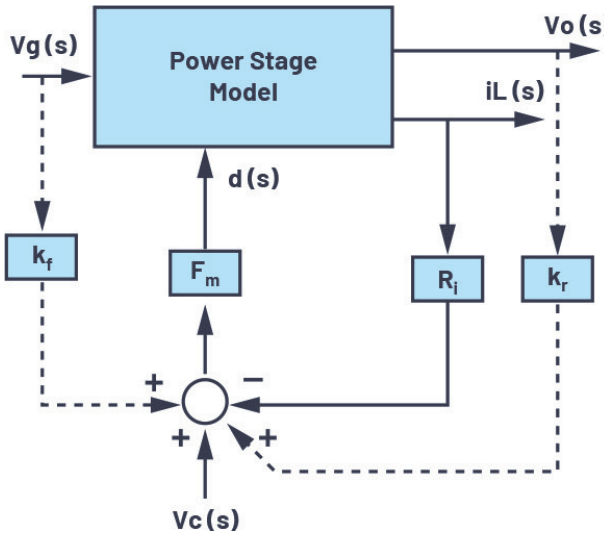
WEI GU, Applications Director

# A Unified LTspice AC Model for Current-Mode DC-DC Converters

**Current-mode control is a popular alternative to voltage-mode control due to its better line noise rejection, automatic overcurrent protection, and other benefits. This article explores a feedback control model for power supplies with current-mode control.**

When a power-supply designer wants to gain a general understanding of a power supply's feedback loop, they turn to Bode plots of loop gain and phase. Knowing the loop response can be predictive, helping to narrow the field of feedback loop compensation components.

The most accurate way to produce the gain and phase plots is to put the supply on the bench and use a network analyzer. However, in the early stages of design, most designers prefer turning to a computer simulation, which can help them quickly settle on a rough range of components—and help build an intuitive understanding of the loop response to parametric changes.




**1. Average model for current-mode control by R. D. Middlebrook.**

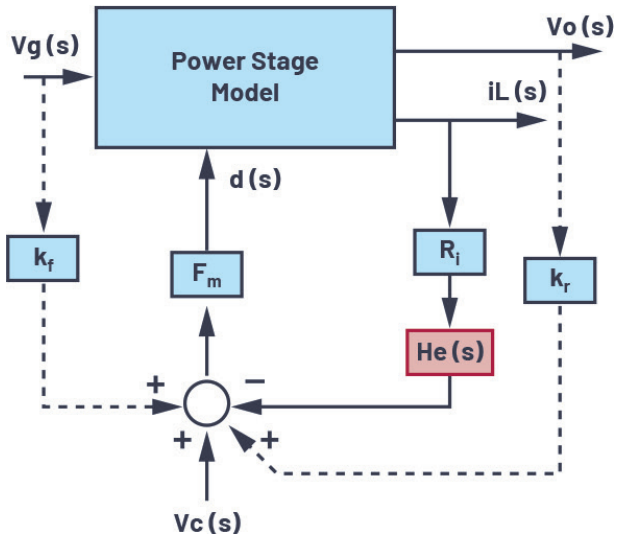
This article focuses on a feedback control model for current-mode-control power supplies. Current-mode control is popular in switch-mode dc-dc converters and regulators because it has a number of advantages over voltage-mode control—better line noise rejection, automatic overcurrent protection, easy parallel operation, and improved dynamic response.

Designers already have access to a significant number of current-mode power-supply average models. Some are accurate to half the switching frequency—matching the increasing bandwidth of converters—but only for limited topologies, such as buck, boost, and buck-boost (not four-switch buck-boost). Unfortunately, three- or four-terminal average models for use with topologies such as SEPIC and Ćuk are not accurate up to half the switching frequency.

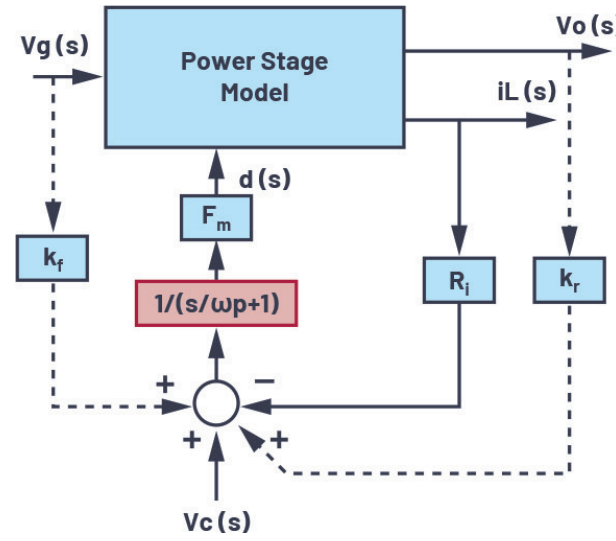
Presented here is an LTspice simulation model that's accurate up to half the frequency (even relatively high frequency) for a wide range of topologies, including:

- Buck
- Boost
- Buck-boost
- SEPIC
- Ćuk
- Forward
- Flyback

Simulation for piecewise linear system (SIMPLIS) results are provided to confirm the validity of the new model, and specific applications of the model are shown in examples. For some examples, bench results are used to validate the model.




**2. Modified average model for current-mode control by R. B. Ridley.**




**3. Modified average model for current-mode control by F. D. Tan.**

**Current-Mode Control Modeling: A Very Brief Overview**

Here, we'll revisit some of the highlights of current-mode-control modeling. For a more complete understanding of current-mode modeling, turn to the publications noted in the References section at the end of this article.

The purpose of the current loop is to make the inductor current follow the control signal. In the current loop, averaged inductor-current information is fed back to a modulator with sensing gain. Modulator gain $F_m$ is derived by geometrical calculations, assuming a constant inductor current ramp and an external ramp. To model the effect of the variation of the inductor current ramp, two additional gains are added to the model: feed forward gain ($k_f$) and feedback gain ($k_r$) *(Fig. 1)*.

To extend the validity of the average model as shown in *Figure 1* into the high-frequency range, several modified average models are proposed based on the results of discrete-time analysis and sample-data analysis. In R. B. Ridley's model *(Fig. 2)*, sample-and-hold effects are equivalently represented by the $H_e(s)$ function, which is inserted into the feedback path of the inductor current in the continuous average model. Due to its origination from the discrete-time model, this model can accurately predict subharmonic oscillations.

Another modified average model is proposed by F. D. Tan and R. D. Middlebrook. To consider the sampling effects in the current loop, one additional pole must be added to a current-loop gain derived from the low-frequency model *(Fig. 3)*.

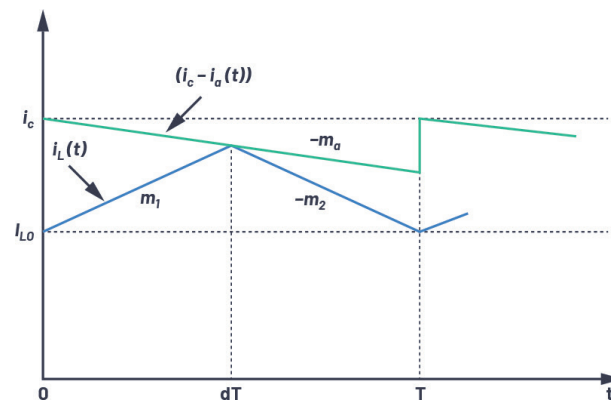
In addition to R. B. Ridley's model, the current programmed controller model introduced by R. W. Erickson also is very popular. The inductor current waveform is illustrated in *Figure 4*.

The average inductor current is expressed as:

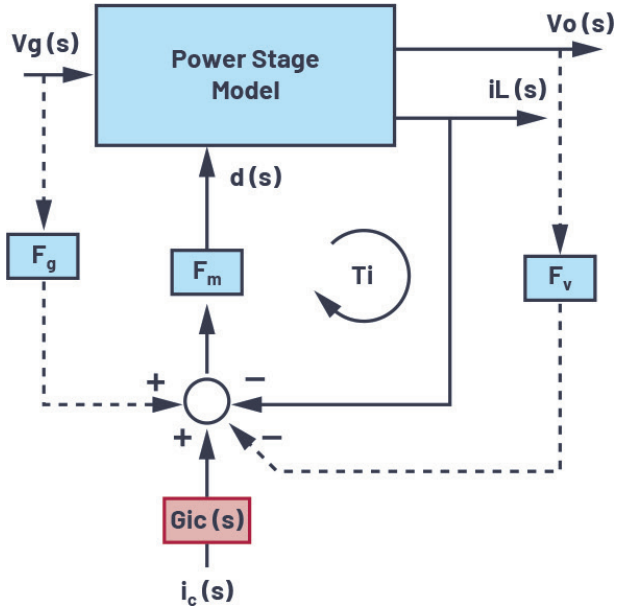
$$<i_L(t)>_T = <i_c(t)>_T - M_a dT - \frac{d^2T}{2} m_1(t) - \frac{(1-d)^2T}{2} m_2(t) \quad (1)$$

where $i_L$ is the sensed current, $i_c$ is the current command from the error amplifier, $M_a$ is the artificial ramp slope, and $m_1$ and $m_2$ are the upward and downward slopes of output inductor current. Perturbation and linearization results in:

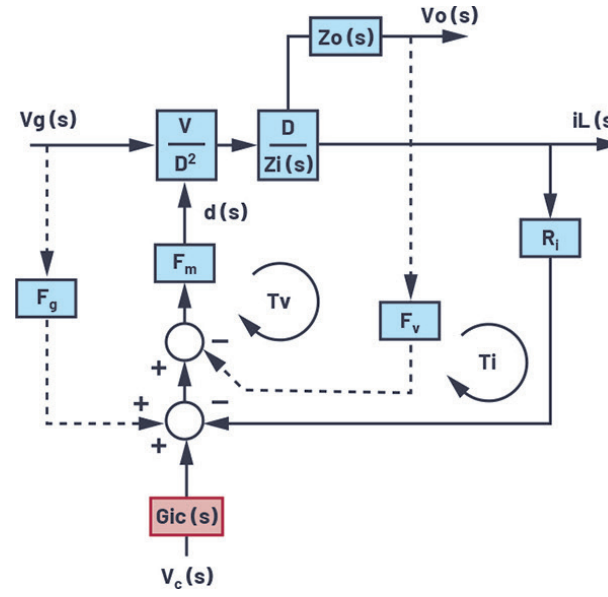
$$\hat{d}(t) = \frac{1}{M_a T}\left[\hat{i}_c(t) - \hat{i}_L(t) - \frac{D^2T}{2}\hat{m}_1(t) - \frac{(1-D)^2T}{2}\hat{m}_2(t)\right] \quad (2)$$




**4. Steady-state inductor current waveform with an external ramp.**




**5. Proposed modified average model for current-mode control.**




**6. Block diagram of the modified average model for a buck converter.**

Based on this equation and the canonical switch model, current-mode converter models can be obtained.

**A New Modified Average Model**

R. W. Erickson's model gives power-supply designers excellent physical insight, but it's not accurate up to half the switching frequency. To extend the validation of the model to the high-frequency range, a modified average model *(Fig. 5)* is proposed based on the results of discrete-time analysis and sample-data analysis.

Sampled-data modeling of inductor dynamics establishes:

$$\frac{\hat{i}_L(s)}{\hat{i}_C(s)} = \frac{1-\alpha}{1-\alpha e^{-sT}} \frac{1-e^{-sT}}{sT} \tag{3}$$

where T is the switch period and

$$\alpha = -\frac{1-\frac{m_a}{m_2}}{\frac{1-D}{D}+\frac{m_a}{m_2}} \tag{4}$$

$G_{ic}(s)$ of the model shown in *Figure 5* can be derived:

$$G_{ic}(s) = \left(1+\frac{s}{\omega_c}\right)\frac{1-\alpha}{1-\alpha e^{-sT}} \frac{1-e^{-sT}}{sT} \tag{5}$$

where $\omega_c$ is the crossover frequency of the inner current loop $T_i$ as shown in *Figure 5*, with the values $\omega_c$ of various topologies derived and shown in *Table 1*.

**Table 1: Inner Current-Loop Crossover Frequency ($\omega_c$) by Topology**

| Topologies | Current Loop ($\omega_c$) |
|---|---|
| Buck | $V_{IN}/L/M_a/T$ |
| Boost | $V_O/L/M_a/T$ |
| Buck-boost, Ćuk* | $(V_{IN} - V_O)/L/M_a/T$ |
| SEPIC* | $(V_{IN} + V_O)/L/M_a/T$ |
| Flyback** | $(V_{IN} + V_O/N_{SP})/L/M_a/T$ |
| Forward** | $V_{IN} \times N_{SP}^2/L/M_a/T$ |

*For two separated inductors, L = L1 × L2/(L1 + L2)

**$N_{SP}$ is the turns ratio of secondary to primary

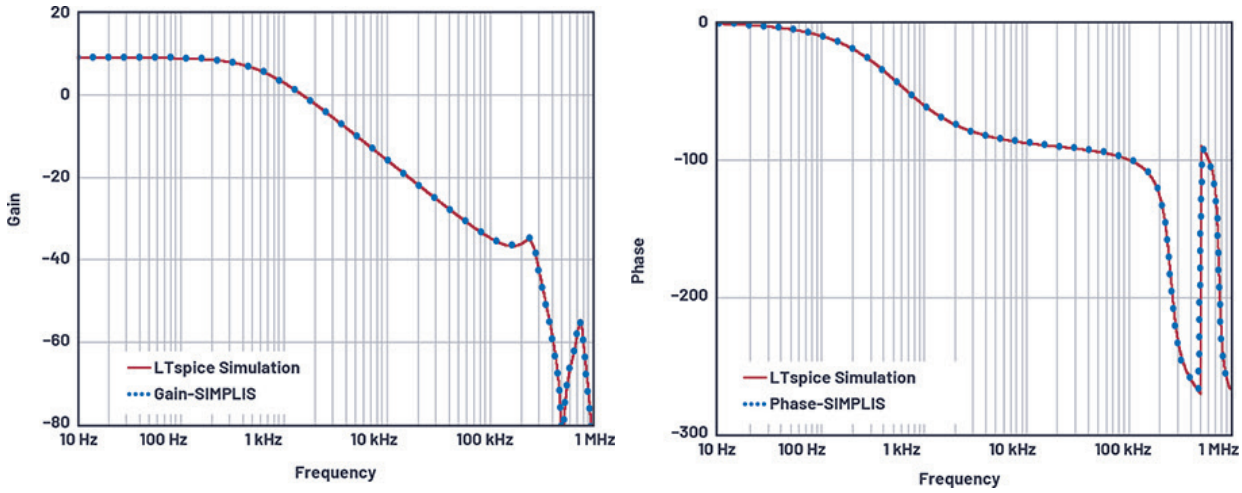
**A Buck Converter Example**

In *Figure 5*, we treat the $F_v$ feedback loop and $i_L$ feedback loops in parallel. We could also draw the $F_v$ feedback loop as internal to the $i_L$ feedback loop. A complete buck converter model with the added $G_{ic}(s)$ stage is shown in *Figure 6*.

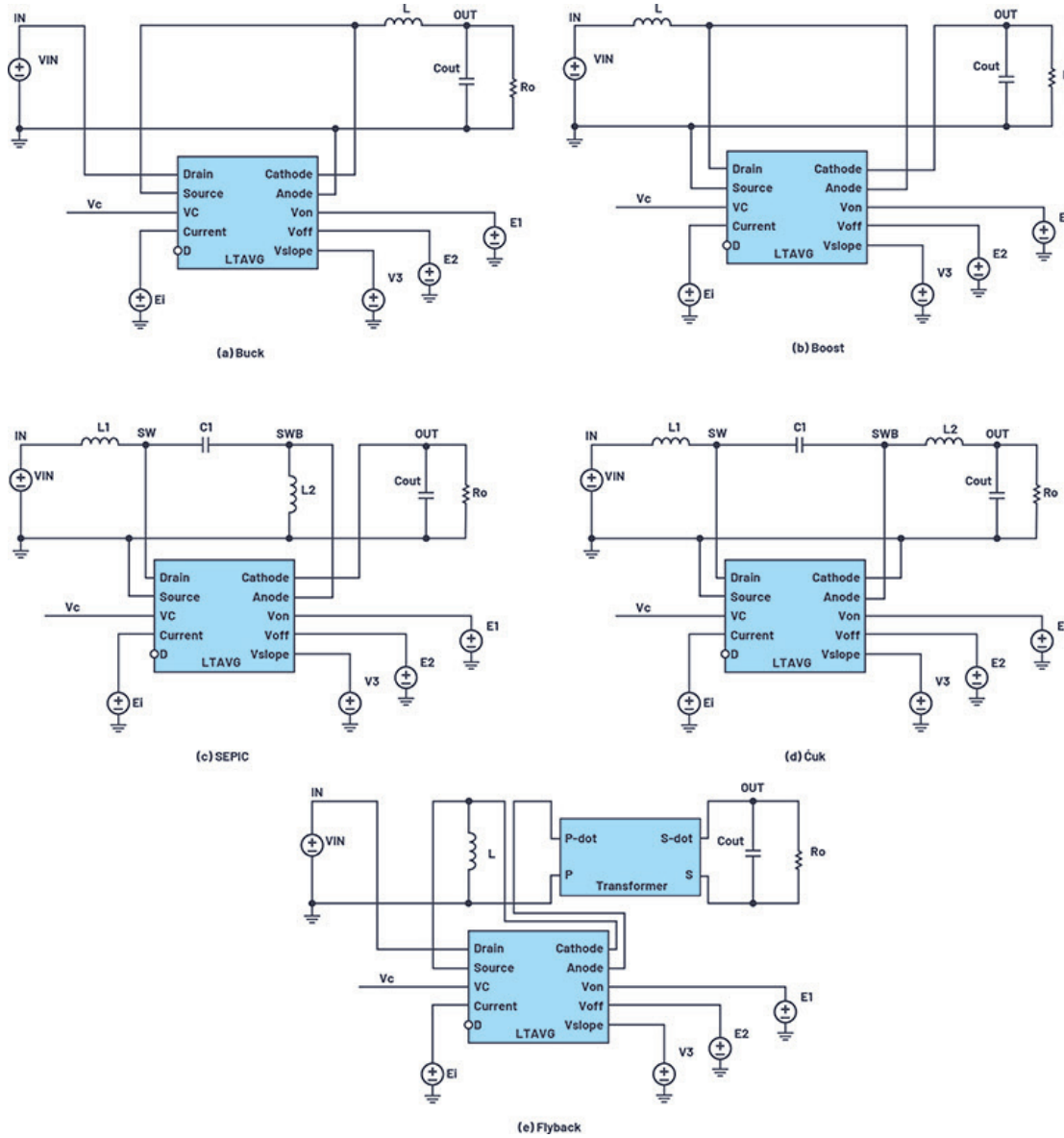
The control-to-output transfer function $G_{vc}(s)$ is:

$$G_{vc}(s) = Z_o(s)\frac{T_i(s)}{1+T_i(s)} G_{ic}(s) \tag{6}$$

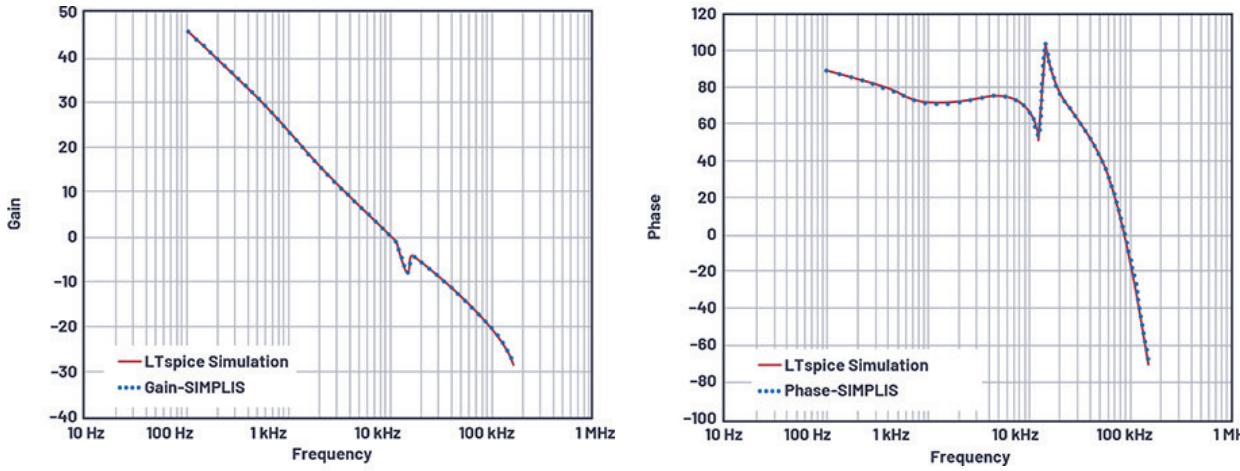
The current loop gain $T_i(s)$ and voltage loop gain $T_v(s)$ are calculated by:




**7. MathCAD results vs. SIMPLIS results ($f_{SW}$ = 500 kHz).**



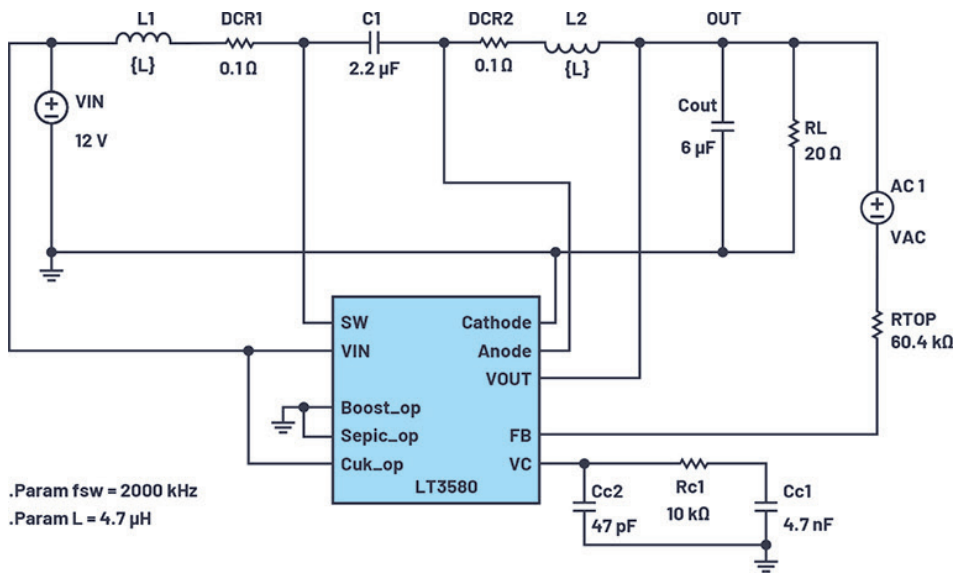

**8. Using the LTspice model for various topologies: (a) buck, (b) boost, (c) SEPIC, (d) Ćuk, and (e) flyback.**



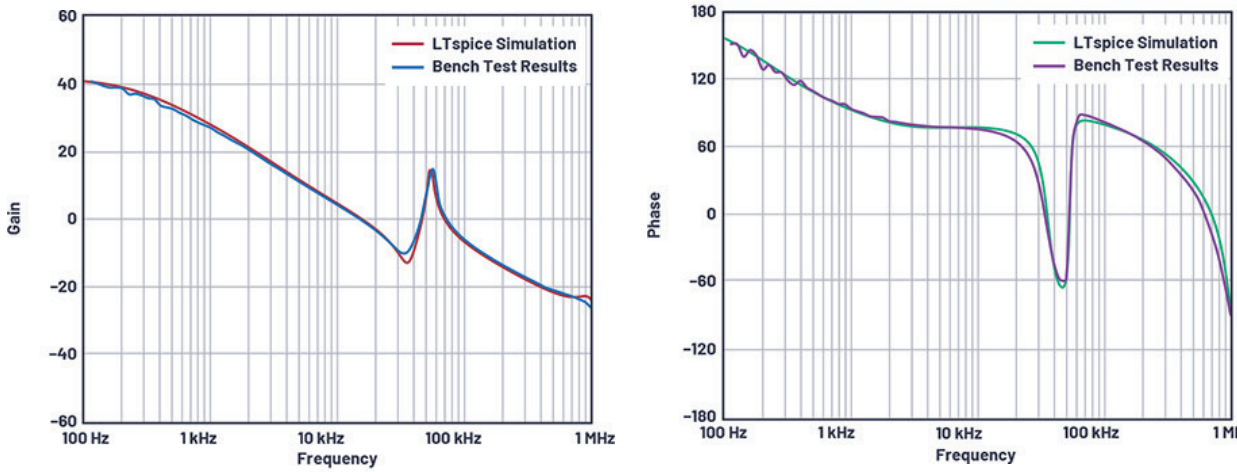

**9. LTspice results vs. SIMPLIS results for a SEPIC converter ($f_{SW}$ = 300 kHz).**

**Table 2: LTspice Behavioral Voltage Source Directives for the Circuits in Figure 8**

| Topology | E1 | E2 | V3 | Ei |
|---|---|---|---|---|
| Buck | V(IN) – V(OUT) | V(OUT) | $M_a/f_{sw}$ | i(L) |
| Boost | V(IN) | V(OUT) – V(IN) | $M_a/f_{sw}$ | i(L) |
| SEPIC | V(SW) – V(SWB) + V(IN) | V(OUT) + V(SW) – V(SWB) – V(IN) | $M_a/f_{sw}$ | i(L1) + i(L2) |
| Ćuk | V(SW) – V(SWB) + V(OUT) + V(IN) | V(OUT) + V(SW) – V(SWB) – V(IN) | $M_a/f_{sw}$ | i(L1) + i(L2) |
| Flyback | V(IN) | V(OUT)/Nsp | $M_a/f_{sw}$ | i(L) |




**10. LT3580 LTspice model.**




**11. Ćuk converter: LTspice simulation Bode plots vs. bench results ($f_{SW}$ = 2 MHz).**

$$T_i(s) = \frac{R_i}{Z_o(s)Fv} \frac{T_v(s)}{1 + T_v(s)} \quad (7)$$

and

$$T_v(s) = F_m \frac{V}{D} \frac{Z_o(s)}{Z_i(s)} F_v \quad (8)$$

where:

$$F_v = \frac{(1-2D)T}{2L},$$

$$F_m = \frac{1}{M_a T},$$

$$Z_o(s) = \frac{R_o}{1 + sC_{out}R_o} \text{ and}$$

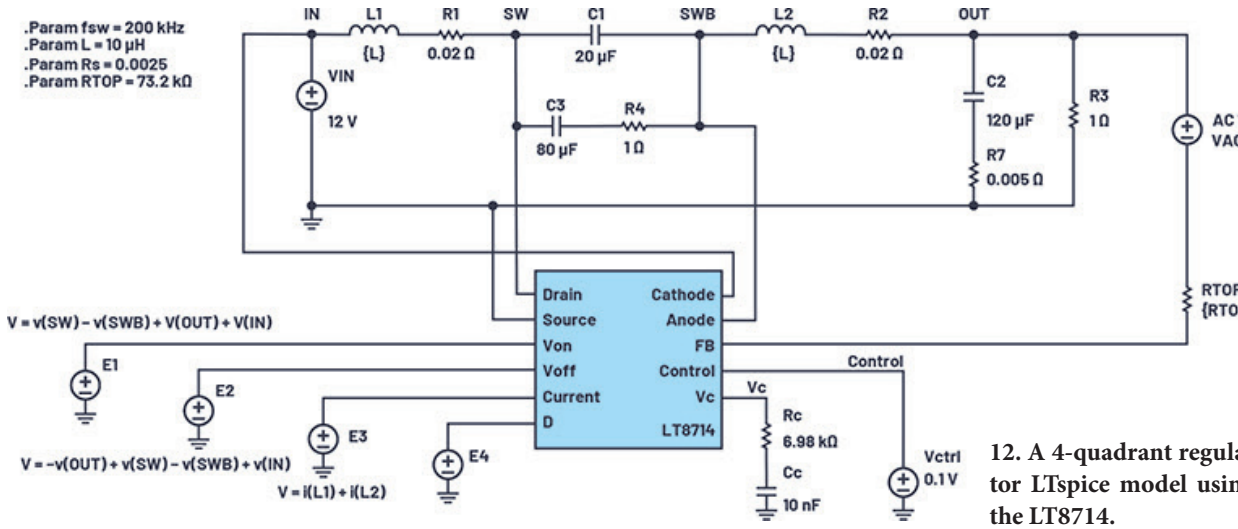
$$Z_i(s) = \frac{R_o}{1 + sC_{out}R_o} + sL \quad (9)$$

In *Figure 7*, calculated loop gain based on the new current-mode model agrees well with SIMPLIS results. In this example, $V_{IN}$ = 12 V, $V_{OUT}$ = 6 V, $I_{OUT}$ = 3 A, L = 10 µH, $C_{OUT}$ = 100 µF, and $f_{SW}$ = 500 kHz.

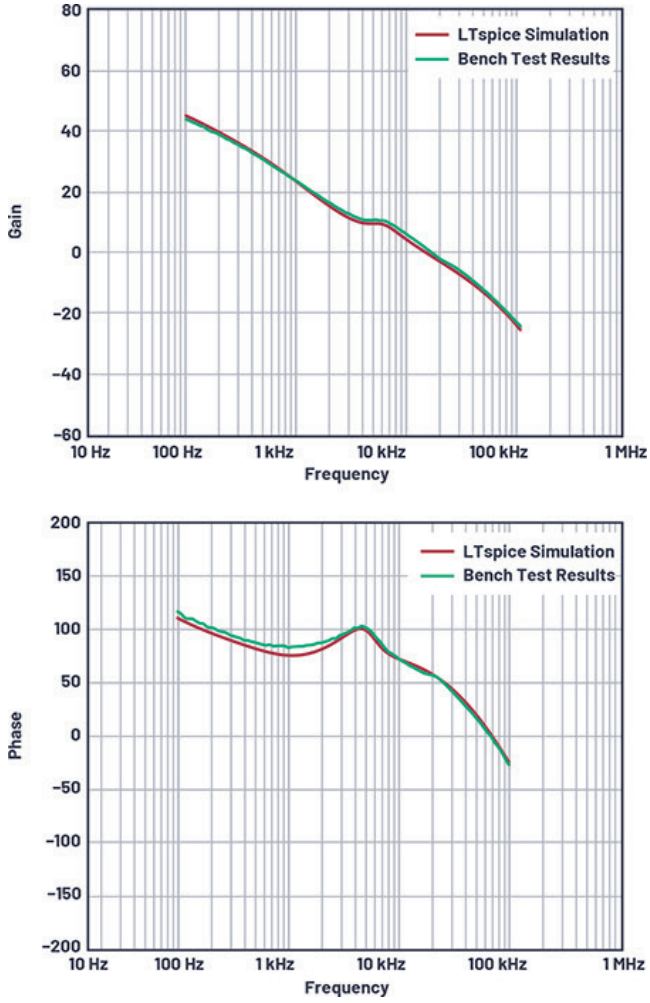
**A Four-Terminal Model with LTspice**

A 4-terminal model is built based on the modified average model shown in *Figure 5*. This four-terminal model can be used to analyze any pulse-width-modulation (PWM) topology for dc and small-signal characteristics using a standard electronic circuit analysis program, such as the free LTspice, in closed-loop operation.

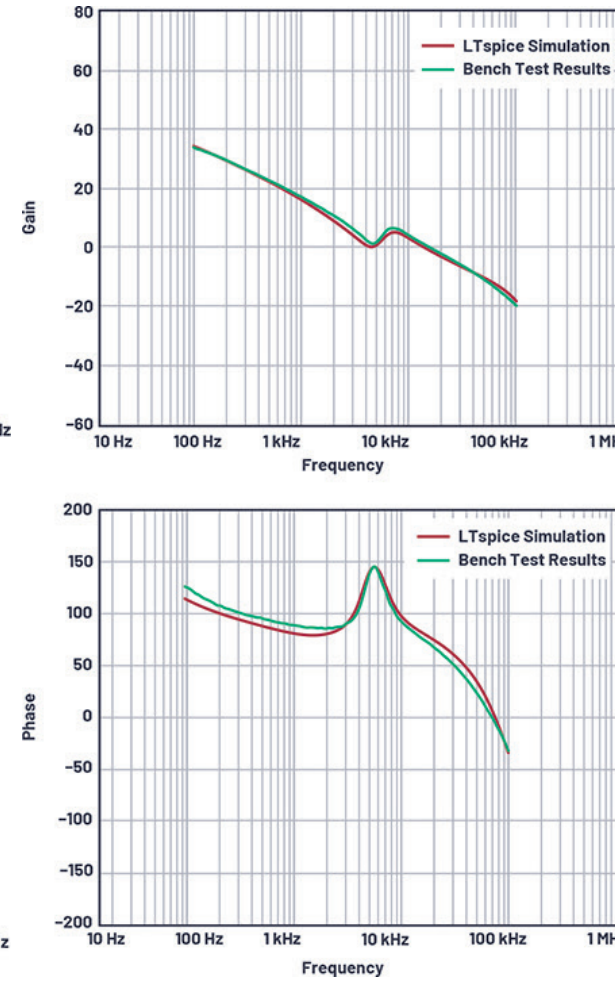
*Figure 8* shows LTspice simulation schematics for various topologies using the same model for each. The feedback resistor divider, error amplifier, and compensation compo-




**12. A 4-quadrant regulator LTspice model using the LT8714.**




**13. Four-quadrant regulator model: LTspice simulation Bode plots vs. those produced on the benchtop ($f_{SW}$ = 200 kHz).**

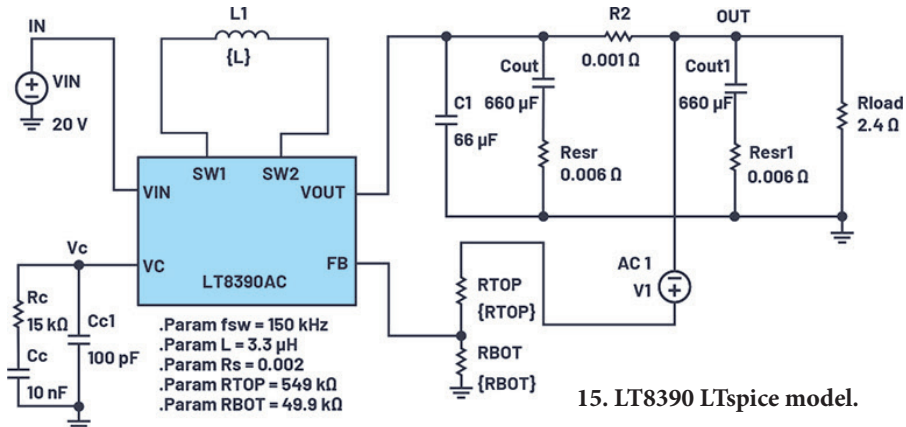



**14. Four-quadrant regulator model: LTspice simulation Bode plots vs, those produced on the benchtop ($f_{SW}$ = 200 kHz).**

nents aren't drawn here. To use the model with a real dc-dc converter model, the output of the error amplifier should be connected to the VC pin.

The various LTspice behavioral voltage-source directives in *Figure 8* are shown in *Table 2*. E1 is the voltage across the inductor when the switch is on, E2 is the voltage when the switch is off, V3 is the slope compensation amplitude, and Ei is the inductor current.

The simulation results for a SEPIC converter with two separated inductors are shown in *Figure 9*, which match the SIMPLIS results up to half the switching frequency. In this example: $V_{IN}$ = 20 V, $V_{OUT}$ = 12 V, $I_{OUT}$ = 3 A, L = 4.7 µH, $C_{OUT}$ = 120 µF, C1 = 10 µF, and $f_{SW}$ = 300 kHz.



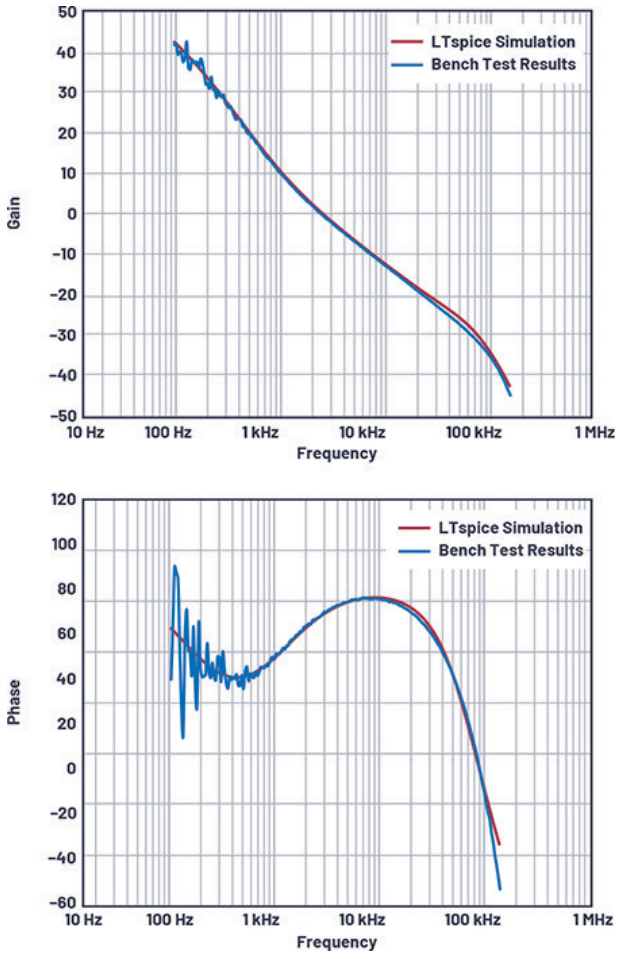

**15. LT8390 LTspice model.**

**Bench Verification of the New Models**

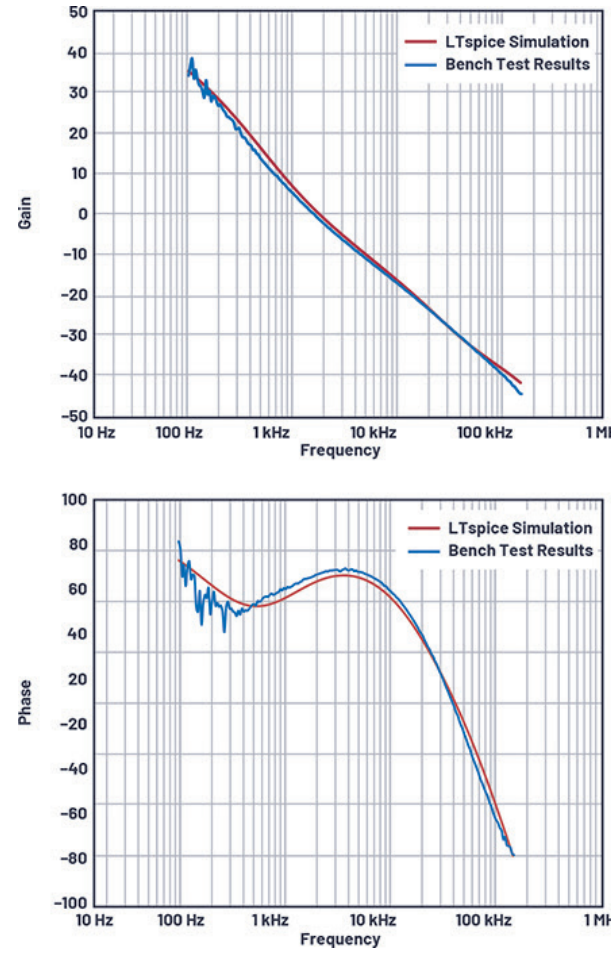
The new LTspice models in *Figure 11* were bench verified for topologies previously unsupported by traditional models, including Ćuk, and four-quadrant and four-switch buck-boost.

*Verifying the Ćuk Regulator Model on the Bench*

The LT3580 is a PWM dc-dc converter containing an internal




**16. LTspice simulation vs. bench results: buck mode ($f_{SW}$ = 150 kHz). $V_{IN}$ = 20 V, $V_{OUT}$ = 12 V, and $I_{OUT}$ = 5 A.**




**17. LTspice simulation and bench results: boost mode ($f_{SW}$ = 150 kHz). $V_{IN}$ = 8 V, $V_{OUT}$ = 12 V, and $I_{OUT}$ = 5 A.**

2-A, 42-V switch. The LT3580 can be configured as either a boost, SEPIC, or Ćuk converter, and its ac model may be used for all of these topologies. *Figure 10* shows a Ćuk converter with $f_{SW}$ = 2 MHz and $V_{OUT}$ = –5 V. *Figure 11* compares the LTspice simulation Bode plots with bench results—they match well up to half the switching frequency.

*Verifying a Four-Quadrant Regulator Model on the Bench*

The LT8714 is a synchronous PWM dc-dc controller designed for a four-quadrant output converter. The output voltage cleanly transitions through zero volts with sourcing and sinking output-current capability. The LT8714 is ideal for regulating to positive, negative, or zero-volt outputs when configured for the novel four-quadrant topology. Applications include four-quadrant power supplies, high-power bidirectional current sources, active loads, and high-power, low-frequency signal amplification.

Based on the CONTROL pin voltage, the output can be positive or negative. In the example shown in *Figure 12*, when the pin voltage is 0.1 V, the output is –5 V, and when the pin voltage is 1 V, the output is 5 V, $V_{IN}$ is 12 V, and the switching frequency is 200 kHz.

*Figure 13* compares the LTspice simulation Bode plots with those produced on the benchtop—they match well up to half the switching frequency. The control voltage (CONTROL) is 1 V, which sets $V_{OUT}$ (OUT) to 5 V.

*Figure 14* compares the LTspice simulation Bode plots with bench results—matching well up to half the switching frequency. The control voltage (CONTROL) is 0.1 V, which sets $V_{OUT}$ (OUT) to –5 V.

*Verifying a Four-Switch Buck-Boost Model on the Bench*

The LT8390 is a synchronous four-switch buck-boost dc-dc controller that can regulate the output voltage (and input or output current) from an input voltage above, below, or equal to the output voltage. The proprietary peak-buck/peak-boost current-mode-control scheme allows for adjustable fixed-frequency operation.

The LT8390 LTspice ac model monitors the input and output voltages and automatically picks one of the four operation modes: buck, peak-buck, peak-boost, and boost. An LT8390 example circuit is shown in *Figure 15*. The LTspice simulation and bench results are shown in *Figure 16* and *Figure 17* for buck and boost mode, respectively. The curves match well up to half the switching frequency.

**Summary**

A current-mode-control model is established to provide both the accuracy of the sample-data model and the simplicity and versatility of a four-terminal switch model. A unified LTspice model—accurate up to half the switching frequency—is presented for buck, boost, buck-boost, SEPIC, Ćuk, flyback, and forward topologies. The LTspice results are validated by bench data. The model is intended for loop analysis in design of current-mode converters in continuous conduction mode.

*Wei Gu is an applications director for power products. He has been with Analog Devices (formerly Linear Technology) since 2006. He received a B.S. in electrical engineering from Zhejiang University and a Ph.D. in electrical engineering from the University of Central Florida.*

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