Electronic Design

FAQ

IN-DESIGN DESIGN RULE CHECKING FOR INTEGRATED CIRCUITS

Q: What is design rule checking and how does it work?

A: To accurately manufacture an integrated circuit (IC), the design layout must be possible for the foundry to produce. Design rules are technology node-specific and change whenever the foundry shifts to a new manufacturing process. Design rule checking (DRC) tools evaluate the circuit layout and find all the places where the design does not comply with the rules. Every design must be DRC-clean prior to being sent to the foundry for manufacturing. Yet, note that all DRC tools are not the same.

Q: How do you mean, all DRC tools are not the same?

A: Electronic design automation (EDA) companies create rule decks that interpret the foundry design rules in code form. Every DRC deck is slightly different because different people interpret the rules differently, then write the design rule checks in various ways. Once a foundry develops a new process node, they must check to be sure that the DRC deck will properly check those rules and accurately find all errors.

The rule deck from each EDA company is evaluated by the foundry and must pass all their checks to be certified as "qualified." This means the foundry will accept DRC-clean designs based on the results obtained from running DRC with that rule deck.

So, how is this done? The foundry uses a "reference" DRC deck—the deck it used during development of the modified rules. They start with the reference deck used for the previous node and update it in collaboration with the EDA company who created that deck. This assures that any changed rules are accurately tested by new and enhanced rule checks.

For all major foundries, the reference rule decks are the Calibre nmDRC decks from Siemens EDA, part of Siemens Digital Industries Software. Any other deck must match the results provided by these reference decks to achieve qualified status.

Q: What is built-in or native DRC?

A : For both digital and custom designs, EDA companies that provide design and/or place and route (P&R) tools include an abbreviated version of a DRC deck that can be used during the design implementation process to quickly check the physical implementation. The violations these P&R DRC engines don't address are typically complex DRC errors, or errors that occur in the late stages of implementation, when it is more difficult to implement layout changes. Such errors often require numerous manual debugging and DRC iterations to fix. Built-in decks typically don't accurately reflect signoff DRC, which means the results they return may not correctly reflect issues that cause the design to fail signoff DRC in the final closure stage.

Q: Why not just always run signoff DRC during implementation/P&R?

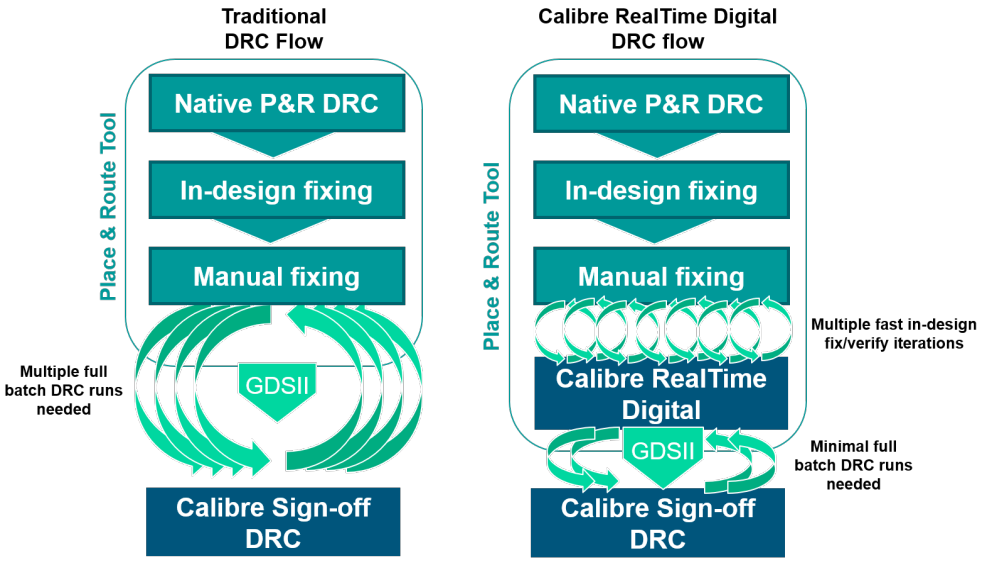
A : To "test" a design implementation against signoff DRC, designers stream out the design OASIS/GDS database, complete a batch run using a qualified signoff DRC tool against the design, debug and fix the resulting errors in the layout, then run another stream out/batch DRC run to verify the changes correctly fix the errors. This can require a lot of time—from multiple hours to a day or more. In addition, many errors are irrelevant because they are caused by the incomplete status of the design. Still, designers must debug all of them, making the time spent identifying irrelevant errors wasted.

For example, most ICs include intellectual property, or IP: pre-built code (such as memory handling) that is sourced from both internal and external suppliers. These IP are inserted into the design in later design stages. Running signoff DRC early generates errors that only exist because these blocks have not been fully connected. Designers can't tell what caused a particular error, so therefore must debug every error.

Q: What are engineers/ designers looking for in DRC capabilities?

A: P&R engineers and IC designers want to create the best and most optimized physical implementation that meets the power, performance, and area (PPA) goals set for each individual design—using the fewest resources and in as little time as possible. A P&R engineer wants to fix DRC errors quickly without compromising the layout quality, which means having access to immediate signoff-quality DRC feedback so they can instantly know if the layout has a problem. Then they need a faster way to debug the complex DRC errors to find and fix the problems and verify the fix is correct. Finally, they want a method to provide what-if analyses for multiple fix options while debugging errors to ensure an optimal fix.

Q: What does the Calibre RealTime Digital tool do differently from a traditional DRC tool?



A: The Calibre RealTime Digital platform changes the traditional DRC closure flow by bringing Calibre nmDRC signoff verification into the P&R environment. By using the same Calibre nmDRC signoff deck and engine used in batch DRC runs, engineers get immediate signoff-quality DRC feedback and can perform multiple check/fix/verify iterations without streaming out databases and running batch DRC verification. They can also run selected groups of checks for targeted checking. Typical Calibre RealTime Digital iterations take a few seconds to minutes, compared to the hours needed for a full batch verification run.

Because this tool provides direct calls to Calibre analysis engines running foundry-qualified signoff Calibre rule decks, they perform fast, incremental checking in the vicinity of shapes being edited for nearly instant feedback on design rule violations and recommended rule compliance. Once an error is found, it highlights the DRC error marker and the IP shapes around the error marker in the P&R tool. This allows designers to fix the error and validate the fix without leaving the P&R environment. They can also perform what-if analyses on design rule violations and recommended rule compliance to find an optimal solution.

Q: What's the payoff?

A: The Calibre RealTime Digital tool enables engineers to catch and fix signoff DRC errors much earlier and faster in the design cycle. P&R engineers can use the time saved to better optimize PPA goals and still significantly accelerate DRC closure cycles, often by as much as 2-4x, getting designs to market faster.