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To provide the most current, accurate, and in-depth technical coverage of the key emerging technologies that engineers need to design tomorrow's products today.

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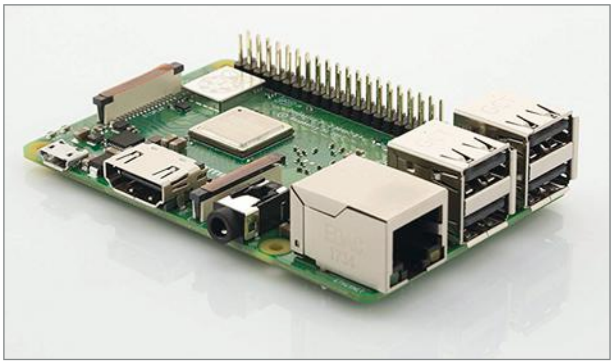

Is Raspberry Pi the Right Platform for Embedded Product Development?

The Raspberry Pi was designed as a platform to teach computer science to students. Given its low cost and wide availability, is it suitable as a platform for commercial embedded products?

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Can 5G Really Live Up to Its Hype, and Why Should You Care?

As the electronics industry gears up for the eventual massive 5G rollout, questions abound regarding everything from small-cell infrastructure to available spectrum to handset development.

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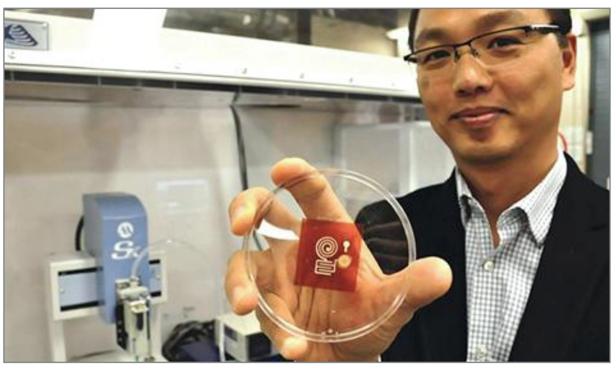

Wood-Based 3D-Printed Sensors Include Wireless Access

Leveraging a previously developed technique, researchers developed sensors that are printed on cellulose and can be read wirelessly using a VNA.

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11 Myths About USB Type-C

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Editorial

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Backdoors are for Houses—Not Security

Attorney General Barr is only the latest to suggest that a "safe" backdoor should be added to products. That's a very, very bad idea.

Security has finally found a place in embedded applications as the Internet of Things (IoT) continues to rise in importance. Hacked systems have been the bane of PCs and smartphones, even as developers try to deliver more secure systems. It's hard enough to prevent attacks like ransomware without having to worry about backdoors.

These days, IoT solutions are hyping end-to-end security. This typically includes secure attestation, authentication, secure communication, and even secure updates. A lot of security layers and protocols are involved, and they're designed to secure a system and possibly isolate any breaches. Knowing that a breach has occurred is useful information by itself when considering the overall security of a system.

A security backdoor is one that bypasses the normal security features of a system. It usually provides unimpeded access and possibly control of a system. This can be handy for debugging it's and often why developers include one, but they should never be left in a shipping system. Unfortunately, many systems have been attacked through such a backdoor. Developers often have done very dumb things like simple, hard coded passwords.

Granted, creating a secure backdoor could be possible, but it essentially places two security systems within a product. An attacker simply needs to bypass one of these to gain control. While the front door protection will usually be robust, the same can't be said for the backdoor, which is also secret. Security through obscurity is generally a bad idea.

Anyone who knows anything about security will tell you that backdoors are an extremely bad idea. Those that ignore security experts will be in for very bad surprises.

Unfortunately, Attorney General William Barr is just the latest to call for backdoors. He said, "Don't give me that crap about security, just put the backdoors in the encryption." Forcing this through legislation has been suggested as well. It could only end badly.

Good security is built on layers that have been tested and designed to work together. The latest systems are designed from the ground up for security, starting with private encryption keys that never exist outside of the chip. Secure boot is simply the next step of the process. All of this security, hardware, and protocols are designed to prevent specific types of attacks. There are many ways to attack a system, and it only takes one success to cause major headaches.

There are ways to provide hierarchical security within many systems, but that's by design. Backdoors bypass this design. It will be even worse if a backdoor gets added after the fact.

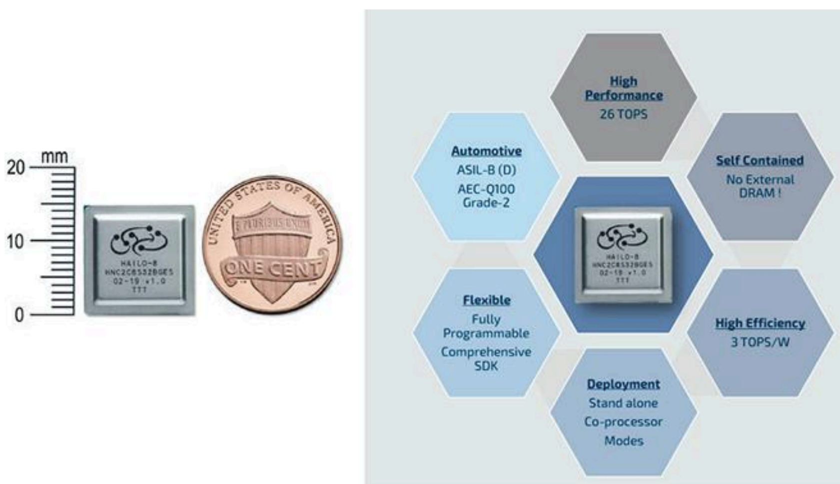
Another problem with backdoor security is that those who feel secure because of the primary security system have been deluded. The premise for a backdoor is that the "good guys" can do things the "bad guys" will not know about. Unfortunately, that's often not the case—the backdoor can be used for nefarious reasons regardless of who is controlling the backdoor. Gaining access by compromising a backdoor system or attacking a poorly designed one results in a system that's not only hacked, but the security layers designed to isolate other attacks are completely bypassed.

The bottom line is that backdoors should not be included in any system, and everyone should understand why. There's no secret sauce that will make a backdoor safe. Don't let anyone try to convince you otherwise. ed

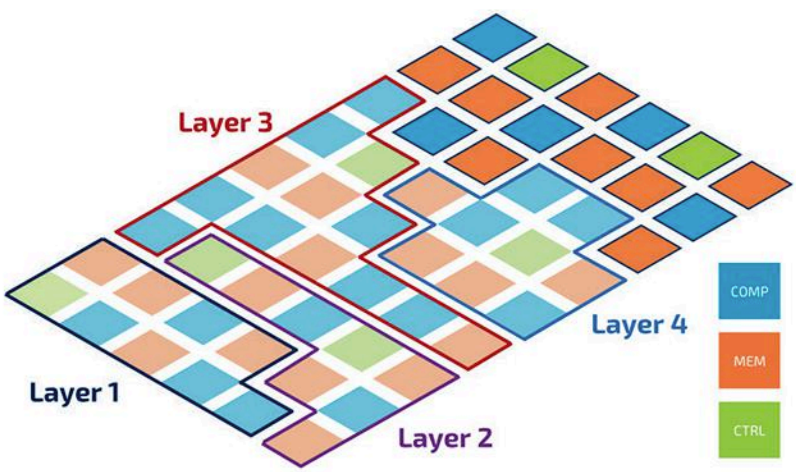
News

MACHINE-LEARNING CHIP

Takes on Rugged Apps—from Cars to Wearables



1. Hailo Technologies' Hailo-8 is a compact chip designed for rugged environments, including automotive applications.



2. The Hailo-8 can distribute multiple layers of an ML model across its collection of compute (COMP), memory (MEM), and control (CTRL) blocks.

It's possible to incorporate machine-learning (ML) and artificial-intelligence (AI) methodologies at the edge, where many compact, embedded IoT devices live using standard processors and SoCs. However, this limits the functionality that can be provided due to computational limitations. Utilizing specialized AI accelerators is a requirement when tackling problems such as image recognition with streaming video.

Hailo Technologies, based in Tel Aviv, has created the Hailo-8 (*Fig. 1*), a compact chip designed for rugged environments including automotive applications. It offers significantly higher performance while using less power than many GPGPU-based solutions. Consuming less than 1.7 W, it can deliver a 682-frame/s processing speed for the ResNet-50 benchmark with 224-by 224-pixel resolution, 8-bit precision, and a batch size of 1. Small batch sizes are important on the edge.

The Hailo-8 distributes multiple layers of an ML model across its collection of compute, memory, and control blocks *(Fig. 2).*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18 Debbie Brady, Manager, User Marketing — Date 9/3/19

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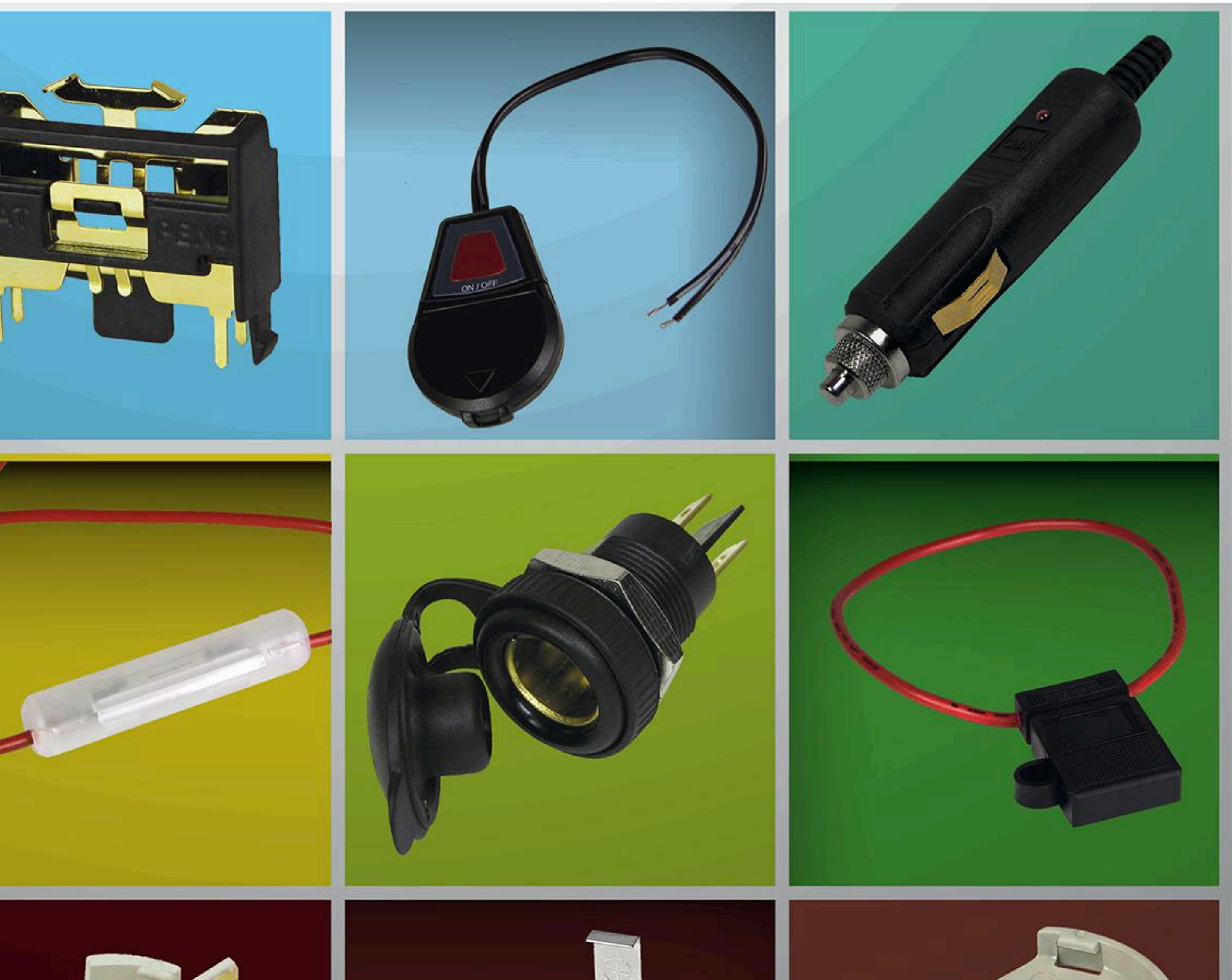
The Hailo-8 distributes multiple layers of an ML model across its collection of compute, memory, and control blocks (*Fig. 2*). An interconnect provides FPGA-like configurability, allowing the Hailo-8 to process one or more models at the same time.

In addition, Hailo crafted the Hailo-8 development board (*Fig. 3*), a Developer Suite, and software development kit (SDK). The SDK supports ONNX and TensorFlow. It handles automatic numerical conversion and emulation with profiling support.

3. The Hailo-8 development board, Developer Suite, and SDK are available to select customers.

The Hailo-8 can act as a host driven by sensors with a MIPI or parallel interface. The system is able to use SDIO or Ethernet to communication with other systems. Furthermore, an application processor can take advantage of the Hailo-8 with these interfaces as well as a PCI Express (PCIe) interface.

Sample chips are available now with production in 2020. The chip will be ASIL-B certifiable. ■



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APPLE'S A13 PROCESSOR Powers Its Latest iPhone Lineup

APPLE ROLLED OUT its latest line of iPhones with a new A-Series SoC that boosts performance by 20% and lowers power up to 40% over the previous year's phones, powering bigger and better cameras and adding hours to the iPhone's battery life. The launch comes as the Silicon Valley electronics giant looks to get out of a prolonged slump in iPhone sales, as consumers hold onto their high-end handsets longer than ever before upgrading.

Apple's A13 Bionic runs in the $699 iPhone 11, which costs $50 less at launch than the entry-level iPhone 10. The chip is also slapped inside the $999 iPhone 11 Pro, which adds another camera to create a three-camera system, and the $1,099 iPhone Pro Max. The chip has more built-in artificial intelligence capabilities that are central to the new iPhone's ability to shoot better photos and videos and offer faster facial and voice recognition.

The move highlights Apple's advances in custom chip design and how the company is trying to appeal to customers ahead of launching its 5G iPhones, which are expected to come out in 2020. Sri Santhanam, vice president of Apple's silicon engineering group, detailed the A13 on stage at Apple's iPhone 11 product launch event. Kaiann Drance, senior director of iPhone marketing, claims the A13 is the fastest CPU and GPU in any smartphone today.

The A13 processor moved to a more advanced 7-nm node than last year's A12 Bionic. Apple tends to jump to the front of the line for the most advanced and costly chip production process from TSMC, the world's biggest made-to-order chip maker, which also makes chips for China's Huawei. The new chip contains has 8.5 billion transistors—20% more than the previous A12 processor's 6.9 billion, which was 60% more than the A11 Bionic's 4.3 billion.

The company's new A-Series SoC contains a six-core central processing unit (CPU), including four high-efficiency cores that are 20% faster or consume 30% less power than last year's iPhones. The A13 processor also has a pair of high-performance CPU cores that are designed to be up to 20% faster or 40% lower power for running through more rigorous computations. Apple also designed the A13's image signal processor (ISP) to connects to the camera.

Overall, the central processor inside Apple's A13 can perform a trillion operations per second (TOPS).

Overall, the central processor inside Apple's A13 can perform a trillion operations per second (TOPS). Crammed inside the CPU are AI accelerators that can handle the core mathematical operations of machine learning. It also incorporates an eight-core Neural Engine for running AI chores inside the iPhone 11 instead of the cloud, reducing delays and potentially adding to privacy. The A13's Neural Engine is 20% faster and 15% lower power than the A12's.

Apple also has expertise developing high-end graphics processing units (GPUs) in the iPhone. The A13 processor features a custom four-core GPU that runs 20% faster or consumes 40% less power so that iPhone customers can play games with higher-resolution graphics. Another slice of custom silicon in the A13 sends AI chores to the CPU, GPU or Neural Engine depending on the area of the chip that can strike the best balance of speed and efficiency.

The A13 processor is also designed to make the iPhone's camera more capable. Phil Schiller, Apple's senior vice president of marketing, called it the cornerstone of the advanced camera system in the high-end iPhone Pro. The rear of the iPhone Pro features three cameras—wide angle, telephoto, and a new ultrawide angle—that can work together to produce better photos. Apple also said it had given the iPhone Pro ability to brighten photos taken in the dark.

Apple introduced its Deep Fusion technology, which will ship with iOS 13. It works by shooting photos from the Pro's three cameras and then combining them into one shot, using the Neural Engine to enhance textures, scrub out blurriness and sharpen details. Apple also added the ultrawide angle camera to its entry-level iPhone 11. The dual camera can take advantage of the A13 to shoot sharper portraits than 2018's iPhone XR, which has one camera.

Schiller underlined how much longer the batteries inside the new iPhones will last with the A13. The entry-level iPhone averages an additional hour of battery life over the iPhone XR, while the iPhone Pro adds around four hours of battery life compared to last year's iPhone XS. The iPhone Pro Max can last five hours longer than the iPhone XS Max. Apple also said it had added Wi-Fi 6 support in the new iPhones, which feature 4G connectivity up to 1.6 Gb/s. ■

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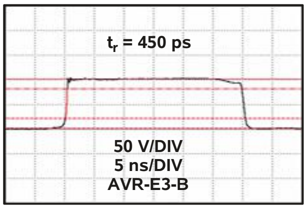

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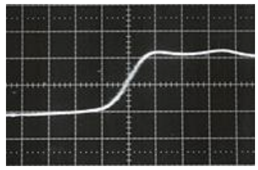

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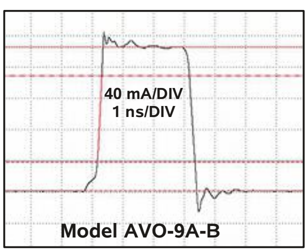

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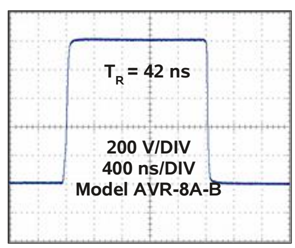

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QUALCOMM TO ADD 5G Modems to More Affordable SoCs

QUALCOMM PLANS TO EXPAND its 5G cellular modems to more affordable apps processors in an effort to make 5G smartphones available at cheaper prices. The move could help connect billions of consumers to 5G networks, which offer far faster data transfers and lower latency than 4G LTE technology today.

Qualcomm is already selling discrete modem chips to Samsung and other customers for early 5G smartphones, which are priced at a premium. These phones tend to take advantage of Qualcomm's Snapdragon 8 Series SoCs, which are usually used in the highest-end handsets. Samsung uses Qualcomm's Snapdragon 855 SoC in its flagship Galaxy S10 5G, which costs $1,300 compared to $900 for the 4G model.

Qualcomm plans to integrate its 5G modems in its mid-range Snapdragon 6 Series and 7 Series SoCs, which are staples in 4G smartphones that sell for $200 to $400. That could curb the high cost of most 5G smartphones on the market. The new Snapdragon 7 Series should be added to 5G devices by the first quarter of 2020, while the 5G Snapdragon Series 6 processor will start shipping in products by the second half of 2020, Qualcomm said.

Alex Katouzian, Qualcomm's senior vice president and general manager for mobile, said that adding 5G to its more affordable chips would speed the global rollout of 5G technology. The San Diego, California-based company said 2.2 billion users could upgrade to 5G gadgets using the cheaper chips. More than 10 smartphone makers plan to use the Snapdragon 7 Series SoCs, including LG Electronics, Motorola and Chinese OEMs Vivo and Oppo.

"5G network rollouts are progressing much faster when compared to 4G," said Steve Mollenkopf, Qualcomm's chief executive officer, on an analyst conference call in July. He said that more than 20 operators are currently rolling out 5G networks globally and more than 20 smartphone makers are developing 5G devices. He added that all 5G coverage in China would be roughly equal to the scale of a major U.S wireless operator by the end of 2019.

Qualcomm is trying to hold onto its lead in 5G technology, which it hopes will breathe new life into the stagnating handset space. Qualcomm, which controls close to 50% market share in cellular baseband chips, is the primary provider of 5G modems for the first 5G smartphones rolled out by Xiaomi, LG Electronics, ZTE and others. More than 150 designs are in development with its X50 and X55 modems as well as its 5G SoCs, Qualcomm said.

But other modem chip designers are getting set to challenge Qualcomm's dominance in 5G. Trying to expand its footprint in premium phones, Mediatek in May introduced an integrated multimode 5G SoC that supports 2.5 Gb/s upload and 4.7 Gb/s download speeds in the sub-6-GHz and 2.5 GHz frequency bands. Mediatek's SoC uses TSMC's advanced 7-nanometer node. It is expected to enter mass production in the first quarter of 2020.

Huawei is shipping its first discrete multimode 5G modem, the Balong 5000, in some of its phones. China's leading smartphone vendor also plans to start adding an integrated 5G SoC to its high-end handsets by the end of the year. The chipset, produced on the 7-nanometer node and designed by Huawei's semiconductor subsidiary HiSilicon, can handle up to 1.25 Gb/s upload speeds and 2.3 Gb/s download speeds in the sub-6-GHz frequencies.

Huawei, which has been hurting Qualcomm with its massive market share gains in China, plans to use the integrated 5G SoC in its flagship handset, the Mate 30. But the smartphone may not be able to launch with access to Google's Android operating system or any of Google's popular apps due to U.S. sanctions slapped on the Chinese telecom equipment maker in May. That could severely hamper sales of the new smartphone.

However, Qualcomm holds a key advantage over other players in the $21.5 billion modem chip market, analysts say. The company's chips can cover the full range of frequency bands used by 5G, including sub-6-GHz bands favored in Europe and China for early 5G deployments. They can also handle millimeter waves, which have a shorter range than sub-6-GHz bands and can even be deflected by your hand holding your smartphone but higher capacity. ■

KURT WATTELET | Product Line Manager Overvoltage Components/Surge Protection Devices, Bourns Inc.
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Redesign Overvoltage Protection to Bolster Reliability and Safety

Different circuit-protection technologies are used to overcome metal-oxide-varistor limitations in certain harsh environments. A novel hybrid approach ups the reliability and safety ante to meet application demands.

To ensure reliability and safety for devices that run on ac and dc power lines, circuit protection is a definite design requirement. Unfortunately, there's no universal protection solution. Varying levels of exposure to lightning and switching transients, poor line voltage regulation in rural and developing areas, and inconsistency among different grids make a common solution impossible. And, higher-density, higher-performance designs add to the challenge in addressing all circuit-protection device needs. While the UL 1449 standard for surge protective devices (SPDs) outlines the requirements for certification, this too doesn't provide the basis for a single circuit-protection solution.

This article evaluates standard metal-oxide-varistor (MOV) device performance and documented failure modes in a variety of overvoltage conditions. It presents the types of circuit-protection technologies required to overcome MOV degradation and failure issues.

EXISTING OVERVOLTAGE PROTECTION

Designers of power supplies, power systems, line voltage, telecom systems, and white goods have long used MOVs

Designers of power supplies, power systems, line voltage, telecom systems, and white goods have long used MOVs to guard applications from overvoltage transients such as lightning, power contact, and power induction.

to guard applications from overvoltage transients such as lightning, power contact, and power induction. As a radial leaded varistor device that provides bidirectional protection, MOVs are popular due to their high current handling, high current absorption, and fast reaction times.

A downside to using MOVs is that they're known to degrade and possibly fail over time. As the MOV ages, the maximum continuous operating voltage it can withstand will decrease. A MOV exposed to long-term overvoltage surges or high temperatures can go into a failure mode that starts with excessive leakage current, which leads to power dissipation, and eventually can cause application damage due to watt loss heating.

That's why UL requires testing to safeguard designs against these harmful failure modes. Engineers have learned certain applications that are subjected to voltage transients require more protection than a MOV alone can provide.

BAND-AID SOLUTIONS

Designers also commonly employ thermally protected MOVs such as TMOVs (TMOV is a registered trademark of Littelfuse Inc.) for ac power protection. This type of MOV has a thermal fuse that disconnects the MOV from the power source when it reaches an elevated, but safe, temperature.

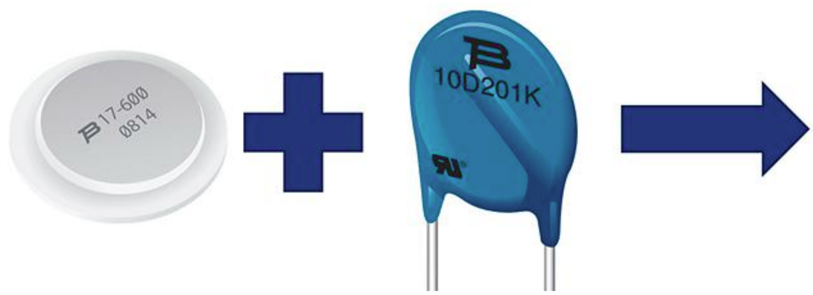
However, they don't prevent the leakage current that drives the power dissipation in the off-state; it simply functions to stop a very dangerous failure mode. Most thermally protected MOV fuses are only tested to 10 A in the UL 1449 limited current abnormal overvoltage test. They may not have the ability to open an actual ac line capable of delivering over 100 A.

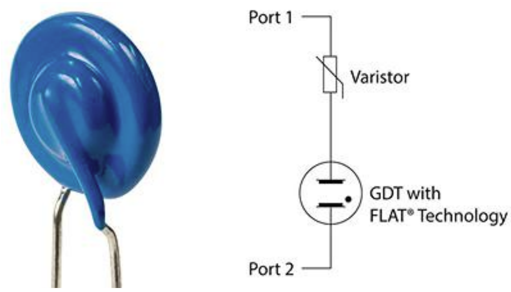
An important function to consider is that when a thermally protected MOV disconnects itself from the power line, it's no longer protecting the equipment. While some feature an indicating lead that can be used to sense a line disconnect, this added circuitry increases the protection scheme cost but doesn't actually increase the device's overall protection.

To lower the chances of a "thermal event," some designers choose to select an MOV with a voltage rating far above the application's normal operating voltage. This approach does reduce the stress and slows a MOV's aging process, but its higher voltage rating also means the clamping voltage of the MOV will also be much higher. This may force the designer to select higher-voltage-rated (and more expensive) products downstream as they must be rated to survive the higher voltages let through during a surge event.

ACHIEVING ENHANCED PROTECTION

Since standard MOVs alone, TMOVs, and higher-voltage-rated MOVs have their limitations for many applications, a different circuit protection approach is needed. One viable solution combines a MOV and a gas discharge tube (GDT)





1. Bourns combines its space-saving GDT, which leverages the company's FLAT technology, with a MOV, creating a compact, enhanced overvoltage protector that's a drop-in replacement for standard 14- and 20-mm MOVs.

into a hybrid component. Providing a space-saving circuit protection device, the two technologies can be packaged in a familiar MOV radial package, thus providing a drop-in replacement option *(Fig. 1)*.

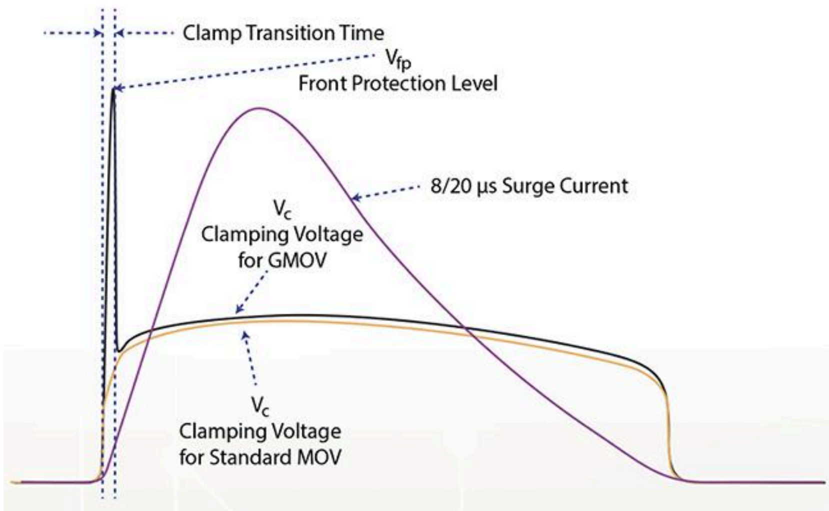
Putting a MOV and a GDT together offers lower leakage over the life of the MOV, resulting in a predictable failure mode and eliminating harmful watt loss heating. With this approach, the line voltage appears largely across the extremely low-leakage GDT under normal operating conditions. This essentially disconnects the MOV from the ac line and protects it from small transients that pose no threat to the protected equipment that would otherwise only serve to age the MOV.

During a surge event, the GDT quickly (in less than a microsecond) switches on and connects the MOV across the line to clamp the surge voltage to acceptable levels. Once the surge event passes, the line voltage falls across the MOV, switching off the GDT. Once the GDT is off, it in-turn disconnects the MOV from the line as before. The symbiotic functionality of the GDT and MOV working together delivers a longer application life with a higher level of reliability. See how the protection characteristics of a GMOV component are defined in *Figure 2*.

Combining a GDT with a MOV doesn't impact signal or system operation. The low capacitance of the GDT assures that the hybrid overvoltage protector will not interfere with high-speed data run over ac or dc power lines. Plus, there's no longer a need to include indicating circuitry and its added costs because the combined MOV and GDT device doesn't have a thermal fuse.

UL 1449 CERTIFICATION

The UL 1449 lost neutral test demonstrates the value of taking a hybrid approach—adding a properly selected GDT to the design provides improved performance in lost neutral testing. For example, choosing a UL 1449 listed overvoltage protector saves time and cost for both the design and certification phases of product development, eliminating the guesswork in finding the right combination of discrete parts. Because the Bourns GMOV device is UL listed as a Type 5 SPD, as is a MOV, it offers an alternative that requires minimal requalification.



2. The protection characteristics of the GMOV component are defined by Front Level Protection (V_{fp}) and Clamping Voltage Level (V_c), where V_{fp} is measured as 10% of peak current in accordance with IEC 61051-1. Note that V_{fp} is a very short event, lasting less than 0.3 µs, and represents the time it takes for the GDT to turn on. V_c is the GMOV components' clamping voltage level, which is the total of the MOV clamping voltage and the on-state arc voltage of the GDT. V_c occurs after the GMOV component has transitioned into its full on-state.

ADVANTAGES FROM REDUCED LEAKAGE CURRENT

Exposure to line irregularities over time and from multiple surges can reduce circuit-protection effectiveness. Leakage current associated with some protection schemes can't be tolerated by certain applications. Using a new hybrid MOV and GDT overvoltage protection solution such as the Bourns GMOV device delivers the lower leakage current and reduced capacitance that solves these issues.

Energy Star applications also benefit from reduced leakage current, specifically under voltage stress conditions. The reduced leakage current and constant capacitance level advantages offered by a combined MOV and GDT device enable power-line communications to operate reliably at higher data rates.

PROTECTING NEXT-GENERATION DESIGNS

With power systems increasingly exposed to a variety of transient events, discrete MOV technology becomes more susceptible to premature failure and thus negatively impacts equipment reliability. New overvoltage protection that overcomes these issues is now possible. Pairing MOVs and GDTs leverages the best attributes of both protection technologies, offering zero standby energy consumption and no degradation from watt-loss heating. Such a solution extends the life of the MOV while making the system more reliable and safer in the process. ed

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SHAWN PRESTRIDGE | Senior Field Applications Engineer, IAR Systems

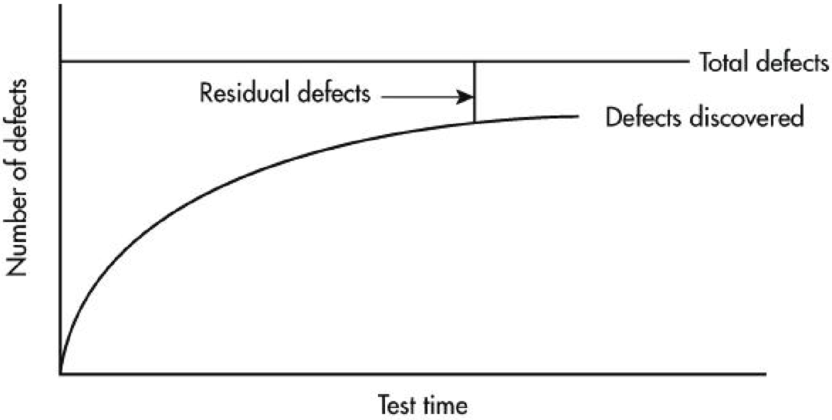
DEBUGGING Starts with Code Quality

Save time on your projects by using coding standards and static analysis to help improve your code quality in the beginning, so you spend less time debugging at the end.

"You will see a few warnings when you compile the code; you can safely ignore those," the engineer claimed confidently. He had contacted me the previous day stating that he had found a bug in our Embedded Workbench compiler, and just sent me his entire project rather than a simple example to replicate the supposed issue.

When I compiled the project on my machine, "a few warnings" was actually 402 warnings, to be more precise. After sifting through the warnings, I found one that was the source of the problem. The warning message for this line of code stated, "Undefined behavior: Order of volatile accesses not guaranteed". What the warning message was trying to tell both of us is that the way the engineer wrote the code was getting into a dark corner of the C language specification that actually wasn't defined. So, when the arguments to a function call are volatile accesses to variables or are nested function calls themselves, the compiler can choose the order in which the different accesses are performed.

To wring the most performance out of the code, the compiler may choose to not go simply left-to-right in the accesses, but rather reorder them if it can make the code tighter and/or faster, depending on the optimization selected by the user. The way that the engineer wrote the code depended on left-to-right accesses for the code to function properly. I showed him how to rewrite the code so that all compilers would interpret it the same way—and more importantly—it would function the way he expected.



Not much test time is needed to find defects at the beginning of a project, but it usually takes quite a bit of testing to find a defect later in the development lifecycle.

BEWARE BUG BITES

This situation reinforced a maxim that I've used in my professional career: Warnings are bugs just waiting to bite you. Therefore, you should always attempt to clean up every warning in your code by understanding why the warning was issued and what it's really trying to tell you. With this in hand, you're better equipped to make the appropriate changes in your application

so that your code is more robust.

However, compilers and linkers typically don't examine your code in much detail. Consequently, simply having zero warnings when you build isn't enough to engender confidence in the defect level of your code. Rather, it's a first step to making your application easier to debug. A more thorough analysis of the code is necessary to avoid common pitfalls that developers fall into as well as to avoid some of the undefined behaviors of the C and C++ language that were mentioned previously. In other words, you need to get serious about code quality.

Developers commonly use two approaches to get high levels of code quality: coding standards and static-analysis tools. Employing both of these in conjunction with testing will not only make your code as defect-free as possible, but it can actually foreshorten time-to-market by allowing you to meet your application's release criteria much more quickly.

"The later you find a bug, the more expensive it is to fix." We have all heard this platitude so many times that we never question its veracity. But have you ever stopped to wonder why this is so? To reveal this, let's take a look at a typical mean-time-to-failure (MTTF) curve *(see figure)*.

As you can see, when you first start testing an application it's easy to find quite a few defects. As the software matures, it takes more and more testing time to find the next defect. The reason that it's more expensive to fix a bug later in the test cycle is that it artificially skews your curve, making it take even more test time to meet your company's release criteria. Therefore, the earlier you find the defect in testing, then the less impact it has on the project schedule and is "cheaper" to fix.

But what if you could foreshorten the amount of testing time by reducing the number of defects in your code? That's where code quality can help you. By enforcing coding standards and using static analysis, you can eliminate defects while desk-checking your code. Once you check code into a build, then every defect counts against your release metrics. However, if you find it before then, it's like the bug never even happened!

STANDARD PROCEDURE

Now that we know why code quality is important, let's look at the two common ways to achieve this. The first way is by implementing a coding standard. Many organizations have coding standards that set forth things like how variables and functions are named, calling conventions, how comments are structured, etc. Some go so far as to limit the actual size of each individual piece of source. The idea is to increase readability during code walkthroughs to make it easier to find defects and to improve maintainability.

These are all great goals and should be part of a standard, but there are standards that go beyond this level. One of the most popular is MISRA C. MISRA stands for the Motor Industry Software Reliability Association, which—as the name implies—was born out of the automotive industry to promote safe and reliable embedded coding practices. However, many other industries such as avionics, medical, industrial controls, and even consumer products have co-opted these rules for their usage. That's because the standard tries to remove all of the undefined behaviors in C as well as prevent users from engaging in "risky" programming practices that are error-prone. For example, look at this code snippet:

```
if((a==b)&&(c--)){...}
```

What's wrong with it? You probably don't see the subtle behavior, and that's the issue that MISRA C is trying to avoid. The issue with this statement is that the decrement of c **only** happens if a equals b. While it may be that you fully understand that behavior and it's what you intended, you're betting that anyone who reviews or maintains your code understands that as well. It's easy to miss and easy to get wrong, which is why MISRA C won't allow this kind of behavior—it can easily add to your bug tally. Here's another example:

```
a == 3 || b > 5
```

What has precedence? It's hard to remember, which is why MISRA C forces logical ANDs and ORs to be primary expressions by forcing you to wrap them in parentheses like:

```
(a == 3) || (b > 5)
```

It's clearer and easier to read. Parentheses are free in code—use them liberally! Depending on which flavor of MISRA C you use (1998, 2004, or 2012), there are up to 226 different rules like this that help you avoid common mistakes in your code and therefore reduce the number of defects found during formal testing, therefore it drastically reduces the amount of debugging your application requires. There is even a MISRA C++ to help you code safely in C++!

STATIC ANALYSIS

The second approach to improving code quality is to do static analysis of

your application. Most static-analysis tools can check your code for MISRA C/C++, but the better tools go beyond that. For example, the C-STAT static-analysis tool in IAR Embedded Workbench adds a few hundred other rules that are pulled from a variety of other sources, like the Common Weakness Enumeration (CWE) from Mitre.

The CWE is a list of some of the most common sources of defects in application code compiled by exhaustive research from the folks at Mitre. For instance, they recommend against doing comparisons of floats with == or != operators or using a divisor without having a check for non-zero. More sophisticated static-analysis tools like C-STAT can also find paths through the code where you're dereferencing a NULL pointer—and show you the path through the code that makes that pointer be NULL when the dereference occurs. They can do the same thing for uninitialized variables, too.

In addition, the CWE guards against misusing a pointer by directly accessing a member of a struct by using an offset from the struct. If you change the struct, it can easily cause a litany of bugs in your code, all of which will delay your project's release. These are just a small sample of the defects that static analysis can help you find. Removing these issues improves your code quality, and thus reduces the amount of required debugging.

So, what happened to the engineer I mentioned at the beginning of the article? I told him about my maxim of warnings-as-bugs and advised him to spend some time cleaning them up to improve his code quality. He said he would and thanked me for my help. About a week later, he ran into another issue and asked for help. He said he would send me a new code dump and then surprised me by stating that he had cleaned up all of the warnings! I was very pleasantly surprised until I received the new code dump and realized that he had chosen to suppress the warning diagnostics during the build. Some people never learn, but I like to think that we can all be taught new tricks.

If you want to spend less time at the end of your project debugging, then spend a little more time at the beginning of your project using coding standards and static analysis to help you improve your code quality. As Ben Franklin opined famously, "An ounce of prevention is worth a pound of cure." ed

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WILLIAM WONG | Senior Technology Editor

Attacking the Memory Bottleneck

Is it time to go serial for the memory interface in servers? Microchip and IBM think so.

The Open Coherent Accelerator Processor Interface (OpenCAPI), announced at the Flash Memory Summit, is managed by the OpenCAPI Consortium. It's a new high-performance bus interface designed for servers that now has memory semantics in the form of the Open Memory Interface (OMI). The big difference between it and the standard memory interfaces for DRAM is the switch from parallel to serial in the same fashion that PCI Express (PCIe) replaces the parallel PCI bus. The consortium was started by AMD, Google, IBM, Mellanox Technologies, and Micron.

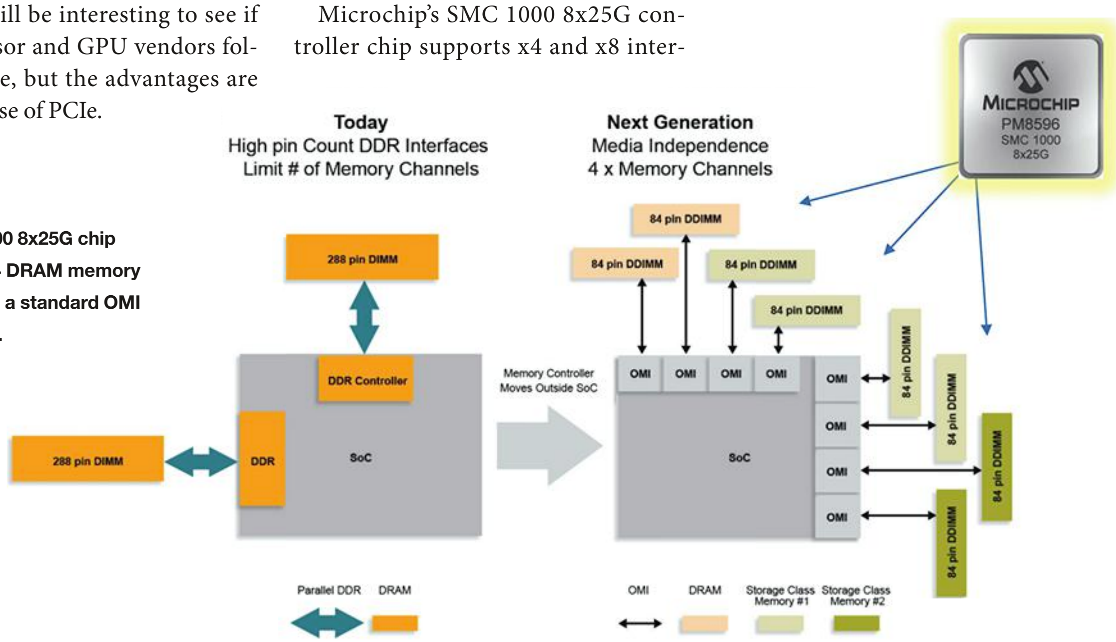
Last year, IBM announced that new Power9 processors would incorporate an OpenCAPI interface for memory support. It will be interesting to see if other processor and GPU vendors follow this route, but the advantages are similar to those of PCIe.

Microchip is at the forefront of delivering on storage needs. The SMC 1000 8x25G PM8596 chip acts a front end to memory using an OMI interface *(Fig. 1)*. One big difference between the conventional parallel interface and the serial OMI is that the interface is platform agnostic. OMI has an abstraction layer; therefore, a controller can attach to different types of media.

The typical DDR4-3200 memory channel requires over 300 pins and has a bandwidth of 25 GB/s. A single OMI memory channel uses about 75 pins and can deliver the same 25-GB/s throughput. The 4x OMI system employs about the same number of pins as the parallel interface, but it has a 100-GB/s bandwidth or an increase of a factor of four.

Microchip's SMC 1000 8x25G controller chip supports x4 and x8 interfaces with 25.6-Gb/s serial links using OIF-28G-MR support. This includes dynamic low-power modes. Housed in a 17- by 17-mm package, it can interface to NVDIMM-N persistent-memory modules as well as a range of 16-Gb DDR4 memory with up to four ranks. The on-board, open-source firmware handles DDR/OMI initialization and provides in-band temperature and error monitoring support as well as support for the ChipLink GUI.

The SMC 1000 8x25G provides security and data-protection services, too. It can support hardware root-of-trust, secure boot, and secure update. Also included is single-symbol-correction/double-symbol-detection ECC support. The chip can handle memory scrubbing with auto correction of errors.



1. The SMC 1000 8x25G chip supports DDR4 DRAM memory while providing a standard OMI serial interface.

FREE WEBINAR

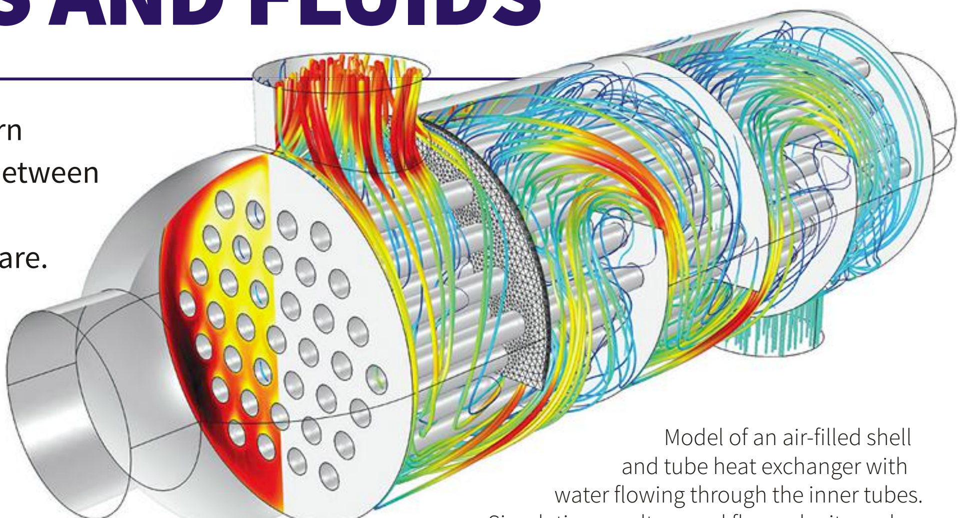
October 29, 2019 | 2:00pm EST

Registration URL: https://www.electronicdesign.com/webcasts/simulation-heat-transfer-solids-and-fluids-webinar

SIMULATION OF HEAT TRANSFER IN SOLIDS AND FLUIDS

Tune into this webinar to learn how to model heat transfer between solids and fluids using the COMSOL Multiphysics® software.

We must consider thermal characteristics in product development. One example is systems that include temperature control combining conduction in solids and convection in fluids.



Model of an air-filled shell and tube heat exchanger with water flowing through the inner tubes. Simulation results reveal flow velocity and temperature distribution within the vessel.

In this webinar, we will discuss heat transfer between solids and fluids and highlight examples with convection, radiation, and conduction; electromagnetic heating; and structural thermal expansion. You will also get a live demonstration of modeling heat transfer in COMSOL Multiphysics® and creating an app with a customized user interface based on the model.

You can ask questions at the end of the webinar during the Q&A session.

SPEAKER: Nicolas Huc, Product Manager, Heat Transfer Module, COMSOL

Nicolas Huc joined COMSOL France in 2004 and is currently the head of their development team. He is also the manager of the Heat Transfer Module. Nicolas studied engineering at ENSIMAG before receiving his PhD in living system modeling from Joseph Fourier University.

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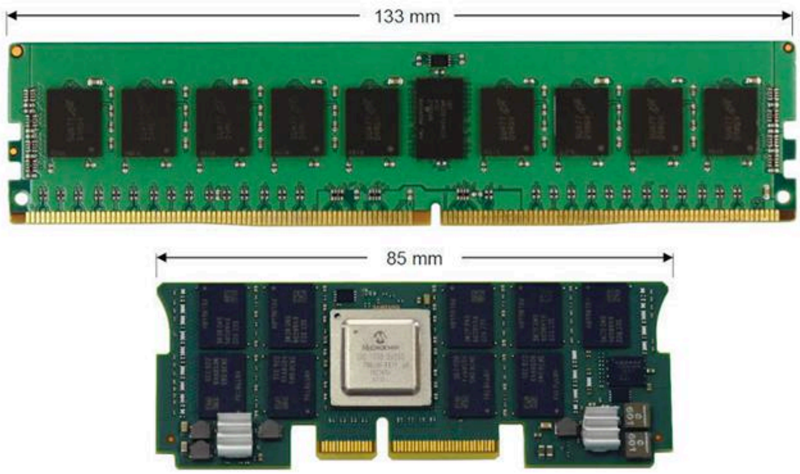
The DDIMM form factor *(Fig. 2)* provides a point-to-point 8x25G OMI memory interface. These DDIMMs support DDR4 DRAM memory. DDIMM modules are available from a number of vendors, including SMART Modular, Samsung Electronics, and Micron, in multiple capacities from 16 GB up to 256 GB.

Using the OMI approach brings advantages with it, such as higher bandwidth and lower pin counts. Normally, load/store operations are queued by the memory controller within the processor. In this case, the memory controller is integrated within the SMC 1000 8x25G. Microchip's product has innovated in the area of device latency, so that the difference in latency between the older parallel DDR interface and this newer OMI serial interface is under 4 ns when compared to LRDIMM latency.



2. This DDIMM form factor is designed to support a range of volatile and non-volatile storage chips.

The OpenCAPI consortium has made the host and target OMI IP component technology available to consortium members on a royalty-free basis. This should further adoption, as will processor, GPU, and FPGA implementations that take advantage of it. Likewise, embedded applications could be ripe for this type of interface, especially single-channel implementations where reduced pin count would be advantageous. Computing on the edge is demanding more, higher-performance memory. ed

24 GHz to 44 GHz Wideband Integrated Upconverters and Downconverters Boost Microwave Radio Performance

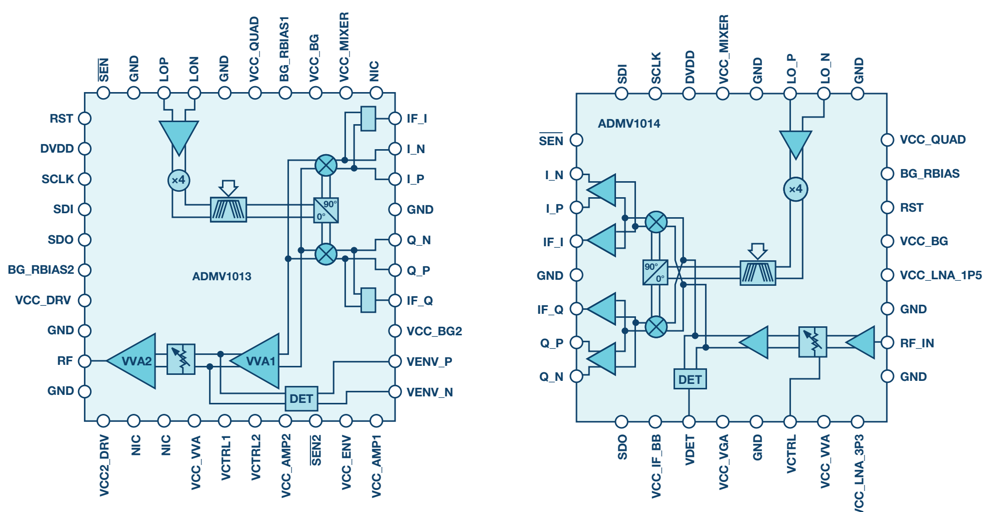
James Wong, Kasey Chatzopoulos, and Murtaza Thahirally
Analog Devices, Inc.

Analog Devices launched a pair of highly integrated microwave upconverter and downconverter chips, the ADMV1013 and the ADMV1014, respectively. These ICs operate over a very wide frequency range with a 50 Ω match from 24 GHz up to 44 GHz and they can support more than 1 GHz instantaneous bandwidth. The performance attributes of the ADMV1013 and ADMV1014 ease the design and implementation of small 5G millimeter wave (mmW) platforms that cover the popular 28 GHz and 39 GHz bands in backhaul and fronthaul, as well as many other ultrawide bandwidth transmitter and receiver applications.

Each upconverter and downconverter chip is highly integrated (see Figure 1), and comprised of in phase (I) and quadrature phase (Q) mixers with on-chip quadrature phase-shifter configurable for direct conversion to/from the baseband (operable from dc to 6 GHz) or to/from an intermediate frequency (IF) that can operate from 800 MHz to 6 GHz. The upconverter RF output has an on-chip transmit driver amplifier with a voltage variable attenuator (VVA), while the downconverter's RF input contains a low noise amplifier (LNA) and gain stage with a VVA. Both chips' local oscillator (LO) chains consist of an integrated LO buffer, a frequency quadrupler, and a programmable band-pass filter. Most of the programmability and calibration functions are controlled via an SPI interface, making the ICs easily software configurable to a performance level that is unmatched.

An Inside Look at the ADMV1013 Upconverter

The ADMV1013 offers two modes of frequency translation. One mode is direct upconversion from baseband I and Q to RF. In this I/Q mode, the baseband I and Q differential inputs can accept signals from dc up to 6 GHz that is, for instance, generated from a pair of high speed transmit digital-to-analog converters (DACs). These inputs have a configurable common-mode range; thus, they can accommodate the interface requirements of most DACs. The other mode is single-sideband upconversion to RF from complex IF inputs such as those signals generated by a quadrature digital upconverter device. Unique to the ADMV1013 is its



(a) ADMV1013 Upconverter Chip Block Diagram

(b) ADMV1014 Downconverter Chip Block Diagram

Figure 1. (a) The ADMV1013 upconverter chip block diagram. (b) The ADMV1014 downconverter chip block diagram.

capability to allow digital correction of the I and Q mixers' dc offset error, resulting in improved LO leakage to the RF output. Achievable LO leakage after calibration can be as low as –45 dBm at the RF output, at maximum gain. The ADMV1013 allows users to digitally correct for the I and Q phase imbalance through register tuning. In normal operation, the upconverter exhibits an uncalibrated sideband suppression of 26 dBc, which can be improved to about 36 dBc after calibration. Additional suppression can be achieved by further adjusting the phase balance of the I and Q DACs at baseband in the I/Q mode. These performance enhancement features minimize external filtering while improving radio performance at microwave frequencies. With the LO buffer integrated, the part requires only 0 dBm drive. Thus, the device can be conveniently driven directly from a synthesizer with an integrated voltage controlled oscillator (VCO) like the ADF5610, further reducing external components. The on-chip frequency quadrupler multiplies the LO frequency to the desired carrier frequency and is passed through a programmable band-pass filter to reduce the undesired multiplier harmonics. The modulated RF output is then amplified through a pair of amplifier stages with a VVA in between. The gain control provides a user adjustment range of 35 dB, with a maximum cascaded conversion gain of 23 dB.

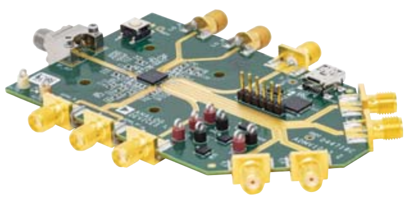


Figure 2. The ADMV1013 in a 6 mm × 6 mm surface-mount package shown on its evaluation board.

An Inside Look at the ADMV1014 Downconverter

The ADMV1014 also has similar elements on the LO chain. The ADMV1014 has an LNA in its RF front end, followed by a VVA and an amplifier. A continuous 19 dB gain adjustment range is controlled by a dc voltage. Users have the option to use the ADMV1014 in I/Q mode as a direct conversion demodulator from microwave to baseband dc. In this mode, the demodulated I and Q signals are amplified at the respective I and Q differential outputs. Their gain and dc common-mode voltage can be set by registers via the SPI. Alternatively, the ADMV1014 can be used as an image-reject downconverter to single-ended I and Q IF ports. In either mode, the I and Q phase and amplitude imbalance can be corrected via the SPI. Overall, the downconverter provides a total cascaded noise figure of 5.5 dB, with a maximum conversion gain of 17 dB, over the frequency range from 24 GHz to 42 GHz. As the operating frequency gets close to the band edge, the cascaded NF is still a respectable 6 dB.

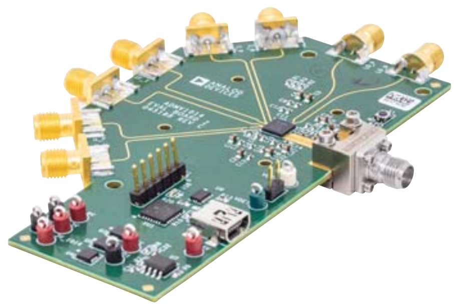


Figure 3. The ADMV1014 in a slightly smaller 5 mm × 5 mm package mounted on its evaluation board.

Boosting 5G mmW Radio Performance

Figure 4 shows the measured performance of the downconverter at 28 GHz frequency, using a 5G NR waveform over 4 independent 100 MHz channels modulated at 256 QAM at –20 dBm input power per channel. The resulting EVM measured –40 dB (1% rms), enabling demodulation of higher order modulation schemes that mmW 5G require. With the upconverters and downconverter's >1 GHz bandwidth capability, along with a 23 dBm OIP3 for the upconverter and 0 dBm IIP3 for the downconverter, the combination can be expected to support high order QAM modulations—hence high data throughput. In addition, the devices benefit other applications such as satellite and Earth station broadband communication links, secured communication radios, RF test equipment, and radar systems. Their superior linearity and image rejection performance are compelling and—when combined with compact solution size—small form factor, high performance microwave links, broadband base stations can be realized.

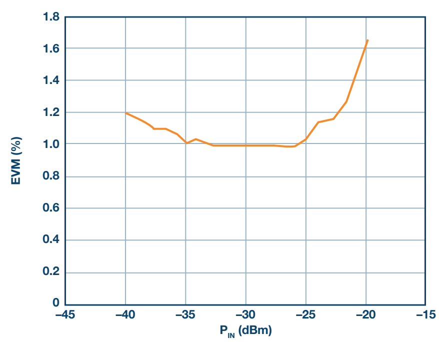


Figure 4. Measured EVM performance in rms percentage vs. input power and the corresponding 256 QAM constellation diagram at 28 GHz.

Data sheet download mou.sr/ADMV1013

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5.	Digi-Key Electronics	$3.160 billion
6.	TTI Inc.	$2.800 billion
7.	Electrocomponents plc/Allied Electronics & Automation ***	$2.030 billion
8.	Mouser Electronics	$1.9 billion
9.	Smith & Associates	$1.66 billion
10.	Newark	$1.5 billion
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12.	Fusion Worldwide	$1.008 billion
13.	DAC	$959.1 million
14.	Sager Electronics	$308 million
15.	America II Electronics	$283 million
16.	Master Electronics	$280 million
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18.	PEI-Genesis	$250 million
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21.	The Powell Electronics Group	$173.9 million
22.	Richardson Electronics, Ltd.	$163.2 million
23.	Sourceability	$162 million
24.	RFMW Ltd.	$156 million
25.	Phoenics Electronics	$155 million
26.	Electro Enterprises	$151.462 million
27.	Classic Components	$120 million
28.	Hughes-Peters	$110.3 million
29.	Flame Enterprises	$95 million
30.	CoreStaff Co., Ltd.	$89 million
31.	Steven Engineering, Inc.	$85.32 million
32.	Chip 1 Exchange	$75 million
33.	Crestwood Technology Group	$75 million
34.	Symmetry Electronics, Corp.	$65 million
35.	Marsh Electronics, Inc.	$62.52 million
36.	Edge Electronics, Inc.	$57.9 million
37.	IBS Electronics, Inc	$52 million
38.	SMD Inc.	$45.8 million
39.	NRC Electronics, Inc.	$41.6 million
40.	Air Electro Inc.	$31.2 million
41.	Area51-ESG, Inc.	$28.41 million
42.	Diverse Electronics	$26.7 million
43.	Powertech Controls Co. Inc	$24.8 million
44.	March Electronics, Inc.	$23.98 million
45.	PUI (Projections Unlimited, Inc.)	$22.1 million
46.	Kensington Electronics, Inc.	$20.6 million
47.	Cumberland Electronics Strategic Supply Solutions Inc (CE3S)	$19.09 million
48.	Gopher Electronics Company	$18.3 million
49.	NASCO Aerospace & Electronics	$16.62 million
50.	Marine Air Supply	$16.2 million

* *SourceToday* adjusted Avnet Inc. revenue to 2018 calendar year
** *SourceToday* estimated Future Electronics global revenue
*** *SourceToday* adjusted Electrocomponents/Allied Electronics & Automation to 2018 calendar year

DR. THOMAS GALLA | Chief Expert Automotive Networks, Elektrobit
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Unleash Multicore-Processor Performance in Automotive Architectures

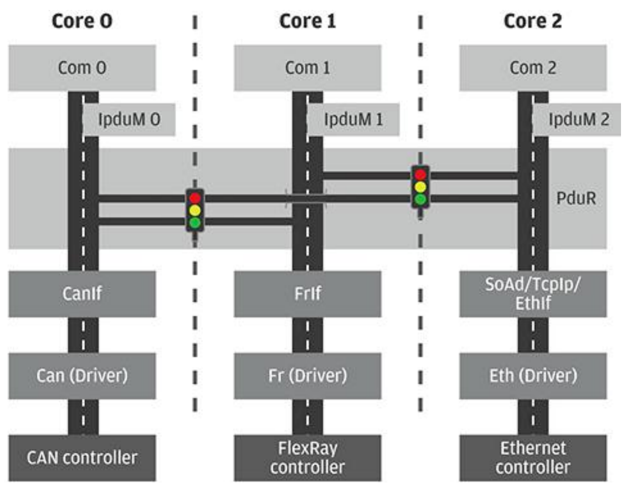
Software must be parallelized and modified to benefit from new approaches to enhance hardware performance in today's automotive designs. AUTOSAR's layered software architecture leverages MCUs to meet the latest demands.

For many decades, software developers benefitted from being able to use the same software code while working with increasingly powerful hardware. As hardware manufacturers regularly improved the performance of their semiconductors by enhancing transistor densities and clock speeds, software development enjoyed a "free ride"—they were able to readily develop on these new devices without having to change software architectures.

However, processing power has hit a wall due to the limit in increasing clock speeds. As a result, chip manufacturers have been turning to dramatically new approaches to achieve further performance gains. First it was hyper-threading and homogeneous architectures, and then heterogeneous multicore architectures. To benefit from these hardware changes, existing software had to be parallelized and modified to deal with the heterogeneity.

Modern microcontrollers (MCUs) and systems-on-a-chip for automotive, such as Infineon's AURIX 2G or NVIDIA's Drive Xavier, point to the trend toward homogeneous, and even heterogeneous, multicore hardware architectures. To benefit from these advances in hardware, changes in automotive software are required as well.

In this article, I will discuss how standardized software architectures, specifically AUTOSAR's layered software architecture, are being updated with today's powerful MCUs to enable dramatically improved performance.



This multicore communication stack architecture is by means of core allocation of the AUTOSAR stack.

OPTIMIZING AUTOSAR FOR MULTICORE ARCHITECTURES

A critical enhancement to the AUTOSAR software architecture has been the distribution of the AUTOSAR communication stack over different cores, which is mandatory for realizing the performance benefits of multicore architectures.

As background, in AUTOSAR 4.0.1, support for multicore MCUs was first introduced. In this update, AUTOSAR provided the means to allocate application software components (SWCs) to dedicated cores and facilitated the cross-core communication between those SWCs via the runtime environment (RTE). AUTOSAR basic software (BSW), however, was still allocated to a single core.

In AUTOSAR 4.2.1, the AUTOSAR basic software was divided into so-called functional clusters that could be allocated to different cores using the BSW schedule manager (SchM) for inter-core communication. Since the communication stack as a whole is such a functional cluster, distribution of the communication stack over multiple cores wasn't supported. And, although AUTOSAR 4.4 introduced the possibility to distribute the BSW modules of the lowest layer (the microcontroller abstraction layer), the remainder of the AUTOSAR communication stack still had to be placed onto a single core.

At this point in the evolution of AUTOSAR, it became obvious that a monolithic communication stack allocated to a single core would eventually become the performance bottleneck. That's because the sequential part of the software would continue to impose a theoretical limit on the speeds achieved by a multicore MCU. Hence, it led to the fresh approach of distributing the communication stack over the different cores, which is a necessity for reaping the performance benefit of multiple cores.

When working on communication stack software distribution, it's important to consider the following to make efficient use of the multicore resources:

- *Inter-core communication and synchronization should be reduced as much as possible,* since they typically involve inter-core interrupts that in turn lead to changes in the MCU's operation mode (transition from user to supervisory mode), pipeline stalls, and cache misses.
- If inter-core calls are required and can't be avoided, *asynchronous calls should be favored over synchronous ones.* The latter block the caller until the callee is finished, thereby reducing the degree of parallelism and thus the potential speedup. Unfortunately, this isn't always possible since, for legacy reasons, AUTOSAR's communication stack makes heavy use of synchronous APIs and changing that would be a major backwards-incompatible redesign.
- In addition, *inter-core mutual exclusion by means of locks should be avoided* if possible, because this blocks all other involved cores while one core resides in the exclusive area. Since typical inter-core mutual exclusion primitives like spinlocks involve busy waiting, this also wastes CPU cycles on the blocked cores.
- *Another crucial consideration is the proper placement of code and data required by the non-uniform memory architecture used by most multicore MCUs.* Memory is divided into core-local memory (caches, flash, and RAM) dedicated to a single core, which can be accessed quickly and conflict-free by that core, and global memory (flash and RAM), which is shared among the different cores and where access to this memory is substantially slower and subject to conflicts. In such a non-uniform memory architecture, proper placement of code and data is critical. Frequently accessed code and data needs to be placed as close to the accessing core as possible. Using the static AUTOSAR memory-mapping mechanisms, such placement should be performed based on access statistics derived under realistic load scenarios.

STACK DISTRIBUTION STRATEGY

With these considerations in mind, we can develop the general distribution strategy for the AUTOSAR communication stack. We split the communication stack into sub-stacks based on the particular network type (i.e., CAN, LIN, FlexRay, and Ethernet) and allow each of these sub-stacks to be allocated to a dedicated core. Thus, any potentially concurrent access to the communication hardware peripherals (i.e., CAN, LIN, FlexRay, and Ethernet controllers) from different cores can be ruled out. In addition, fully independent and parallel execution of the different sub-stacks is possible without interaction among them.

To drive this separation and independence even further, we split the general network-type independent BSW modules of the communication stack (i.e., IpduM and Com) into different parts. Each part is equipped with a dedicated processing function that takes care of processing the subset of the communication originating from, or targeting to, a particular network type. Those dedicated processing functions are then allocated on the dedicated core for the respective network type.

By doing this, we effectively keep all of the communication of a particular network type local to a single core and rule out interference with the communication of any other network type. Thus, we avoid inter-core communication and synchronization, maximize the independent execution of the different communication sub-stacks, and are able to keep most of the AUTOSAR communication stack's synchronous API calls local to the respective core.

The communication paths originating on one network type and targeting some other network type (i.e., gateway routing paths), and communication paths targeting multiple network types (i.e., multicast routing paths), are handled by a multicore-capable PDU router (PduR). The PduR takes care of the required core transitions in those routing paths using the SchM's intercore communication capabilities. Buffering or queuing within the PduR facilitates the use of asynchronous (instead of synchronous) inter-core calls. This results in a decoupling of caller and callee, and thus keeps the execution of the sub-stacks for the different network types independent even for these kinds of communication paths.

This kind of core allocation of the AUTOSAR communication stack results in the multicore communication stack architecture *(see figure on page 34).*

SUCCESSFUL OEM IMPLEMENTATIONS

The approach described here has been successfully implemented and deployed in two real-life automotive series projects for a major German car manufacturer. The first project dealt with the central gateway electronic control unit (ECU) of a premium vehicle that required a vast amount of data to be routed between different networks and exhibited very complex routing paths. In this setup, an STMicroelectronics Chorus 6M MCU was used, where the CAN, FlexRay, and Ethernet sub-stacks were each allocated to dedicated cores.

The second project dealt with a powertrain domain master ECU exhibiting time-critical event chains involving multiple ECUs and requiring strictly deterministic timing on several CAN networks. In this setup, an Infineon AURIX 2G MCU was used, where the CAN and LIN sub-stacks were allocated on one core and the FlexRay and Ethernet sub-stacks were allocated on another core.

Due to the reduced number of communication paths crossing core boundaries in this project, almost no overhead for inter-core communication and synchronization (less than 1% additional CPU load) was measurable. As far as memory mapping is concerned, we gathered access statistics under realistic load scenarios and optimized the memory mapping for frequently accessed code and data. The optimized memory mapping reduced CPU load by 15% compared to an unoptimized memory mapping.

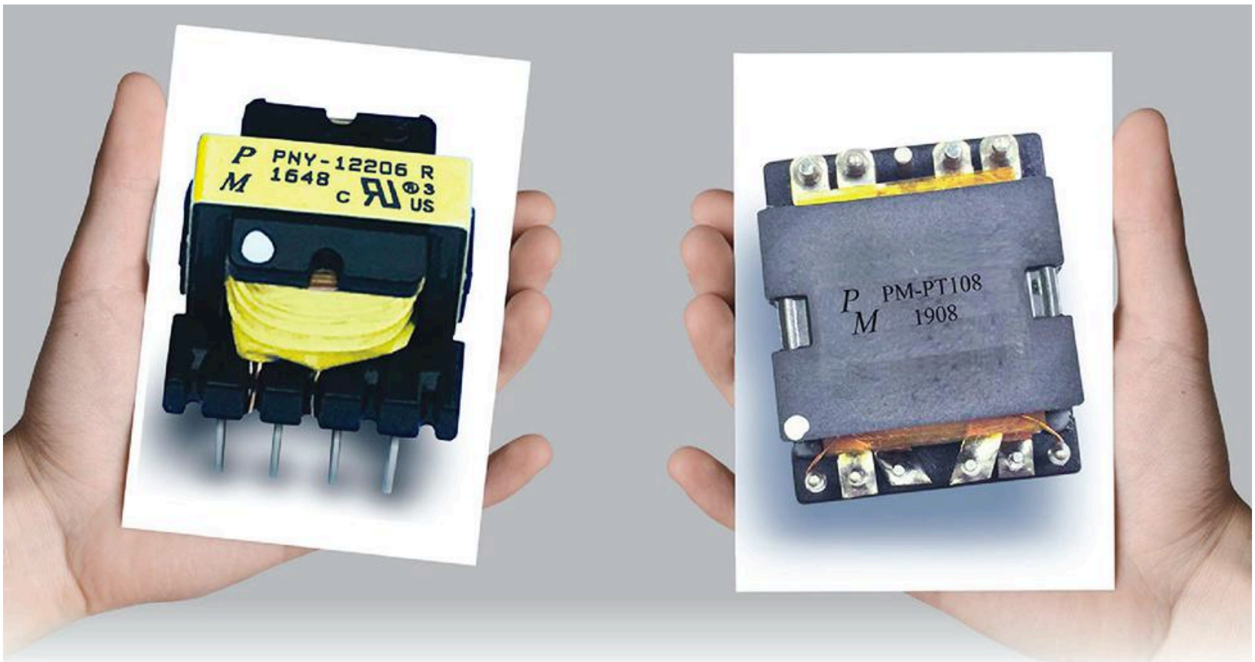
SUMMARY

The efficient use of multicore MCUs requires distribution of the AUTOSAR basic software in general, and particularly of the communication stack. We proposed to split the communication stack according to the different network types to prevent concurrent access to the communication hardware peripherals, to allow for fully independent and parallel execution of the different sub-stacks, and to reduce the need for inter-core communication and synchronization.

We recommend locating code and data within memory with a strong affinity to the respective core using AUTOSAR's static memory-mapping functionality to properly use fast core-local memory as well as prevent/reduce conflicts upon access to slower global memory. Implementing this approach and deploying it in two series projects for a major German OEM showed that by means of distributing the communication stack and doing a proper allocation of the application software components, an efficient use of the multiple cores of an AURIX 2G MCU can be achieved. And there's almost no overhead for inter-core communication and synchronization. ed

DENNIS EARLEY | VP/General Manager, Premier Magnetics

What's the Difference Between Conventional and Planar Switching Power Transformers?



The demand for higher efficiency and smaller packages has been the driving force behind advances in switch mode power conversion topologies including buck, boost, flyback, forward converters, and others. Requirements for smaller devices coupled with the demand for higher power densities are being achieved via innovative component packages. Traditional MOSFET power conversion topologies have responded to these demands through the development of devices designed to operate with lower switching losses at higher frequencies. Over the past several years, emergence of wide bandgap (WBG) devices capable of operating at yet even higher frequencies has accelerated the drive toward higher efficiency and smaller packaging. Planar magnetics devices are replacing traditional transformers and inductors in some of these higher frequency power conversion applications.

This article offers a brief answer to the question: What's the difference between conventional and planar magnetics and how to choose the right one for your application?

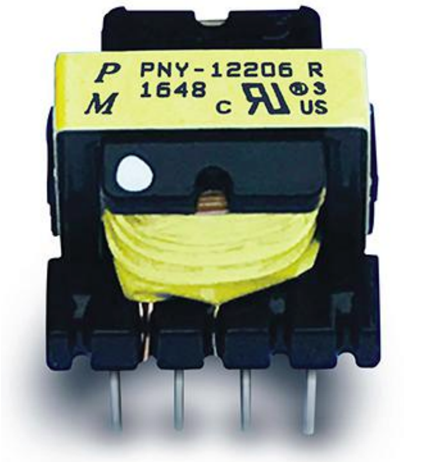
CONVENTIONAL VS. PLANAR TRANSFORMER

A traditional switching power supply transformer like the one shown in *Figure 1* is comprised of primary and secondary wire windings wound on a bobbin and ferrite core. Wire insulation and tape are used to separate the windings. The bobbin and core configuration are determined by the circuit topology.

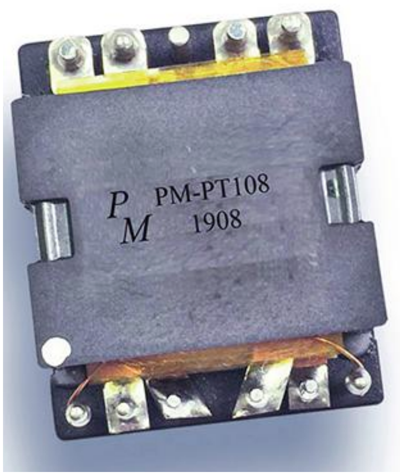
A planar magnetics transformer *(Fig. 2)* replaces the wound wire and bobbin with thin copper sheets "wound" on a printed circuit board that is sandwiched between a ferrite core and fastened with rivets.

HIGHER FREQUENCIES = SMALLER MAGNETICS COMPONENTS?

The first order effect of the increase in switching frequency is the reduction in the inductance of magnetic components. As frequencies continue to increase to several hundred kHz and into the MHz range, other factors emerge that can impact the size reduction benefits of lower inductance.



1. An example of a bobbin and core transformer for a 100-kHz switch-mode power supply.



2. A planar magnetics transformer optimized for switching power supplies operating at up to 700 kHz.

Of significant importance is skin effect. Skin effect is the tendency of an alternating electric current (ac) to become distributed within a conductor such that the current density is largest near the surface of the conductor and decreases with greater depths in the conductor. Since resistivity is a function of the cross-sectional area of the conductor, the result of skin effect is higher resistance at higher frequencies.

To resolve this using a conventional wire-wound-on-bobbin transformer the diameter of the winding wire can be increased. Another way would be in bundle multiple, smaller gauge wires.

Both add more conductive capacity, but both also add to the bulk of the windings. This, in turn, can result in increasing the core size which results in higher core losses. A planar transformer's windings, made up of thin copper foil patterns, are less susceptible to skin effect.

PLANAR TRANSFORMER ADVANTAGES

The turns in a planar transformer are flat foil patterns on a printed circuit board which limits the number of turns possible. At the same time, the greater magnetic cross-sectional area allows for fewer turns. And, the flat form of the magnetic core materials provides a larger surface area for power dissipation. The printed circuit nature of the windings results in a high degree of consistency in spacing between turns and layers, so interwinding capacitance is consistent and winding interleaving allows for reduced ac conduction losses. And, as with any other printed circuit layout, creepage and clearance spacing is used to meet dielectric breakdown requirements. Taking all of this into account, planar transformers offer excellent efficiency and high degree of reproducibility.

TRADITIONAL TRANSFORMER ADVANTAGES

Were it not for the demand for higher frequencies, it is somewhat doubtful that planar transformers would be considered as an alternative to traditional wound-wire magnetics. For all their apparent benefits, and even in those high frequency applications, traditional wound-wire transformers still offer a number of important benefits. Planar Magnetics take up a great deal more circuit board footprint than traditional transformers. So, unless power dissipation and/or headroom are major design considerations, then designers will typically go with a standard transformer.

Finally, the turn-around time for traditional transformers will be shorter than for planer devices. Samples can be wound in a matter of days and adjustments can be quickly made to optimize the performance. Planar devices require a printed-circuit layout and tooling for the magnetic core materials. In very high volume, higher power applications, planar devices will provide the higher performance and economical solution. But traditional magnetics will be the answer for nearly every other application.

WORKING WITH A QUALIFIED SUPPLIER

Ultimately, the best idea is to work with a qualified supplier who understands the benefits and tradeoffs of *both* transformer types. That way, designers can be assured of a truly optimum solution. ed

Special Report

PAUL RAKO | Contributing Editor

What's All This Pease Prototype Stuff, Anyhow?

Digging through boxes of the prototype circuits that Bob Pease had amassed over the years proved to be a fun time for all involved.

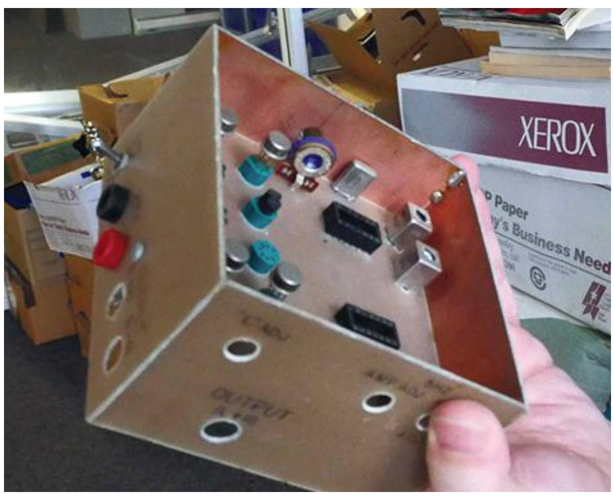
While visiting Texas Instruments in February of 2019, marketing maven Gayle Bullock took me and analog guru Paul Grohe into the storage area where all of Bob Pease's stuff was stored. The yearly Analog Aficionados party was that weekend, and Gayle thought we could give away some of the books and gizmos that were in storage.

Only a few minutes had passed when Grohe pulled a large copper-clad prototype fixture out of the pile and exclaimed, "Look at this, the LM317 voltage regulator prototype! *(Fig. 1)*." The LM317 adjustable voltage regular chip was a very popular IC designed by Bob Dobkin at National Semiconductor before he left to found Linear Technology, now part of Analog Devices. We assumed Pease's hoarding instincts made him grab up this prototype, knowing its historical significance.

I wrote Dobkin, and he replied, "In ancient days, I designed the LM317 and Pease designed the LM337 a couple of years later. He did not have anything to do with the 317 development. The 317 was designed in 1975 and introduced in 1976 if I remember correctly."

The intriguing thing about this "317 breadboard" is that it's dated 4/24/84 and has the notation, "Better tempco (temperature coefficient)." So perhaps Pease worked on this after Dobkin left the company. Dennis Monticelli wrote me, "Don't remember it. I think Bob reported to Tim Isbell at this time. He reported to me later in 80s. That said, it fits with Bob's style. He was always exploring ways to improve bandgaps. He may have done this project on the side and, if successful, would have advocated for making a premium version. The 317 was being widely copied at the time so performance differentiation was probably on his mind."

1. Texas Instruments application engineer Paul Grohe holds up an LM317 voltage regulator IC prototype likely designed by Bob Pease to improve the regulation accuracy over temperature.



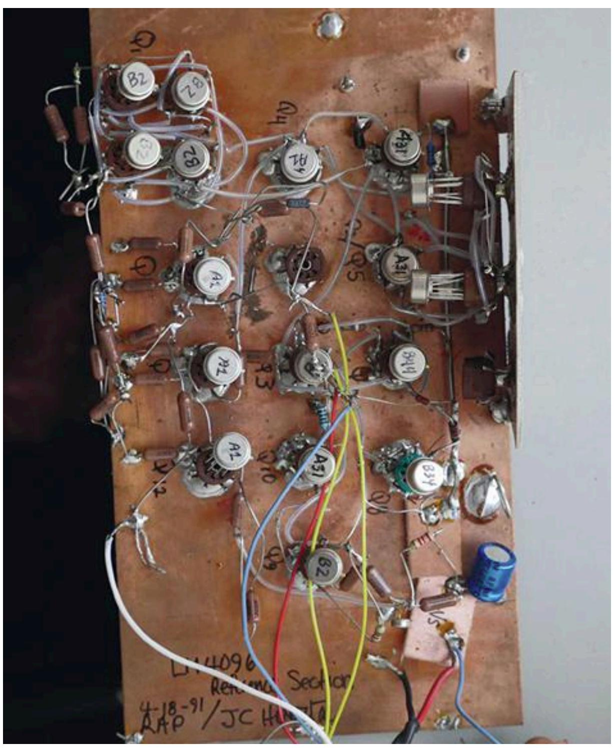
2. Pease and other engineers would use copper-clad circuit board material as a structural and shielding component in their prototypes.

PCB BOXES FOR RF

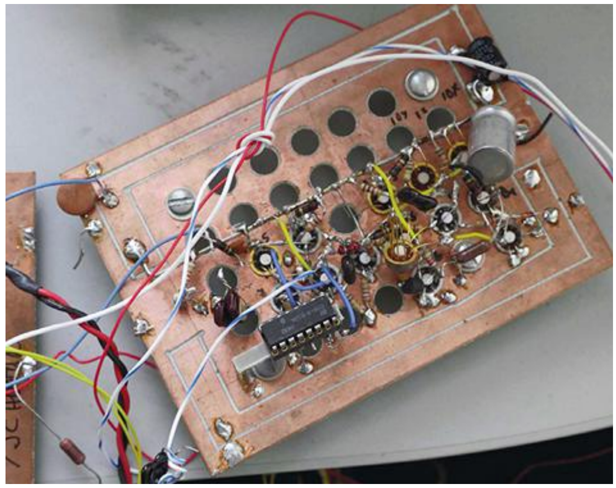
Soon Grohe fished another treasure out of a box *(Fig. 2)*. This looks to be an RF circuit, probably part of the AM radio system National Semiconductor worked on decades ago. This little cube is of interest to show how Pease or a technician would fabricate a prototype that was suitable for RF frequencies. It's a shame that some of the sockets are empty.

There were two copper-clad boards for the LM4096. The reference section was dated 4/18/91 and initialed by Pease with a notation of his tech, JC Huerta *(Fig. 3)*. The board had over a dozen transistors in metal cans. These are "kit parts" that design engineers could use to make a physical prototype of an integrated circuit. The kit parts were made on the same process as the IC. The kit parts will have more inductance in the wiring, and they won't track temperature as well as when on the same IC. Even with these limitations, it was a great way to see if a circuit would work, before Spice simulations became so common.

The circuit board connected to the reference section had more kit part transistors and a precision resistor IC with eight 10-kΩ resistors *(Fig. 4)*. Being in the same IC, these resistors do track over temperature. This board uses a prototype method I had not seen before. The board has a matrix of holes that fit the metal can of the kit parts. Some of the cans are soldered to the copper-clad circuit board. This is similar to a "dead bug" prototype, since the parts are upside down, and resemble a dead insect. With the kit parts firmly mounted, it's simple to "air-ball" wire the leads and connect in discrete components.



3. This is a prototype of the reference section of the LM4096 1-W audio amplifier, no longer in production.



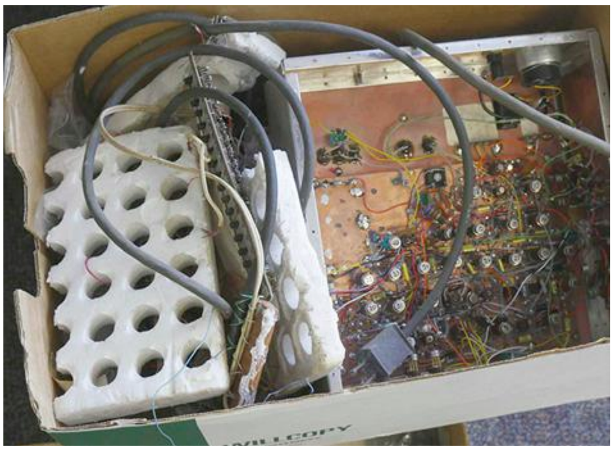
4. A second board Pease used in the LM4096 prototype.

I looked in a large box that was formed by two boxes taped together *(Fig. 5)*. It was Pease's ball-on-beam demonstration, where he showed that an operational amplifier can balance a ball on a moving beam. Pease used this demo at many trade shows and seminars.

5. A large box contained Pease's ball-on-beam demonstration.

There were moving boxes chock-full of prototypes, circuits, and other Pease detritus *(Fig. 6)*. One box had a very complicated copper-clad prototype *(Fig. 7)*. I only wish that Pease had kept better documentation on them. When I build prototypes, I have a ring binder for them. Each prototype of a set gets a section where I keep track of any changes or differences to the others, as well as the test results. The rest of binder is full of datasheets and bills-of-materials for the design. Rather than keep a lab notebook separately, I would just put my design notes in one section of the binder.

6. A moving box from Bob Pease's home had several prototypes and a CD ROM player, as well as lots of paper. Pease was a hoarder.



7. Another box from Pease's home has a more complicated prototype, a switch panel, and dozens of odd and ends.

8. This box has several of Bob Pease's hand-built prototypes. The 9-V battery is most likely long dead.

Yet another moving box had a cache of complex hand-built Pease prototypes *(Fig. 8)*. Oh, if these slabs of copper-coated FR4 could talk. On the top was another prototyping technique I had not seen. Pease cut copper-clad board material into long narrow strips. He then soldered three of those strips to other boards, spaced out so he could solder components in between. I could see the strips carrying positive and negative power, as well as a ground strip in the middle. You could use the other sides of the copper-clad to interconnect intermediate circuit nodes. Pease was clever in everything he did.

THERE'S GOLD IN THOSE BOXES

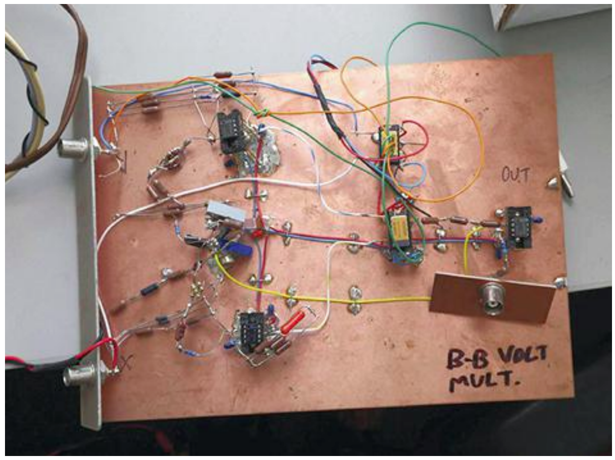
One box was full of gold-plated metal-can parts *(Fig. 9)*. I thought those were valuable, but Grohe explained that they would need to be scrapped. Since they might be what is called "first silicon," there was no way of knowing if the parts were production parts or prototypes. The records of the case codes are long gone.

9. Pease had a huge hoard of parts in his lab. Some of these are unlabeled and may have been for his gag Czar of Bandgaps costume used in advertisements.

When I worked at National Semi, I once saw 4,000 LM-series audio boomer amplifiers in tubes in a hallway. Thankfully, Grohe had me check with the audio group, and they confirmed they were a first spin of a part, and had problems, which is why they were scrapped. They went to a metal recycling place, not an electronics salvage yard.

Not all of the boards were hand-built prototypes. Bullock found a TP3237V evaluation board *(Fig. 10)*. This is not a TI board or something Pease designed. There's a company name, but several letters are obscured by a wire. It looks to be something like Semoltec, but I can't be sure. I suspect we threw this board away since it was not a Pease prototype. Likely, it was something Pease used to evaluate one of his parts or some other design experiment.

A nice little prototype was labeled "B-B Mult" *(Fig. 11)*. This means Burr-Brown multiplier, a circuit that multiplies two input signals. Pease loved any good analog IC, even if it was made by a competitor like Burr-Brown. How nice that both National Semiconductor and Burr-Brown were both bought by Texas Instruments.



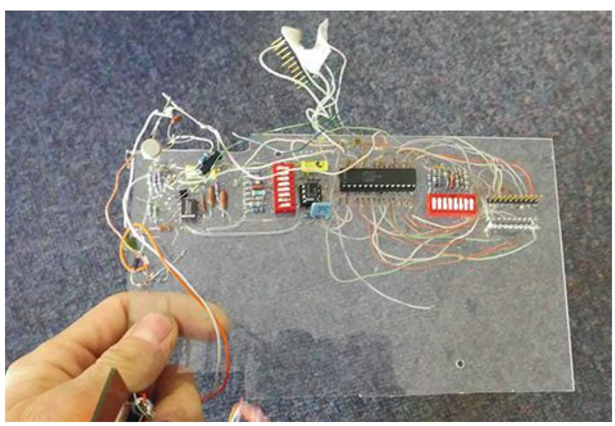
11. Pease fashioned this voltage multiplier circuit using Burr-Brown integrated circuits.

Another cute prototype used a Linear Technology part *(Fig. 12)*. It's an LTC1657 DAC (digital-to-analog converter) IC. That explains the DIP switches Pease used to enter a digital value. We have no idea why this was built on clear plastic as opposed to copper-clad circuit-board material. It might have been an artistic statement, or something to show off to Pease's friend, Jim Williams. Or perhaps it was a Jim Williams prototype that he gave to Pease.

A VHS CASSETTE BOX… A HAIR DRYER… AND A THERMOS MUG

Pease was an avid videographer, carrying about his VHS recorder to treks in the Himalayas as well as trade shows. I once saw him in Fry's Electronics taking a video of the long

10. A mystery evaluation board. Searching the part number TP3237V does not yield any meaningful results.

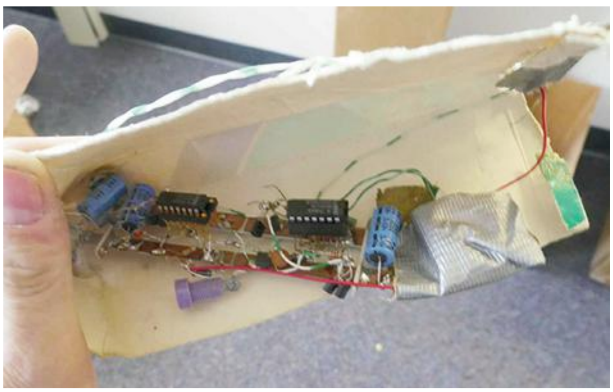


12. A DAC circuit Pease fashioned on clear plastic, very unusual for him.

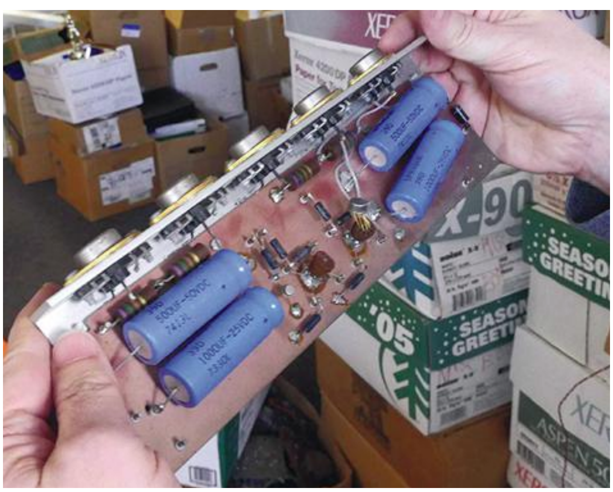
line. It was no surprise he built a prototype inside a VHS cassette box *(Fig. 13)*. Once again, we are not sure of the function of this prototype, with two ICs and a handful of transistors and discrete components, it might be anything.

Pease did not design a lot of power electronics, so I suspect we found an audio amplifier prototype *(Fig. 14)*. With what looks to be two power rails and two metal-can transistors, this is likely a stereo amplifier. I know Pease worked on the remarkable LME49710 audio operational amplifier, so maybe that's what this was for. We were in a rush, so I did not jot down the part numbers of the ICs in the prototypes, sorry.

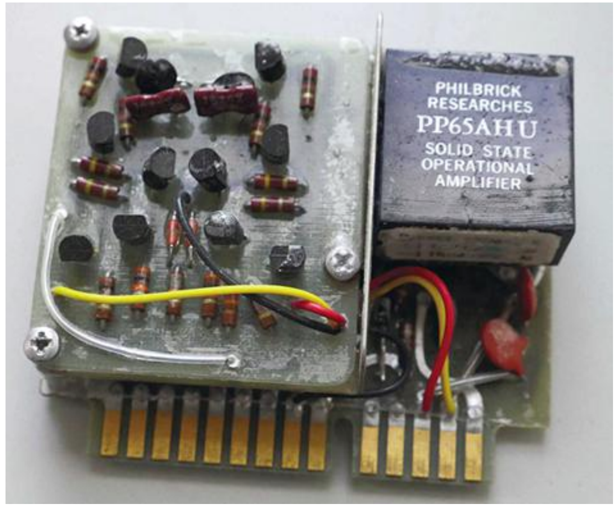
Some of the prototypes went back to Pease's time at Philbrick Researches, in the 1970s *(Fig. 15)*. This assembly incorporated a Philbrick PP65AHU operational amplifier module on a small circuit card. Another prototype had the mezzanine card removed *(Fig. 16)*. There you can see how Pease would put heat shrink around three TO-92 transistors so that they would track over temperature. The back of the board showed how Pease hacked in a few discrete components *(Fig. 17)*.



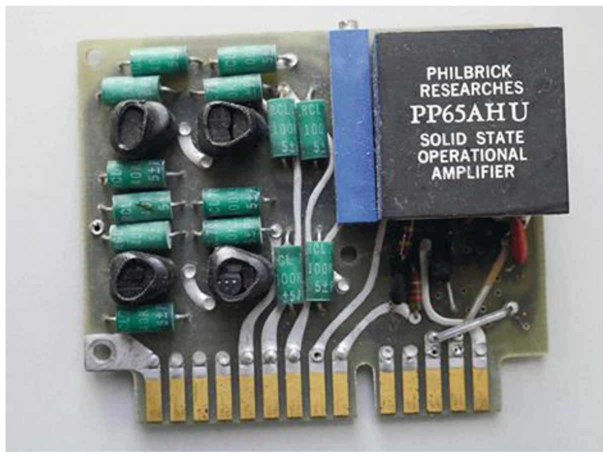
13. Pease used an old VHS cassette tape box to house one of his prototypes.



14. A more substantial Pease prototype, likely a stereo audio amplifier.



15. This mystery circuit card incorporates a Philbrick PP65AHU op amp.



16. Another prototype board. but it's missing the mezzanine card.

17. The backside of one of the prototype Philbrick cards, showing some cuts, jumps, and added components.

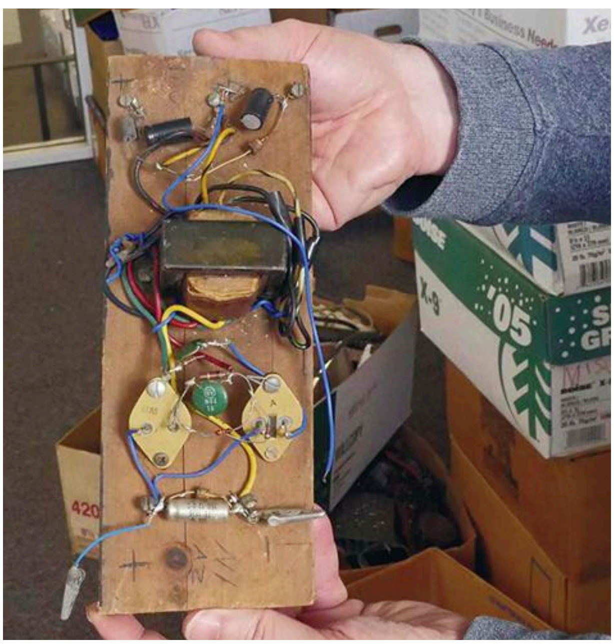
Grohe soon dug up what looks to be another audio amplifier prototype *(Fig. 18)*. This one has transformer coupling, and two TO-3 packaged transistors "dead bugged" on the copper-clad circuit board.

Some prototype functions will be lost to history *(Fig. 19)*. This one was tangled up with a hair dryer that Pease surely used to test his circuits over temperature extremes. Be careful if you do the same, it's easy to overheat an IC with a hair dryer.

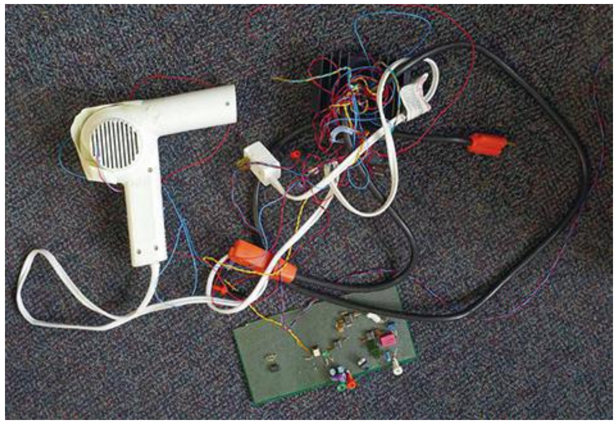
Grohe was delighted to find a thermocouple assembly he used when he helped Pease design an ultra-stable and ultra-precise temperature bath *(Fig. 20)*. He could regulate it to 0.1°C, and the entire device was built into a Thermos mug. They used this to test Pease's LM35 temperature-sensing IC.

We also found an LM109 test fixture *(Fig. 21)*. It was built by analog aficionado Fran Hoffart, now retired. Dated 2-16-75, there's a label on the right side that says "Widlar's Butt." I thought this was a crude reference to Bob Widlar's anatomy, but it stands for "Button."

I got an explanation from Bob Dobkin, now of Analog Devices. He wrote, "The test box, which has an object on the right side called Widlar's button, was developed around the LM309. Widlar didn't like the box at first and wanted the push button on the right side, not the left side. So we took and scraped the copper clad off the bottom inside of the box and put a photo detector underneath that area. When you put your finger over the Widlar button, it blocked the light and activated the test sequence. It was always fun playing tricks on Widlar. When he put his finger on the Widlar button and it activated, he almost fainted." ed

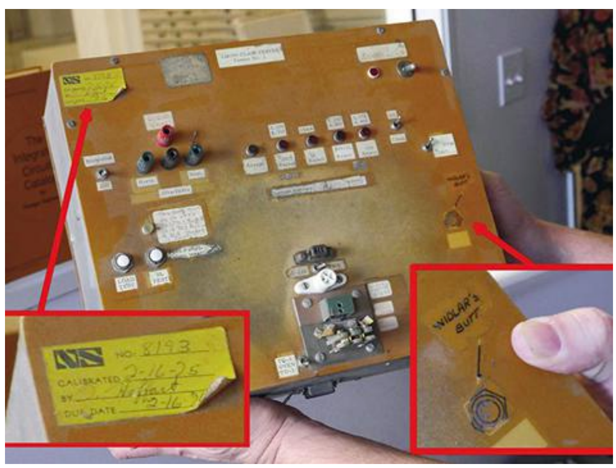


18. Another audio amplifier prototype, with transformer-coupling on the output.



19. Many of the boxes from Bob Pease's house were jumbles of stuff.

20. Paul Grohe shows the thermocouple assembly he helped Pease build.



21. Not a Pease prototype, but a test fixture built in 1975 for Bob Widlar's LM109 voltage regulator. The "Widlar's Button" on the right is a small hole in the board that will activate an optosensor when you put your finger over it.

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Wearable Clinical-Grade Medical Sensors Get Even Smaller

New, compact clinical-grade medical sensors developed by Maxim Integrated will target applications like wireless earbuds.

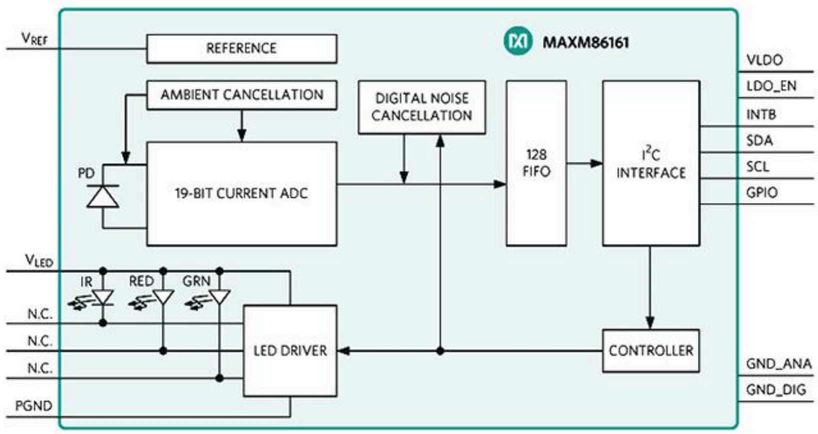
Maxim Integrated Products has been at the forefront of medical sensing with development kits like the Health Sensor Platform (HSP). The HSP is a modular smartwatch form factor that can monitor a user's electrocardiogram (ECG), heart rate, and body temperature.

Its latest products, aimed at the wireless earbud market and similar application areas, are the MAX86161 in-ear heart-rate monitor and its MAX30208 digital temperature sensor. They're designed to deliver clinical-grade medical results while shrinking size and power requirements that are key to delivering compact mobile devices.

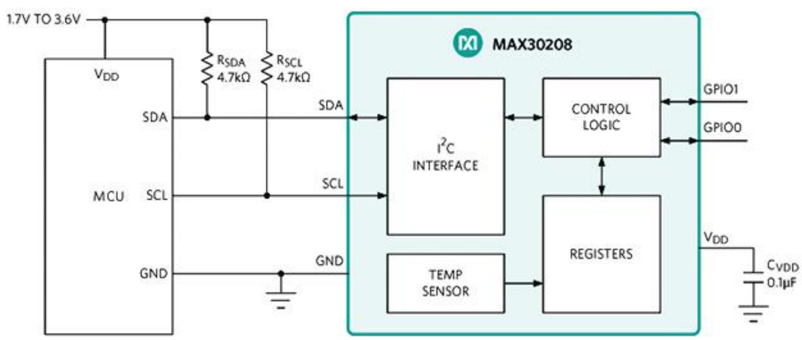
The MAX86161 in-ear heart rate monitor *(Fig. 1)* delivers best-in-class signal-to-noise ratio (SNR) for continuous heart-rate and oxygen-saturation (SpO_2) measurements. It incorporates three programmable, high-current LED drivers, yet only requires a single voltage source from 3.0 to 5.5 V. The receiver uses a high-efficiency PIN photodiode with an optical readout channel. This channel has a low-noise signal conditioning analog front-end (AFE) that consists of a 19-bit ADC, and an ambient-light-cancellation (ALC) circuit to support a picket-fence detect-and-replace algorithm.

Maxim's matching optical solution is 40% smaller than previous versions. The chip comes in a 2.9- × 4.3- × 1.4-mm, 14-pin OLGA package. Maxim also provides algorithms for motion compensation to increase measurement accuracy.

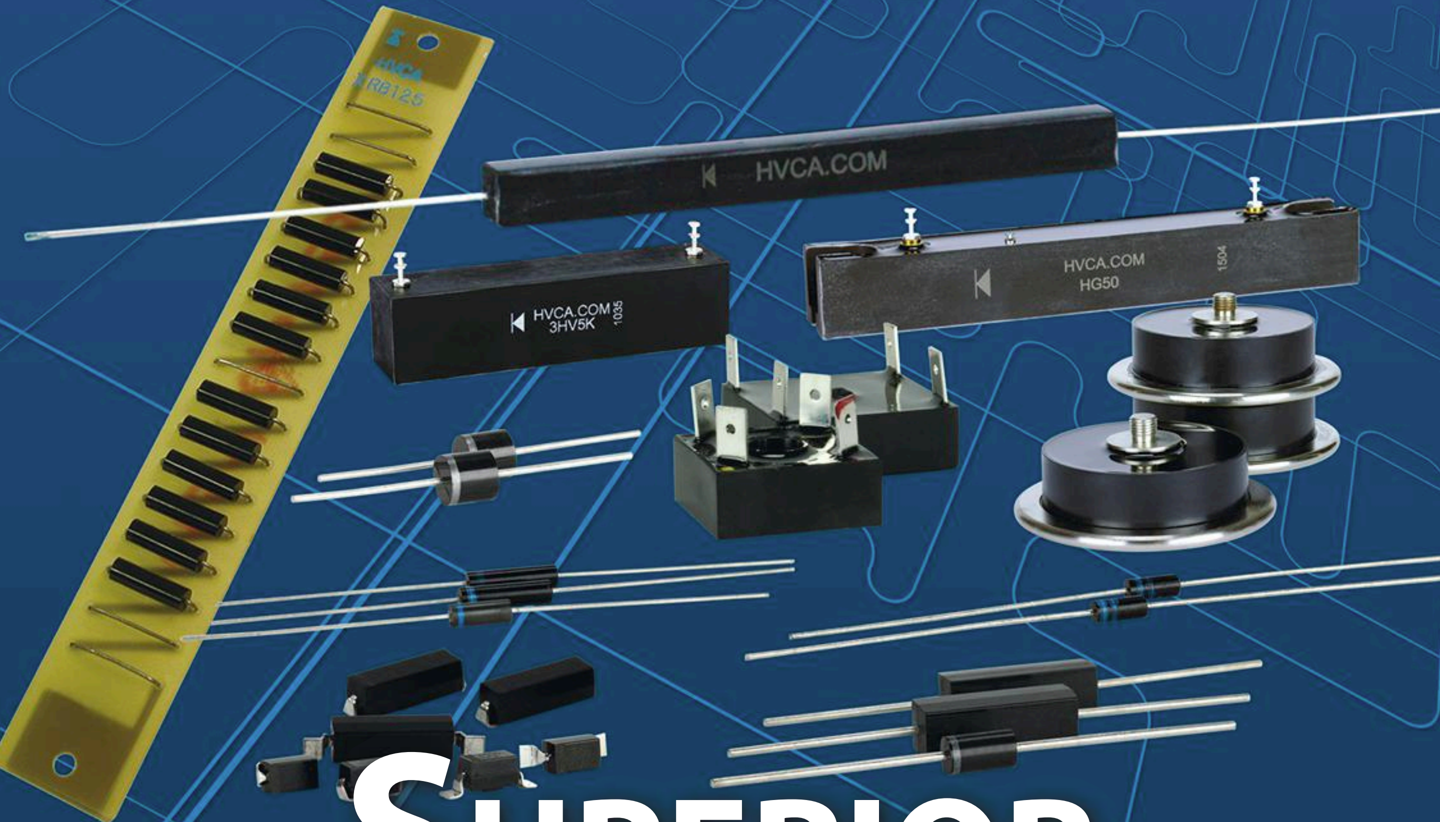
The very low power MAX30208 digital temperature sensor *(Fig. 2)* has an accuracy of ±0.1°C from 30 to 50°C and ±0.15°C over a wider range from 0 to 70°C. The system, replete with 16-bit resolution, uses a single supply voltage from 1.7 to 3.6 V. The tiny 2- × 2- × 0.75-mm, 10-pin thin LGA chip also incorporates a unique ROM ID that allows the device to be NIST traceable. ed



1. The MAX86161 in-ear heart rate monitor features optics that are 40% smaller than previous versions.



2. The MAX30208 digital temperature sensor's accuracy is ±0.1°C.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