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Ideas for Design

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Direct digital synthesis ICs can convert square waves to sine/cosine waves but their complexity is a disadvantage. This circuit uses simple CMOS logic and two switched-capacitor filters to perform the conversion.

Determine Equivalent ESR, Ripple Voltage, And Currents For Unequal Capacitors In Parallel

Capacitors are used in parallel to provide special performance attributes; however, it's difficult to determine critical performance specifics of ESR, high-frequency ripple voltage, and individual RMS currents when they have unequal values. This numerical approach provides a straightforward solution to calculating the values based on published specifications.

Graphically Determine The Output Signal Level Of An RC Filter

The need to know what the output filter's value will be is especially important for variable switching power supplies operating at different duty cycles. This discussion provides a method for calculating that output.

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ideas for design

Circuit Generates High-Frequency Sine/Cosine Waves From Square-Wave Input

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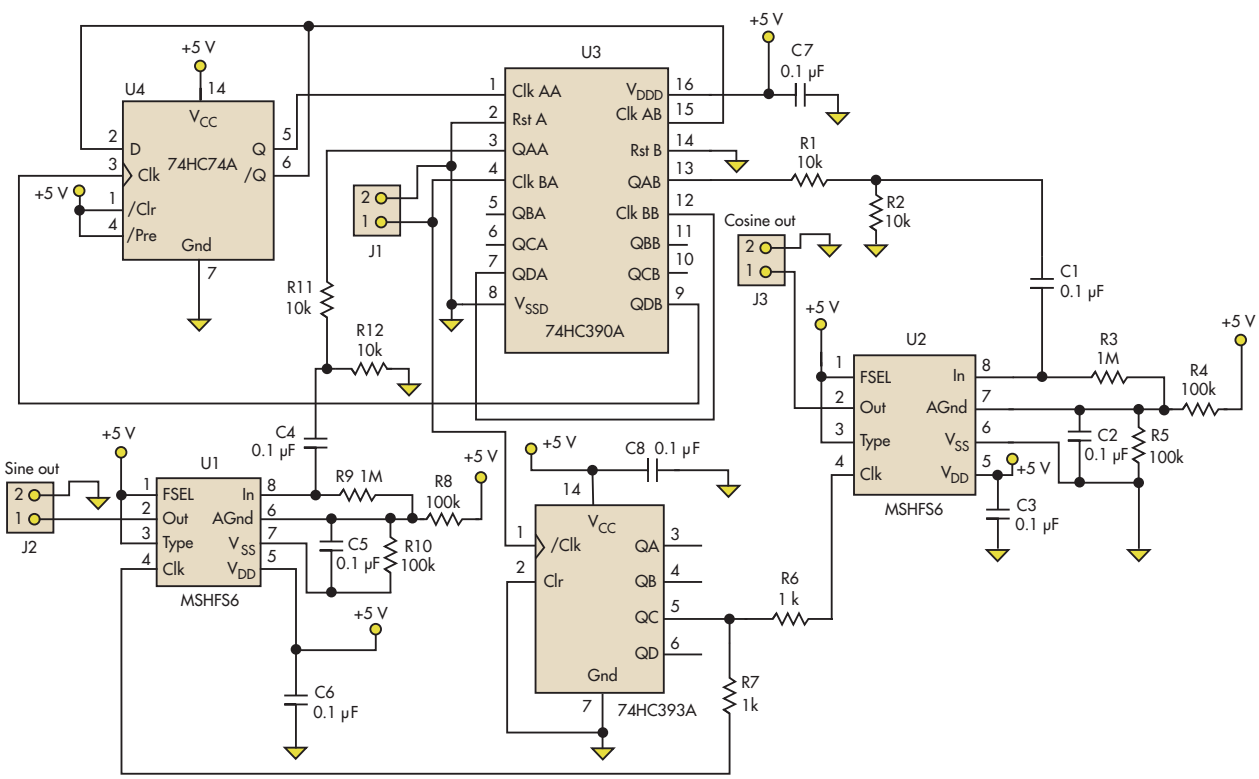
ALTHOUGH QUITE A FEW direct digital synthesis (DDS) ICs can generate high-frequency sine waves, their complexity excludes them from many designs. However, designers can use simple high-frequency CMOS logic and two switched-capacitor filters to create a sine/cosine generator. With newer filters, a 1-MHz output at 1.7 V p-p is possible.

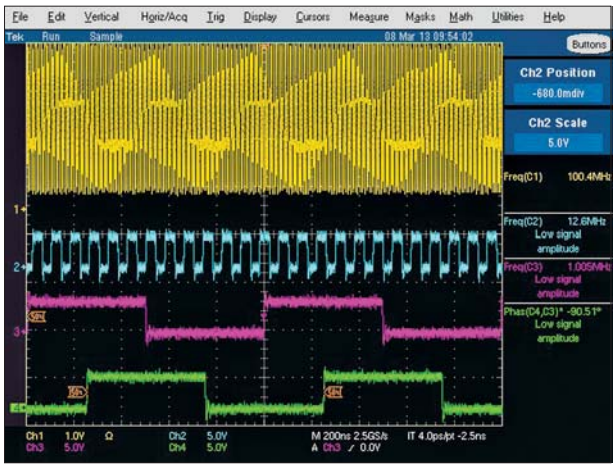
The example circuit uses an MSHFS6 5-V, low-power 12.5:1 switched-capacitor filter with selectable Butterworth, Bessel, or elliptic filters in the lowpass mode and full-, 1/3-, or 1/6-octave filters in the bandpass mode. Since the lowpass mode would cause a 3-dB loss of the signal output, the circuit uses the 1/6-octave bandpass filter, which is selected by tying pins 1 and 3 high on the MSHFS6 *(Fig. 1)*.

Two separate divider circuits are used. The 74HC393A divides the 50-MHz clock to 12.5 MHz. The 74HC390A is a dual divide-by-2 and divide-by-5 device. By combining the 74HC390 with the 74HC74A dual flip-flop, the 50-MHz clock can be divided to 500 kHz.

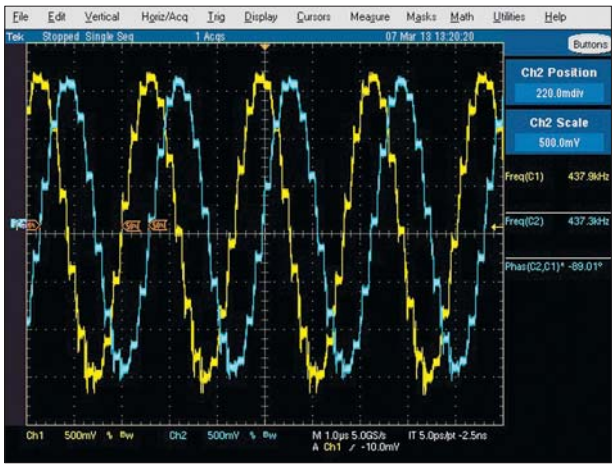
The 74HC74A provides a Q and /Q output at half the frequency of the divide-by-25 output of the 74HC390A. Dividing the 74HC74A output by 2 with the divide-by-2 blocks in the 74HC390A creates two square waves –90° apart. Figure 2 shows a 100-MHz square-wave input, a 12.5-MHz output for the filter clock, and 1-MHz sine and –cosine square-wave output before the dividers. Resistor-divider circuits reduce the amplitude from rail to rail to prevent generation of distor-



1. Instead of a DDS IC, the sine/cosine generator uses simple CMOS logic and two switched-capacitor filters to provide a 1-MHz output at 3.0 V dc.



2. The 1-MHz sine and –cosine outputs of the generator (channels 3 and 4) result from the 100-MHz square-wave input (channel 1).



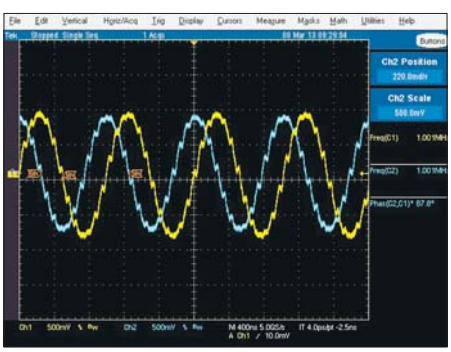
3. Channels 1 and 2 show the outputs of the two switched-filter capacitors with an input clock of nearly 50 MHz.

tion in the filters. The use of ac coupling at the MSHFS6 filter inputs ensures smoothed square waves centered around the filters' analog ground.

Figure 3 shows the output of the two filters with an input clock of nearly 50 MHz. If the inverted cosine is not acceptable, an op amp at the cosine filter output or the inverter at pin 13 of the 74HC390A can correct it.

The Lissajous curve for the two outputs *(Fig. 4)* indicates that the phase circle matches the 89.1° reading in Figure 3. Using a Krohn-Hite 6900B distortion analyzer and a 1-MHz Krohn Hite lowpass filter (to remove the clock), the circuit's total harmonic distortion on the sine output was only 0.1%. Although the 74HC390A and 74HC393A have a guaranteed maximum operating frequency of 50 MHz at 6 V, Mixed Signal Integration Corp. and other companies have found that spec to be very conservative.

In this application, a 100-MHz input clock achieved the desired divide-by-4 and divide-by-100 needed to operate the newer MSVHFS6 switched-capacitor filter at 3.3 V. The only change needed was to reduce V_{DD} to 3.3 V and replace the 5-V MSHFS6 filters with the 3.3-V MSVHFS6. The input clock was increased to 100 MHz. Figures 5 and 6 show the filter outputs' phase relationship in time and as a Lissajous curve.



5. The original circuit used the MSHFS6 switched capacitor, but it also works with the newer MSVHFS6 version, which runs on 3.3 V rather than 5.0 V. This screen shows the two outputs' phase relationship in time.

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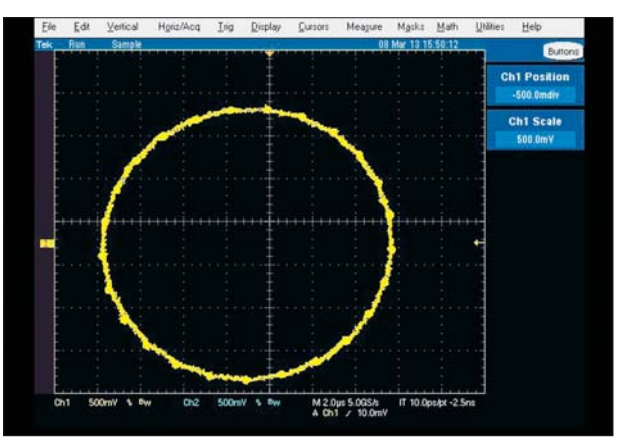

4. The Lissajous curve for the circuit's two outputs shows that the phase circle matches the 89.1° found in Figure 3.

6. The Lissajous curve for the circuit using the MSVHFS6 3.3-V filters shows the outputs' phase relationship.

Determine Equivalent ESR, Ripple Voltage, And Currents For Unequal Capacitors In Parallel

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CAPACITORS OFTEN ARE CONNECTED in parallel in power electronics to decrease high-frequency ripples, current stress, power dissipation, and operating temperature, as well as to shape frequency response and boost reliability. Yet designers have three critical questions about this technique:

- What are the equivalent values of capacitance C_{se} and equivalent series resistance (ESR) R_{se}?
- What is the high-frequency ripple voltage?
- What are the individual RMS currents?

If all N capacitors in the parallel connection are identical *(Fig. 1)*, with equal capacitance values $C_{sk} = C$ and equal ESR values $R_{sk} = R_s$, then for k = 1, 2, . . . N the answers are clear:

- C_{se} is directly proportional to the number of capacitors N: $C_{se} = NC$, and R_{se} is inversely proportional to N: $R_{se} = R_s/N$.
- Ripple voltage V (RMS value) is:

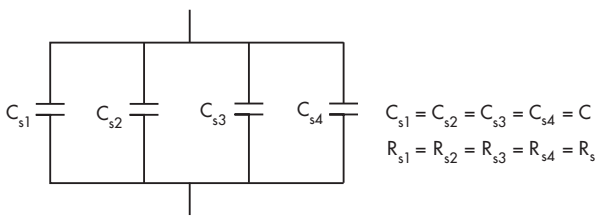
$$V = I\sqrt{R_{se}^2 + X_{se}^2} \qquad (1)$$

for a sinusoidal current excitation $i(t) = I\sqrt{2}\sin(2\pi ft)$ with frequency f, where $X_{se} = 1/(2\pi fC_{se})$ is the reactance of the equivalent capacitor C_{se} and RMS value I, and individual RMS currents in the capacitors are identical: $I_k = I/N$.

When the capacitors in the parallel connection aren't identical, with different capacitance C_{sk} and ESR R_{sk} values, the solution to the problem isn't trivial. The direct approach is to obtain an analytical expression for the input impedance of the parallel connection in the algebraic form $Z = \mathrm{Re}\,Z - j\,\mathrm{Im}Z = Z_{se}\,Z$ and use the formulas $R_{se} = \mathrm{Re}\,Z$, $X_{se} = \mathrm{Im}\,Z$, and $C_{se} = 1/(2\pi f X_{se})$.

A less complicated approach is based on the conversion of series C_{sk}, R_{sk} connections to equivalent parallel C_{pk}, R_{pk} connections. To obtain relationships between R_{pk} and R_{sk}, and also between C_{pk} and C_{sk}, set the admittance Y_{pk} of the parallel C_{pk}, R_{pk} pair and admittance Y_{sk} of the series C_{sk}, R_{sk} pair connections equal to each other: $Y_{pk} = Y_{sk}$, $\mathrm{Re}\,(Y_{pk}) = \mathrm{Re}\,(Y_{sk})$, and $\mathrm{Im}\,(Y_{pk}) = \mathrm{Im}\,(Y_{sk})$. Then:

$$C_{pk} = \frac{C_{sk}}{1 + \left(\frac{R_{sk}}{X_{sk}}\right)^2} \qquad (2)$$



1. For an array of N identical capacitors in parallel, determining the total equivalent capacitance and ESR values is straightforward. For unequal capacitors, the calculation can be difficult.

$$R_{pk} = \frac{R_{sk}^2 + X_{sk}^2}{R_{sk}} \qquad (3)$$

where:

$$X_{sk} = \frac{1}{2\pi fC_{sk}} \qquad (4)$$

is the reactance of the individual capacitor.

After individual parallel capacitances C_{pk} and resistances R_{pk} are calculated according to Equations 2 and 3, equivalent parallel capacitance C_{pe} can be easily found as the sum of C_{pk}:

$$C_{pe} = \sum_{k=1}^{N} C_{pk} \qquad (5)$$

The real part of equivalent admittance can be found as the sum of admittances $1/R_{pk}$. R_{pe} can be obtained as a reverse value of that sum:

$$R_{pe} = \frac{1}{\sum_{k=1}^{N} \frac{1}{R_{pk}}} \qquad (6)$$

The system's equivalent series capacitance C_{se} and ESR R_{se} can be found by conversion of the parallel C_{pe}, R_{pe} connection to the equivalent series connection C_{se}, R_{se}. To obtain relationships between C_{se} and C_{pe} and also between R_{se} and R_{pe}, set impedance Z_{pe} of the parallel C_{pe}, R_{pe} and impedance Z_{se} of the series C_{se}, R_{se} connections equal to each other: $Z_{pe} = Z_{se}$, $\mathrm{Re}\,Z_{pe} = \mathrm{Re}\,Z_{se}$, $\mathrm{Im}\,Z_{pe} = \mathrm{Im}\,Z_{se}$. Then:

$$C_{se} = C_{pe}\left[1 + \left(\frac{X_{pe}}{R_{pe}}\right)^2\right] \qquad (7)$$

$$R_{se} = \frac{R_{pe}}{\left[1 + \left(\frac{R_{pe}}{X_{pe}}\right)^2\right]} \qquad (8)$$

where:

$$X_{pe} = \frac{1}{2\pi f C_{pe}} \qquad (9)$$

is the reactance of the equivalent parallel capacitor C_{pe} *(Equation 5)*.

Based on this analysis, the calculation procedure for equivalent series capacitance C_{se}, ESR R_{se}, voltage ripples V, and RMS currents I_k in the capacitors is:

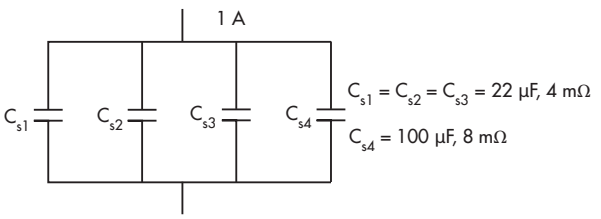
- Calculate reactances of individual capacitances according to Equation 4.
- Determine equivalent parallel parameters C_{pk}, R_{pk} of the capacitors based on Equations 2 and 3.
- Calculate equivalent parallel capacitance C_{pe} of the structure, its reactance X_{pe}, and equivalent parallel resistance R_{pe} according to Equations 5, 9, and 6.
- Calculate equivalent series capacitance C_{se} and ESR R_{se} of the structure according to Equations 7 and 8.
- Obtain RMS ripple voltage V using Equation 1.
- Calculate RMS currents I_k in the capacitors based on:

$$I_k = \frac{V}{\sqrt{R_{sk}^2 + X_{sk}^2}} \qquad (10)$$

Note that ESR values R_{sk} are strong functions of frequency. A designer should use ESR data specified by capacitor manufacturers at a given frequency of operation, such as the data for ceramic and polymer aluminum electrolytic capacitors from Murata Manufacturing Co. Ltd. (MMC) *(http://ds.murata.co.jp/software/simsurfing/en-us/index.html)*.

To illustrate the calculation procedure, let's determine equivalent parameters, voltage ripple, and current distribution for a parallel connection of three ceramic capacitors (GRM-21BR60J226ME39L) and one polymer capacitor (ESASD-40J107M015K00) from MMC *(Fig. 2)*. Using the data f = 200 kHz, $C_{s1} = C_{s2} = C_{s3} = 22$ µF, $R_{s1} = R_{s2} = R_{s3} = 4$ mΩ, $C_{s4} = 100$ µF, $R_{s4} = 8$ mΩ, I = 2 A, then:

- For reactance of each individual capacitance according to Equation 4, we have $X_{si} = X_{s2} = X_{s3} = 3.6$ mΩ, $X_{s4} = 0.8$ mΩ.
- Equivalent parallel parameters C_{pk}, R_{pk} of the capacitors based on Equations 2 and 3 are $C_{p1} = C_{p2} = C_{p3} = 21.7$ µF, $R_{p1} = R_{p2} = R_{p3} = 331$ mΩ, $C_{p4} = 49.7$ µF, $R_{p4} = 16$ mΩ.



2. This example of four capacitors, with three identical and one different, illustrates how the computation scheme works in practice.

- For equivalent parallel capacitance C_{pe}, its reactance X_{pe} and equivalent parallel resistance R_{pe} of the structure according to Equations 5, 9, and 6, we calculate $C_{pe} = 115$ µF, $X_{pe} = 6.9$ mΩ, $R_{pe} = 13.9$ mΩ.
- According to Equations 7 and 8, the equivalent series capacitance C_{se} and ESR R_{se} are $C_{se} = 143.4$ µF, $R_{se} = 2.76$ mΩ.
- For RMS ripple voltage V based on Equation 1, we obtain V = 12.4 mV.
- RMS currents according to Equation 10 in ceramic and polymer capacitors are respectively: $I_1 = I_2 = I_3 = 341$ mA, $I_4 = 1.1$ A.

This shows the technique can easily determine the parameter values in each of the capacitors.

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Graphically Determine The Output Signal Level Of An RC Filter

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WHEN DESIGNING FILTERS, engineers very often need to know what the filtered value at the output will be. This is especially important for variable switching power supplies operating at different duty cycles. The analysis presented here discusses the calculation of the filtered output for RC filters, which are common in feedback circuits, current transformers, output devices, and other circuits. However, the analysis easily can be extended to other kinds of filters.

It's well known that for rectangular-pulse inputs the rms values of the unfiltered output parameters, like voltage and current, are proportional to the square root of a duty cycle. But the designer of a feedback filter for a switching power supply must consider that the filter output is not an rms value but rather proportional to the pulse's duty cycle. You can adjust the filter's parameters to obtain an rms value, but it would be valid only for one duty-cycle value.

The analysis employs several assumptions:

- The filter works in a continuous-conduction mode, which means the filter's time constant is much greater than the pulse's repetition rate (period).
- The filter capacitor's charge and discharge time constants are the same. That means the impedance sourcing signal to the filter is much lower than the filter resistance and the filter's load impedance is much higher than the filter's resistance, which you can easily obtain by using an operational amplifier as a decoupling component.
- The filter's voltage grows in exponential steps (charging and discharging) that become smaller as the output voltage approaches its limit value.
- The filter is loaded with an impedance that is so high that it can be ignored.

We did the analysis with MathCAD 15, and anyone with the appropriate license can reproduce the results.

The expressions for the nth values of the filtered voltage's maximum, Vh, and minimum, Vlow, are:

$$Vh_n = Vlow_n + \left(V_A - Vlow_n\right)\cdot\left(1 - e^{\frac{-\tau_1}{\tau}}\right) \quad (1)$$

$$Vlow_n = Vh_{n-1}\left[e^{\frac{-(T-\tau_1)}{\tau}}\right] \quad (2)$$

where τ is the filter's time constant and τ_1 is the pulse duration *(Fig. 1)*. For simplicity, define:

$$\alpha = e^{\frac{-(T-\tau_1)}{\tau}} \quad (3)$$

$$\beta = 1 - e^{\frac{-\tau_1}{\tau}} \quad (4)$$

$$\gamma = e^{\frac{-\tau_1}{\tau}} \quad (5)$$

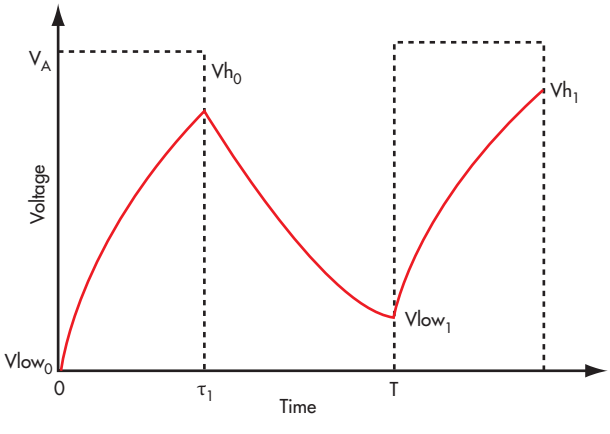
$$\tau_1 = DT \quad (6)$$

where D is the duty cycle of the input pulse train;

$$\tau = kT \quad (7)$$

where k is the number of periods for the filter time constant. So, Equations 1 and 2 become:

$$Vh_n = V_A\beta + Vlow_n\gamma \quad (8)$$



1. The plot of the input pulses (dashed lines) and filter output (solid lines) indicates the definition of the parameters used in the calculations.

$$Vlow_n = Vh_{(n-1)}\alpha \quad (9)$$

To derive the equation for the limit value of the filter output, you must use the recurrent equations for the low and high values and calculate the average, which is based on the initial parameters only. The equations for six high/low pairs are:

$Vh_0 = V_A\beta$
$Vlow_0 = 0$

$Vh_1 = V_A\beta(\gamma\alpha + 1)$
$Vlow_1 = V_A\beta\alpha$

$Vh_2 = V_A\beta(\gamma^2\alpha^2 + \gamma\alpha + 1)$
$Vlow_2 = V_A\beta\alpha(\gamma\alpha + 1)$

$Vh_3 = V_A\beta(\gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$
$Vlow_3 = V_A\beta\alpha(\gamma^2\alpha^2 + \gamma\alpha + 1)$

$Vh_4 = V_A\beta(\gamma^4\alpha^4 + \gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$
$Vlow_4 = V_A\beta\alpha(\gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$

$Vh_5 = V_A\beta(\gamma^5\alpha^5 + \gamma^4\alpha^4 + \gamma^3\alpha^3 + \gamma^2\alpha_2 + \gamma\alpha + 1)$
$Vlow_5 = V_A\beta\alpha(\gamma^4\alpha^4 + \gamma^3\alpha^3 + \gamma^2\alpha^2 + \gamma\alpha + 1)$

Note from the above equations that:

$$Vlow_n = V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right] \quad (10)$$

and:

$$Vh_n = V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right] \quad (11)$$

The average for the output voltage is:

$$V_{limit_n} = Vlow_n + \left(\frac{Vh_n - Vlow_n}{2}\right) \quad (12)$$

You can calculate the limit for the normalized output voltage using MathCAD tools:

$$Limit = \frac{V_A + V_A e^{\frac{D-1}{k}} - V_A e^{-\frac{1}{k}} - V_A e^{-\frac{D}{k}}}{V_A\left(2e^{-\frac{1}{k}} - 2\right)} \quad (13)$$

or:

$$Limit = \frac{e^{-\frac{D}{k}} - e^{\frac{1}{k}(D-1)} + e^{-\frac{1}{k}} - 1}{2e^{-\frac{1}{k}} - 2} \quad (14)$$

(See the derivation of Equations 13 and 14 in "Normalized Output Voltage Limit Derivation," p. 91.)

Equation 14 is a transcendent equation with two variables, which is hard to solve symbolically. But you can find the limit value graphically by fixing the value of k and plotting the limit as a function of the duty cycle, D. If k = 100.0:

$$Limit(D) = \frac{e^{-D\frac{1}{k}} - e^{D\frac{1}{k}}e^{-\frac{1}{k}} + e^{-\frac{1}{k}} - 1}{2\left(e^{-\frac{1}{k}} - 1\right)} \quad (15)$$

A plot of this function shows that the limit of the normalized RC filter output is the duty cycle, D *(Fig. 2)*. To create an example, assign values to the variables in Figure 1:

$V_A = 1$ V

$D = 0.6$

$T = 20$ µs

$\tau_1 = DT$

$k = 50$

$\tau = kT$

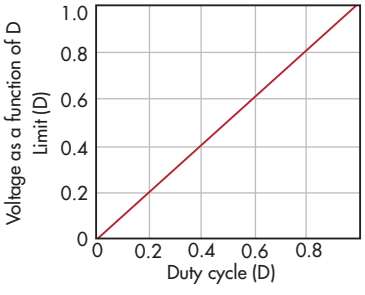
Then:

$\alpha = e^{-(T-\tau 1)/\tau} = 0.992$

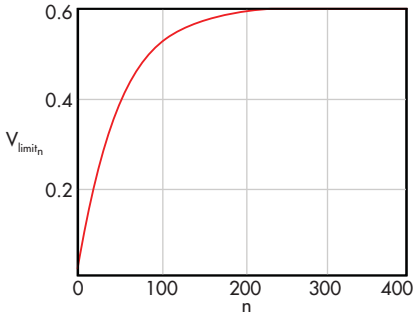
$\beta = 1 - e^{-\tau 1/\tau} = 0.012$

$\tau = e^{-\tau 1/\tau} = 0.988$

Then:



2. The normalized output voltage of the RC filter is the duty cycle value of the rectangular input pulses. The result does not depend on the value of k.



3. The limit value of the filtered voltage is equal to the input voltage's amplitude times the duty cycle.

$$\lim_{n\to\infty}\left[V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]+\frac{\left[V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right]-V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]\right]}{2}\right]\to 0.59999840001834787879(V) \quad (16)$$

To plot the graph for the limit, assign n = 1…400. Then:

$$Vlow_n = V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right] \quad (17)$$

$$Vh_n = V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right] \quad (18)$$

$$V_{limit_n} = \left[Vlow_n + \left(\frac{Vh_n - Vlow_n}{2}\right)\right] \quad (19)$$

Figure 3 shows the resulting plot.

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NORMALIZED OUTPUT VOLTAGE LIMIT DERIVATION

Equation 12 can be interpreted as:

$$\lim_{n\to\infty}\left[V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]+\frac{\left[V_A\beta\left[\sum_{m=0}^{n}\left(\gamma^m\alpha^m\right)\right]-V_A\beta\alpha\left[\sum_{m=0}^{n-1}\left(\gamma^m\alpha^m\right)\right]\right]}{2}\right] \quad (1)$$

Its solution is:

$$\begin{cases}\text{signum}(V_A\beta,0)(\infty) \text{ if } \alpha=\dfrac{1}{\gamma}\\ \lim_{n\to\infty}\left[\dfrac{V_A\beta\left(\gamma\gamma^n\alpha\alpha^n-1\right)}{2\gamma\alpha-2}+\dfrac{V_A\beta\alpha\left(\gamma^n\alpha^n-1\right)}{2\gamma\alpha-2}\right] \text{ if } \alpha\neq\dfrac{1}{\gamma}\end{cases} \quad (2)$$

Only the lower expression is of interest:

$$\lim_{n\to\infty}\left[\frac{V_A\beta\left(\gamma\gamma^n\alpha\alpha^n-1\right)}{2\gamma\alpha-2}+\frac{V_A\beta\alpha\left(\gamma^n\alpha^n-1\right)}{2\gamma\alpha-2}\right] \quad (3)$$

Its solution is:

$$\begin{cases}0 \text{ if } \alpha=\dfrac{1}{\gamma}\\ \dfrac{V_A\beta\left(\alpha-\alpha\infty+1\right)}{2\gamma\alpha-2} \text{ if } 1<\gamma\alpha\\ \dfrac{V_A\beta\left(\alpha+1\right)}{2\gamma\alpha-2} \text{ if } \gamma|\alpha|<1\end{cases} \quad (4)$$

Again, only the lower expression is of interest:

$$-\left[\frac{V_A\left[1-e^{\frac{-DT}{kT}}\right]\left[e^{\frac{-(T-DT)}{kT}}+1\right]}{2\left(e^{\frac{-DT}{kT}}\right)\left(e^{\frac{-(T-DT)}{kT}}\right)-2}\right] \quad (5)$$

which can be converted into Equation 13.