Electronic Design

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JESD204C: A New Fast Interface Standard for Critical Applications

Sponsored by Texas Instruments: To meet the demands of interconnecting today's ever-faster ADCs/DACs to the latest processors and FPGAs, JEDEC upgraded its JESD standard.

As data-conversion circuits have sped up over the years, the current serial interfaces haven't been able to keep pace. But a new interface has arrived, called JESD204C. It's the next iteration of the JESD interface standards. This article introduces JESD204C, explains its features and benefits, and highlights the differences with its predecessor JESD204B.

What is JESD?

JESD204C is a standard of the Joint Electron Devices Engineering Council (JEDEC). It's a high-speed interface designed to interconnect fast analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to high-speed processors, FPGAs, and ASICs.

The standard first appeared in 2006, offering a 3.125-Gb/s data rate. Subsequent releases implemented improvements in function and speed. The JESD204A version in 2008 added lane synchronization that kept multiple serial lanes aligned with multiple converters. The JESD204B upgrade in 2011 boosted speed to 12.5 Gb/s and incorporated deterministic latency. With the new JESD204C version, the interface data rate jumps to 32.5 Gb/s, along with other improvements in the mix. By the way, the newer versions of the standard maintain some backward compatibility with previous versions.

Year after year, ADCs and DACs continue to push the envelope when it comes to speed. Gigabit rates are common. And those circuits transmitting or receiving this high-speed data, such as FPGAs or fast MPUs, have been able to match these perpetual speed increases.

However, the limiting factor has revolved around interconnecting these devices.

The previous JESD204B standard became widely used to allow these fast circuits to talk with one another. Data exchanges take place between chips on a PCB, on backplanes, and via short cables between modules or subassemblies in an instrument or other equipment. But as some have found, the JESD204B specification is no longer adequate to interface the fastest data-conversion circuits. Now, JESD204C brings the interfaces up to speed.

Applications

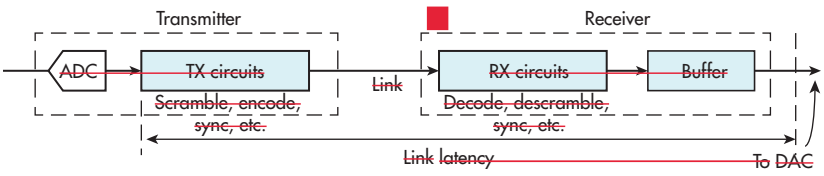
The JESD204C interface can benefit almost any design where data converters run at high megabit and gigabit data rates. A sampling of the applications includes:

- Test instruments
- 5G cellular equipment
- Other cellular base-station gear
- Medical apparatus
- Military/electronic warfare (EW)
- Satellite
- Almost any direct-conversion software-defined radio (SDR)

JESD204B and JESD204C Compared

The JESD204B standard was a real breakthrough and has been widely adopted. It offered a 12.5-Gb/s data rate, multiple lane support and synchronization, 8B/10B encoding, and deterministic latency. The JESD204C standard has all of the features of its predecessor plus some added new benefits such as the 32.5-Gb/s data rate, 64B/66B encoding, and deterministic latency.

The key addition to the standard is the 64B/66B encoding. It also supports a 64B/80B encoding option. The encoding method used in the earlier B version of the standard is



The diagram shows a simplified representation of a JESD204C link.

8B/10B, which means that each 8 bits to be transmitted is first converted into a unique 10-bit number. There are a couple of good reasons for such encoding:

- The encoded character now contains more bits and bit transitions that are helpful in clock recovery and the alignment of the data streams.
- The encoding ensures that the average dc on the line is constant. Random numbers of bits cause a varying or wandering dc average on the transmission path that can introduce bit errors and cause other annoying operational characteristics.

While 8B/10B encoding is beneficial, it also slows down the transmission. Ten bits are transmitted instead of eight, so it takes longer. While the data rate (R) is still based on the bit time (t), the net data rate is 20% less. (R = 1/t)

The JESD204C standard uses 64B/66B encoding. It not only improves dc balance, clock recovery, and data alignment, but also has a much smaller bit overhead of 3.125%, considerably less than the 8B/10B method.

The signal processing includes a scrambler prior to the encoding. A scrambler is a digital circuit that processes the serial data to create a highly randomized version. Like a cyclic redundancy check (CRC), it uses an algorithmic process based on a polynomial, in this case $1 + x^{14} + x^{15}$. The end effect of scrambling is a serial digital signal with a spectrum that greatly reduces the generation of EMI.

Deterministic Latency

Determinism is the characteristic of being able to predict or determine when certain actions will occur. The opposite of determinism is randomness. Something that's deterministic can predict when operations will happen with precision and repeatability.

Latency is the time delay that occurs between the start of an operation and its end. Latency in general is the total time that it takes for an electronic operation to take place or a signal to travel from one part of the system to another. Latency is measured in seconds or clock cycles.

The combination of the two is critical to the actual performance of this device or equipment. Examples include equipment that have two or more data converters for things like I & Q conversion. Interleaved converters are another example. When multiple inputs or outputs must be phase-coherent, the JESD204C standard can provide that condition. The resulting deterministic latency must be constant and repeatable for proper operation in most systems.

The latency of an ADC is the time between the capturing of the analog sample, the subsequent processing by the ADC, and the appearance of the digital output. The latency of a DAC is similar—the time between the digital input to the DAC circuits and when the corresponding analog signal first appears. This latency is measured in seconds or by the number of clock cycles.

Deterministic latency is generally defined as the time between the occurrence of the data input to the transmitter and output at the receiver. It doesn't include the ADC and DAC latencies *(see figure)*. The ADC develops the signal that's processed into the frame of data to be transmitted. The transmitter (TX) circuit processing includes scrambling, 8B/10B or 64B/66B encoding, and some alignment of data. The data is transmitted over the serial link, possibly in parallel with other serial links associated with multiple ADCs.

At the receiver (RX), the signals are decoded and synchronized, then descrambled. A buffer memory is used to provide some timing adjustment if needed. Note the total link latency that must be consistent to achieve deterministic latency.

In most high-speed applications, it's essential that data from multiple streams pass through the system with a consistent known delay. The standard defines some signals to achieve that goal. Different signals and clocks help deliver lane synchronization, lane alignment, and error detection.

The primary clocks are the data frame clock and the Local Multi-Frame Clock (LMFC). The SYSREF and SYNC signals are used to provide time reference alignment. SYNC is a receiver-to-transmitter signal that's used for synchronization requests and error reporting. A SYSREF signal is a phase timing reference that influences the LMFC.

The JESD204C standard is sophisticated and complex. To enhance your understanding of its features, benefits, and operational details, go to the links below. The standard itself can be accessed at the JEDEC website. www.jedec.org