

FIB Circuit Edit Becomes Increasingly Valuable In Advanced Node Design

[Electronic Design](#)

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A technique used on older process nodes is providing even more valuable benefits as IC designers work on devices that will be manufactured at advanced technology nodes including 28 nm and beyond. Now that it takes \$10 million or more to bring a device to market, focused ion beam (FIB) circuit edit has become strategically important for reducing costs, optimizing performance and functionality, mitigating risk, and speeding time-to-market for complex device designs.

IC designers will encounter many new problems at advanced process nodes that would be difficult, if not impossible, to anticipate based on previous design work. EDA tool providers are already addressing the difficulty of advanced node design with advice about design flow and other ways to handle numerous technical challenges. In addition to applying these new design flow modifications, developers can apply FIB circuit editing to the process of debugging and validating fixes or exploring design optimization changes before committing to the high cost or lengthy timetables of a full mask spin.

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Challenges At Advanced Process Nodes

At advanced process nodes, success barriers are magnified because of high mask costs and greater difficulty in finding and fixing bugs. Designers will encounter many new problems at advanced process nodes that would be difficult, if not impossible, to anticipate based on previous design work.

Chips manufactured at 20-nm process nodes have feature sizes 10 times smaller than the wavelength of the laser light typically used in lithography. Pre-silicon testing is growing extremely tedious, simulations are taking excessively longer, and many designs simply cannot be 100% verified. Extremely complex designs may have imperfect simulation models, and packaging can stress sensitive devices.

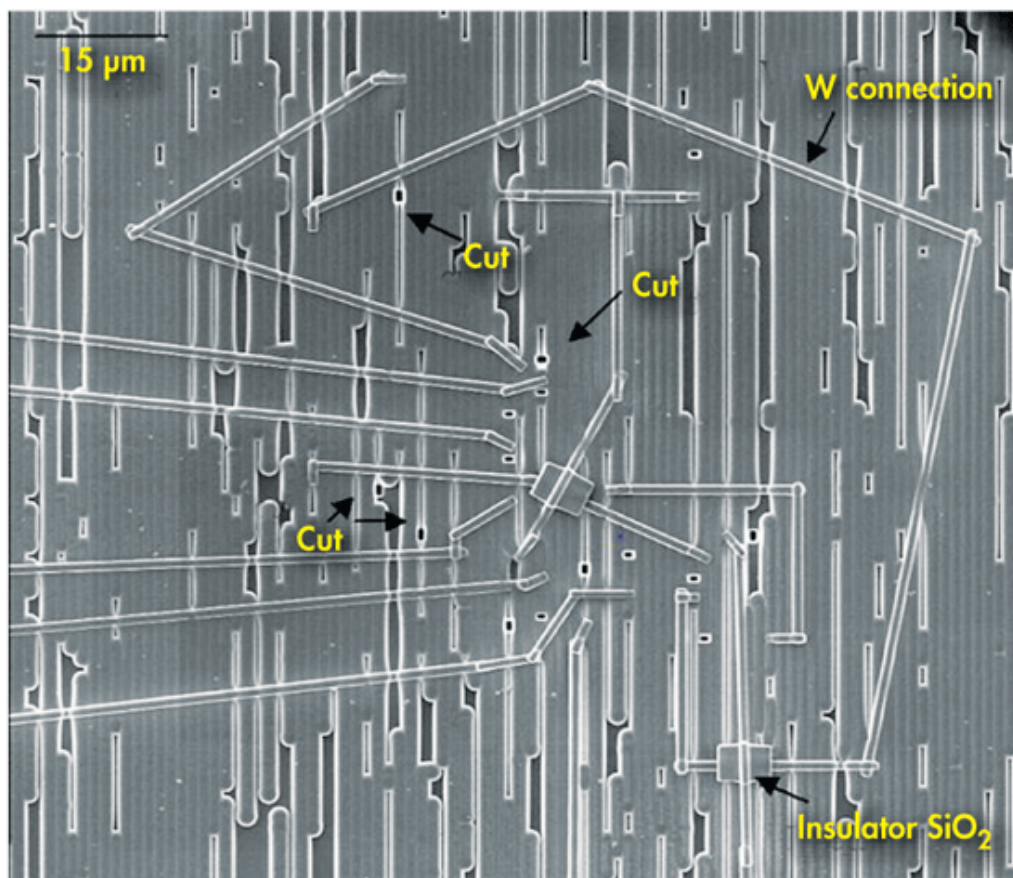
Challenges in this environment range from multiple patterning and layout-dependent effects (LDE) to the use of local interconnect layers, and each new technology node brings design and integration complexity to a new level. Server signals and power electro-migration also create challenges. Decreasing metal pitch leads to coupling effects and signal integrity issues. Increasing wire and via resistance requires more advanced and variable wire sizing and tapering techniques.

Extraction, timing, signal integrity analysis, and modeling also must account for many variation issues to achieve accuracy without compromising performance. Lithography limitations at 20 nm often require a great deal of fixing to achieve signoff. Moreover, there are multiple chip and intellectual property (IP) integration challenges, packaging issues, and additional complexity as these issues interact.

EDA tool providers are already addressing the difficulty of advanced node design with advice around design flow and other ways to handle numerous technical challenges. This is not enough, however. In addition to applying these new design flow modifications, developers can apply FIB circuit editing with their early prototypes during debug or simply to explore design optimization opportunities by quickly and inexpensively implementing and creating physical prototypes that can be tested and validated before committing to the high cost or lengthy timetables of a full mask spin. FIB-edited device prototypes can be used to guide one-time modifications to masks, eliminating the need for a trial-and-error approach with successive versions of masks.

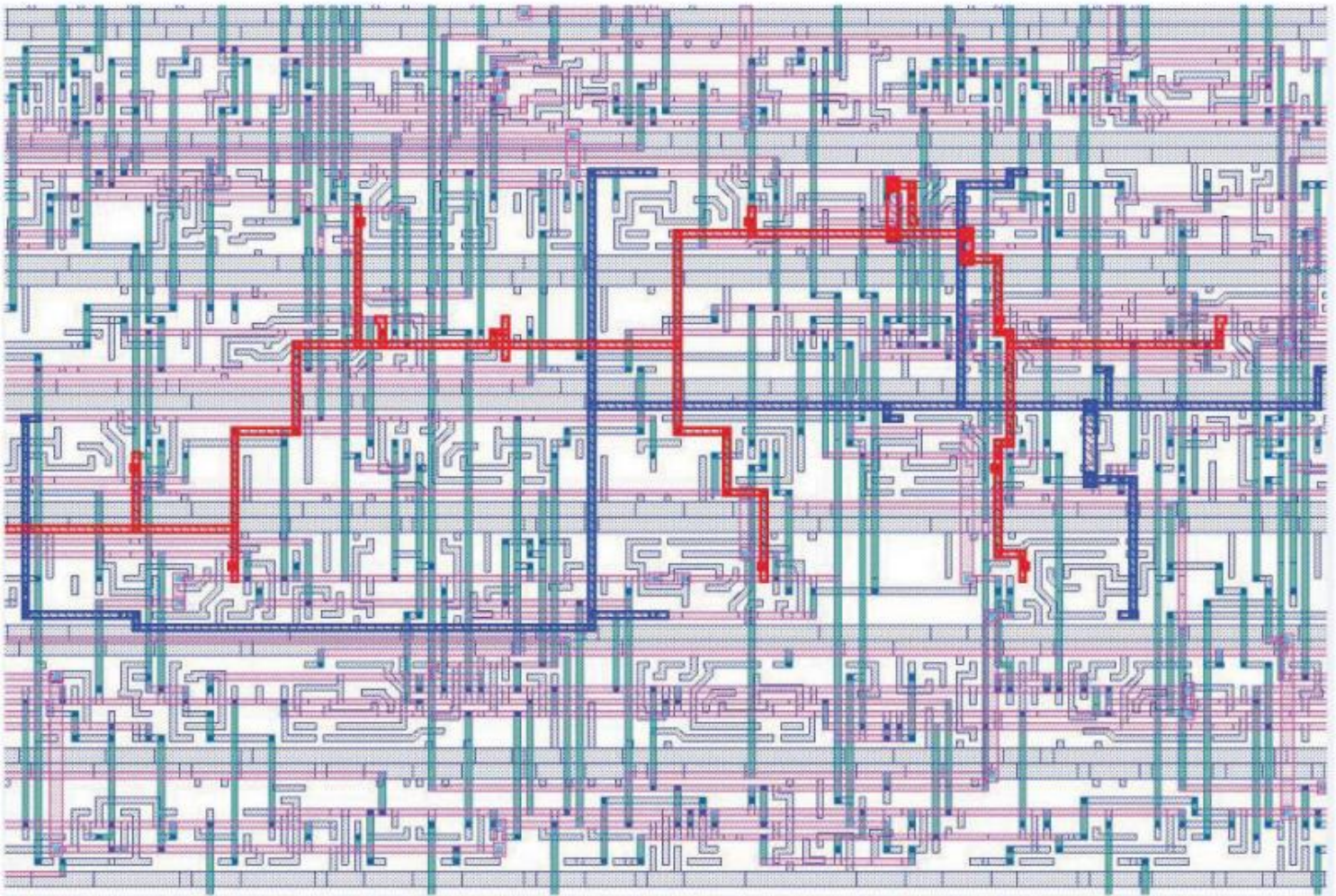
FIB Circuit Edit Capabilities

FIB systems have many uses in the semiconductor industry, as well as in the fabrication of microelectromechanical systems (MEMS) and in biological studies. In the semiconductor industry, a primary use for FIB systems is in circuit edit, allowing designers to cut traces or add metal connections within a chip (*Fig. 1*). FIB edits can be done quickly and easily, at a small fraction of the \$5 million to \$10 million in costs that are typical for a new lot of wafers in a fab. With today's state-of-the-art equipment, it is possible to edit circuits fabricated with 28-nm and smaller technology nodes and featuring multiple-layer metal stacks and in flip-chip and other advanced chip-scale form factors.



FIB circuit edit works by using a finely focused gallium (Ga^+) ion beam with nanoscale resolution to image, etch, and deposit materials on an IC with an extremely high level of precision. This process of removing and depositing materials enables designers to cut and connect circuitry within the live device and to create probe points for electrical test. It is the equivalent of performing microsurgery on IC devices. The high-energy Ga^+ beam can mill through conductors, and it uses various types of gases to either enhance milling precision or more effectively deposit conductive and dielectric materials. For instance, by utilizing the appropriate gas chemistries, a choice of tungsten, platinum, or silicon dioxide can be very precisely deposited using the ion beam.

To execute circuit edits, the FIB tool is coupled to a CAD navigation system that makes it possible to locate the area of interest. Typically, FIB circuit edit uses GDS files from the designer to navigate to the precise area. This provides a method to find subsurface features and ensure that the right edits are made (*Fig. 2*). Accurate positioning of the ion beam is among the most important requirements for circuit edit using FIB systems.



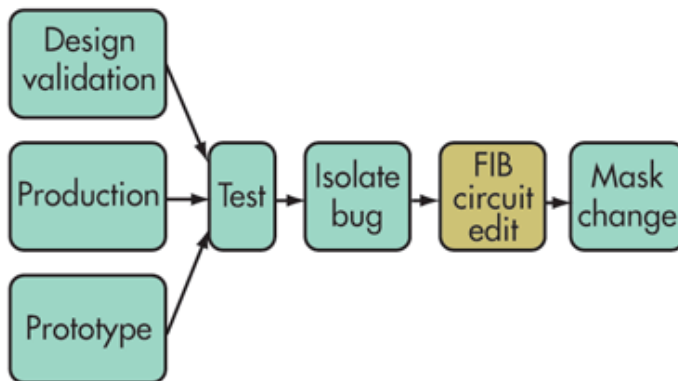
FIB Circuit Edit Applications

There are numerous applications for FIB circuit edit at every commercially available node. It can be used to verify design change on the tester and validate design change at the system board level. Typical applications include:

- Debugging and optimizing devices in production: FIB circuit edits are often performed once a design flaw has been identified to ensure that the proposed fix will solve the complete problem. Designers can repair mask errors and know that the device will work after one and not two mask spins, while also expediting the next steps in terms of software development and still getting working prototypes into customers' hands. With cycle times becoming more and more compressed in market segments such as mobile devices, a week of lost cycle time can be extremely damaging to a successful product rollout.
- Exploring and validating design changes: Simulation isn't everything when it comes to optimizing designs, and FIB circuit edit takes designers beyond simulation to the ultimate in emulation capabilities. Designers can try derivatives of device designs and observe the results of those changes, including options like cutaway fuses or other functional changes, experimenting with them on a live device before committing to the cost or timetable of a complex mask spin.
- Prototyping new devices without costly and time-consuming mask set fabrication: FIB prototype devices are often used to enable next-level testing to get a jumpstart on the next round of device debug. FIB circuit edit accelerates development cycles because it eliminates the need for multiple rounds of prototype tests and mask modification cycles. Designers can implement and evaluate the results of circuit changes on physical prototypes that will optimize or correct flaws in the design before committing to them in a new mask spin. What would otherwise cost \$5 million to \$10 million in wafer costs and six to eight weeks in wafer processing cycle time can be done for hundreds or thousands of dollars in a matter of hours, ensuring that only one additional wafer spin will be required.

- **Scaling fixes:** Once the fix has been verified on a prototype using FIB circuit edit, it is possible to duplicate that fix on a handful or tens of devices to provide internal test, validation, and qualification teams and even customer samples. This ensures that further system or application development work can take place in parallel while waiting for the mask spin and final production devices to come back.
- **Accelerating time-to-market:** Delivering on time to customers is critical since their product designs are on hold until they can get devices. FIB circuit edit speeds up the whole cycle for getting customers into production and avoiding loss of reputation, or potential competitors getting their foot in the door. Some large OEM customers also place penalties on late delivery of chips, which can sometimes reach millions of dollars.

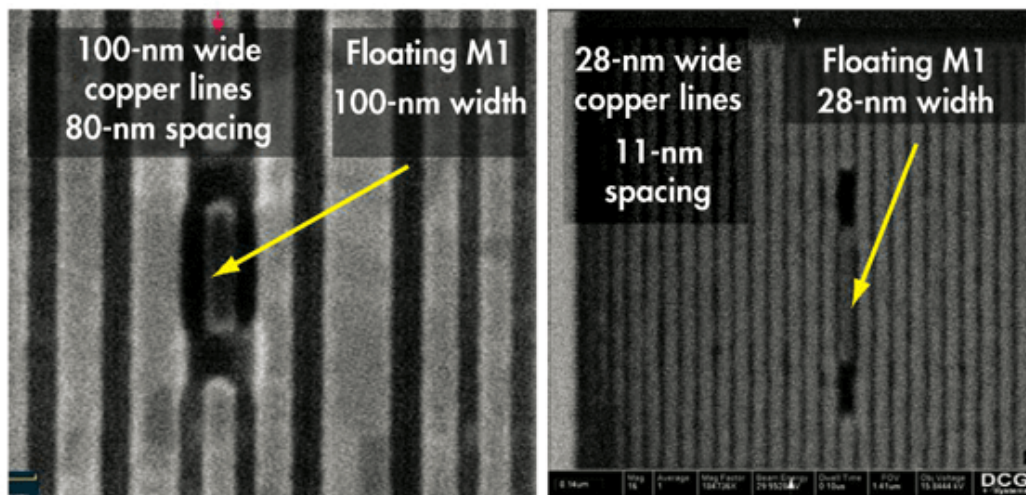
Figure 3 shows how best to integrate FIB circuit edit into the overall process of developing and testing IC designs.



Improvement Continues

There is a misperception that FIB circuit edit only works well at 90-nm and 65-nm process nodes and has “run out of gas” at anything below. But this is not true. Thanks to tool and methodology advances that have been derived from the experience of dedicated teams running thousands of circuit edit hours/months, FIB circuit edit can be used for more precise beam guidance, operate in smaller areas, perform more intricate operations on both the back and front sides of the device, and handle copper layers.

A major area of development for FIB circuit edit has been tool advances that provide better aspect ratios for smaller cuts as part of the solution. There have been important advances in areas such as ion beam resolution, operating software, and CAD navigation, all of which bring greater capabilities to FIB systems. Indeed, ion beam resolution advances have been critical for recognizing small features, aiding in visual end-pointing, enabling precise CAD alignment, and improving box placement accuracy (*Fig. 4*).



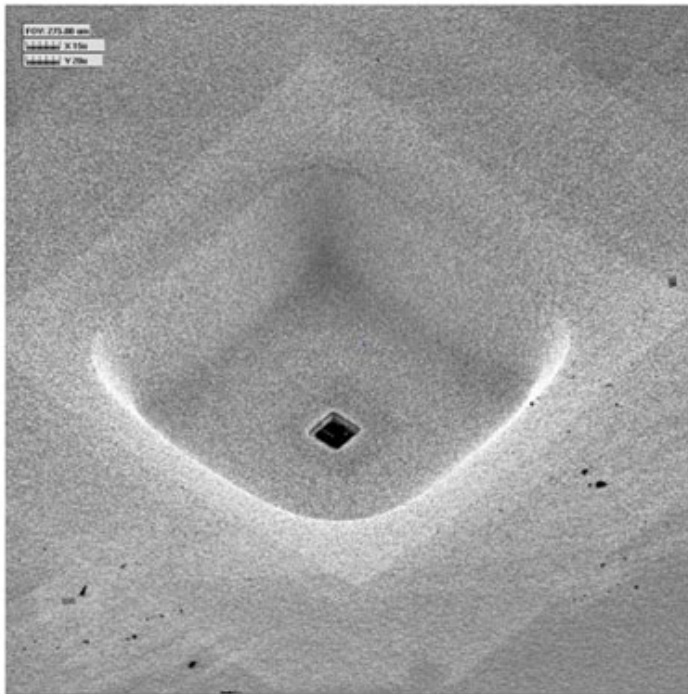
Tool advances don't tell the whole story, however. FIB tools are not entirely automated, and there is no underestimating the critical importance of how experienced FIB operators are. In fact, this expertise is key to the success of circuit edit work. Endpoint detection, or the ability to know when selected layers of interest have been successfully etched, continues to require a high level of skill to achieve high success rates. The need for operator skill in this area is even more pronounced at smaller geometries, as well as during the most challenging FIB operations. Also important is the unique knowledge that operators must have in such areas as IC circuitry, IC process technology, ion milling patterns, and the general basics of how to use a FIB tool.

Achieving this level of expertise can be difficult for an in-house operation. Often, larger semiconductor companies that already conduct some level of circuit edit will augment these resources with external service labs that have deeper and more extensive experience in solving the toughest FIB circuit edit challenges. Few small and mid-sized companies can bear the expense of purchasing a FIB tool that might cost on the order of more than \$1 million, and even if they could afford the tool, they would be unlikely to have staff with the right experience to most effectively operate it. Most tend to go straight to an external lab. Today's labs can implement circuit edits to support basic electrical design characterization or verification of redesign parameter, and a full range of debug tools enables designers to solve difficult logic failures and other anomalies.

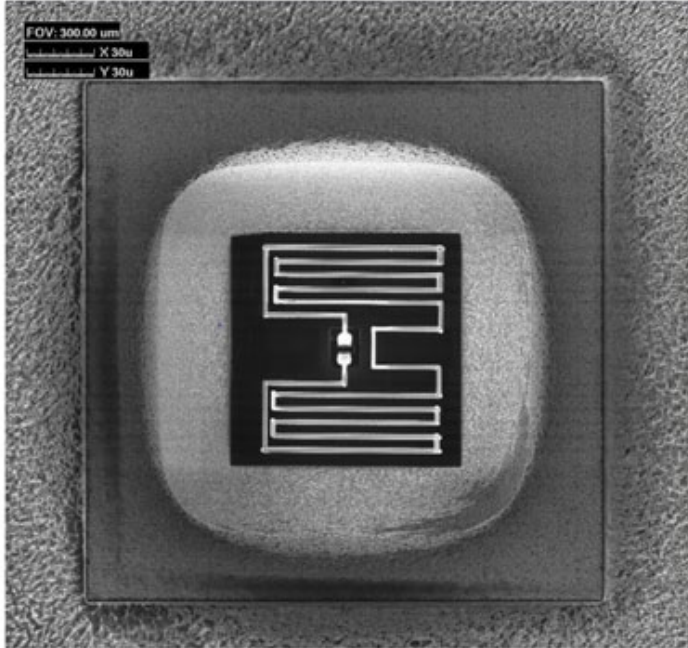
Best Practices: Part Art, Part Science

There are a number of key prerequisites for FIB circuit edit success:

- **Tools:** High resolution is particularly important at advanced nodes such as 28 nm and 20 nm. It generally requires a 0.1- μm resolution (or aspect) ratio as well as a trenching approach that supports a finer resolution to make these edits. With today's equipment, the smallest hole that can be made is 0.1 by 0.1 μm with an aspect ratio of 1/20. For most 20-nm and 28-nm cases, it is impossible to make a small enough hole to reach the target. To do this, specialized FIB techniques are required to decrease the aspect ratio and gain access to the target. This includes an ability to smoothly remove dummy metal above the target metal layer, and it requires deep and extensive knowledge of IC circuitry and processes, FIB tools, and ion milling patterns. Figure 5 shows a typical back-side trench.



- **Backside and frontside editing:** Many believe that flip-chip FIB circuit edit only can be performed from the top of the device, and neither backside nor frontside editing is possible. Not only is this not true, but frequently backside edit is the most effective way to operate, either because of substrate material in flip-chip packaging or because of the increased number of metal circuit layers in today's ICs that make it harder to get to a lower layer when editing from the top. Figure 6 shows a backside FIB circuit edit in which a resistor is introduced across two nodes.



- **Handling copper layers:** Most 28-nm and 20-nm devices are copper devices featuring a crystal structure that is very difficult to remove smoothly. Special methods are required, and the engineer's experience is extremely important to ensure the metal is removed smoothly with a very high level of quality. Also, accurate beam positioning is more challenging for copper metal devices due to the non-visibility of the circuit patterns. This is also important for aluminum metal devices if there are no unique patterns to recognize on the top level.
- **Companion failure analysis and test tools, expertise, and capabilities:** Because most devices must ultimately get into packages, there should be a smooth transition to de-capping or de-lidding them and performing micro-probing and other debugging tests on FIB-edited parts.
- **Front-end expertise:** Semiconductor advanced technology nodes not only present challenges due to ever shrinking nanoscale geometries, they also introduce new front-end materials as processes evolve. FIB circuit edit labs then can benefit from being part of a larger lab environment characterized by a significant level of front-end process understanding and materials expertise. Labs that support process R&D activity and yield support will offer an advantage and insights, as well as other know-how that will help maximize the success of FIB circuit edit strategies.

Conclusion

IC design verification and validation will continue to become more and more difficult as the industry moves to smaller and smaller nanoscale geometries. Far from obsolete at today's advanced nodes, FIB circuit edit is becoming increasingly valuable for improving the success rates for these designs, which often can cost \$10 million or more to bring to market. Thanks to advances in both tool technology and best practices, FIB circuit edit can be used for a variety of purposes including debugging and validating fixes, as well as earlier in the process to explore opportunities for design optimization, without having to commit to a full mask spin.



Taqi Mohiuddin joined Evans Analytical Group (EAG) in 2013 to lead sales and marketing for the MTE division. He brings more than 18 years of diverse experience with startup, early growth, and established multinational corporations in software, systems, and semiconductor market segments. His previous roles include leading solutions marketing for the Motorola Solutions Enterprise Networks Division, vice president of marketing and business development for Siverge, and executive director of marketing for Mindspeed Technologies. He holds an MBA from DePaul University and a BS in electrical engineering from the University of Illinois at Chicago. He is also a co-author of a LabVIEW programming book. He can be reached at taqi@eag.com.

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