How HyperBus Delivers 330 Mbyte/s Using A Dozen Signals

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Spansion could not get enough performance out of a dual quad SPI (QSPI) interface for its latest NOR HyperFlash chip so it created HyperBus. HyperBus is capable of delivering 330 Mbytes/s using only twelve signals including n 8-bit bus.

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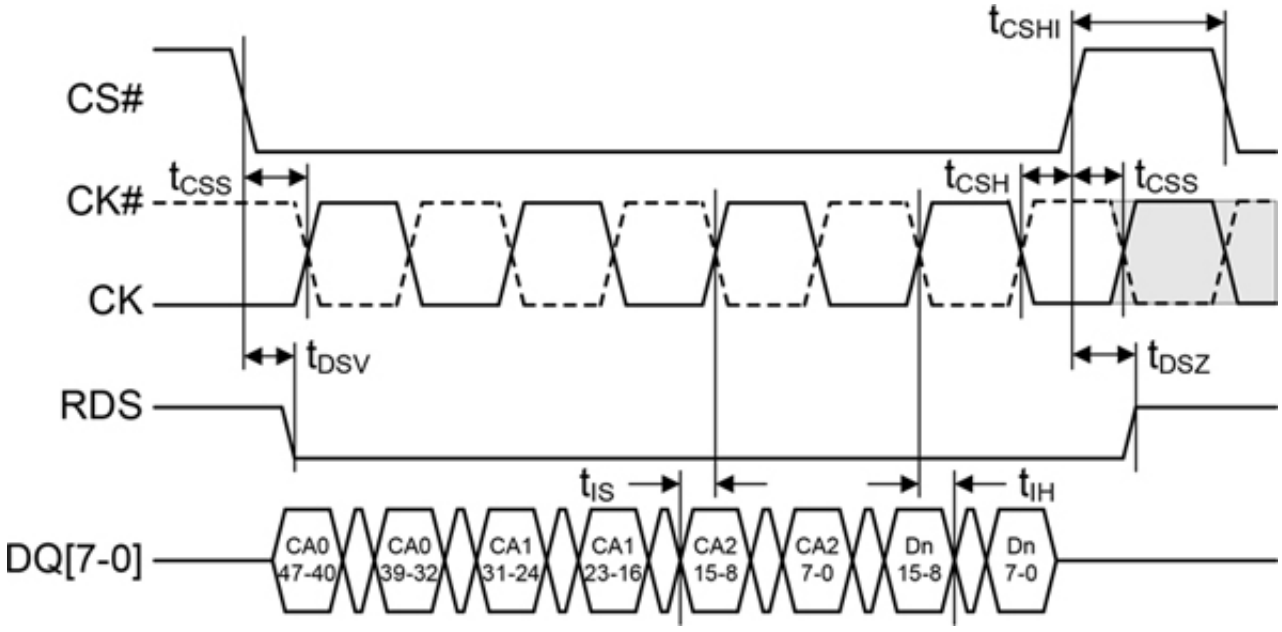
The HyperBus operates at 1.8 V and 3 V. The latter runs with a 100 MHz clock and uses only eleven lines since it does not use a differential clock. The 1.8 V version uses CK and CK# signals.

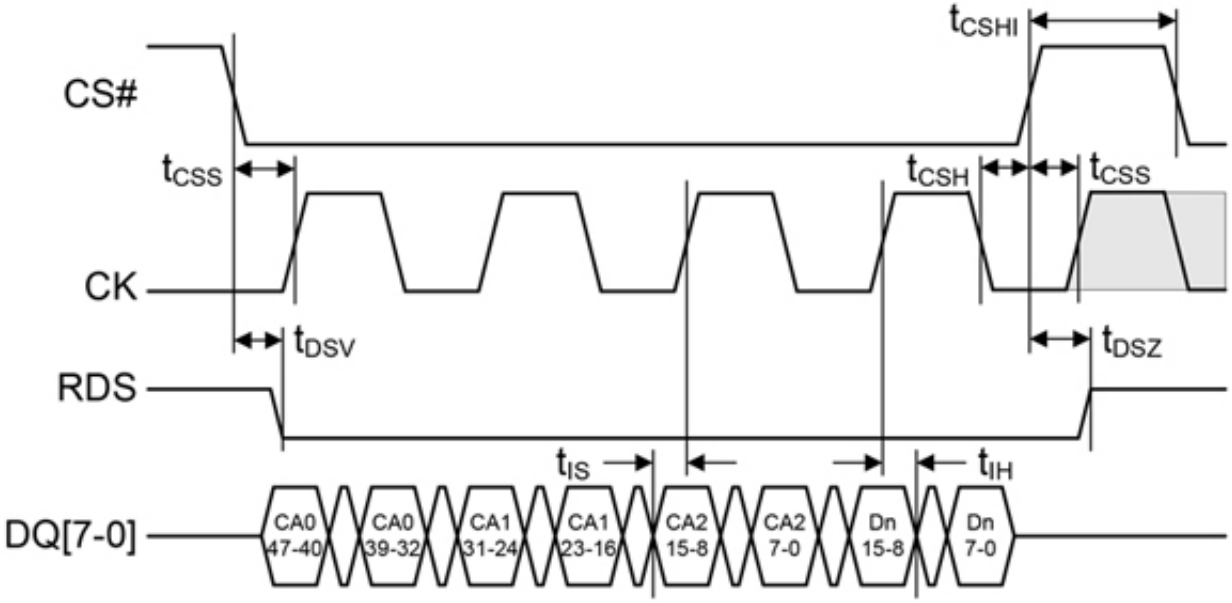
HyperBus operation is relatively simple. Each transaction begins with a six byte command/address sequence. Three bits of the first byte are used for the commands that include read, write and burst mode. This leaves 45 bits for addressing although a few more bits may be reserved for future use. That would still leave a 40 bit address space.

The write transaction for the 1.8 V writes two bytes of data *(Fig. 1)*. The read data strobe (RDS) is not used for write transactions. The delay until the next transaction is usually enough for a flash device to store the data. Multiple writes are handled via multiple transactions.

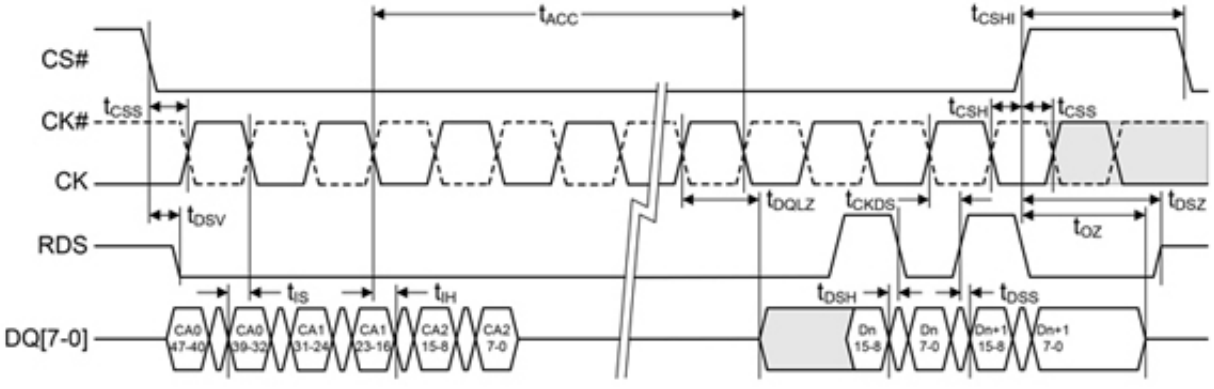


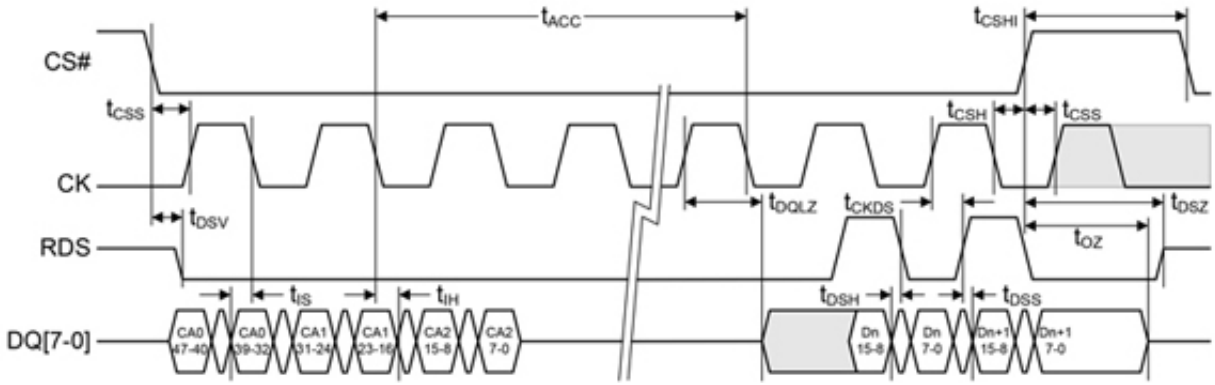
The 1.8 V clock rate is 166 MHz. The transfers are double data rate (DDR) hence the 333 Mbyte/s transfer rate.

The 3 V version has the same timing sequence writing two bytes *(Fig. 2)* but it uses only the CK signal. It also runs at 100 MHz. This version still delivers better performance (200 Mbyte/s) than dual quad SPI (QSPI) interfaces. The typical QSPI pumps out data at 40 to 66 Mbytes/s. Parallel NOR flash runs at rates from 70 to 96 Mbytes/s.



RDS comes into play with read transactions *(Fig. 3)*. The 3 V version simply uses the CK signal. The six byte header starts things off. At this point the host waits until RDS goes high At this point the device begins sending data to the host. Sequential data is provided until the host terminates the transfer. The host terminates the transfer by raising the chip select (CS) line.





The Spansion HyperFlash is a NOR flash device that supports HyperBus. It supports a wrapped burst mode of 16, 32 and 64 bytes.

Multiple HyperBus devices can operate using the same data and control lines but each requires their own chip select line. In theory, it would be possible to use reserved bits for addressing but that is not something the current crop of devices will support. In practice, a single device will be the normal configuration.

HyperBus fills a large performance gap with an interface that should be easy to implement on most hosts unlike more powerful interfaces like MIPI/M-PHY and PCI Express. These serial interfaces operate at a significantly higher clock rate and using more sophisticated protocols. They have their advantages but tend to be overkill for many midrange embedded applications.

HyperBus fits above I^2C and SPI. These use fewer lines but at a much slower transfer rate. There are still plenty of applications for these slower interfaces and many devices that support them. Devices that support HyperBus will probably include support for these as well.

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