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Multi-Protocol ICs Drive Data Networks

Electronic Design

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Wed, 2013-12-04 14:10

With high-speed serial standards moving to ever-faster speeds, designers must find new methods for maintaining signal integrity within their systems. Also, standards typically are application-specific with varying demands on signaling, channel training, and the physical-layer (PHY) rate. Fortunately, various standards and signaling requirements are working with a new generation of devices to improve signal integrity across multiple protocols.

Introduction

High-speed serialized interconnects evolved from their parallel bus ancestors to eliminate skew and move to higher throughput. Many serial standards today have maintained the architecture of their predecessors, but they have serialized the PHY to allow higher speeds and eliminate difficulty with electrically matching transmission lines.

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Western Digital developed the parallel AT attachment (PATA or simply ATA) standard to connect integrated drive electronics (IDE) hard drives to IBM "AT" and clone computers through a standard interface. It was based on a 16-bit Industry Standard Architecture (ISA) bus and remained software-compatible with the original ST-506 hard-drive controller standard developed years earlier by Seagate Technologies.

The parallel interface was limited to 133 Mbytes/s and roughly 18 inches due to inadequacies in the PHY. To overcome these limitations, the Serialized ATA (SATA) version 1.0 standard was released in 2003. It pushed the speed higher to 1.5 Gbits/s (roughly 150 Mbytes/s due to encoding). The serialization of the bus allowed the clock to be embedded within the stream and eliminated bus skew (by eliminating the parallel bus).

Additionally, the new standard used full duplex differential *low-voltage differential signaling* (LVDS) signaling. This reduced both electromagnetic interference (EMI) and power consumption, versus the transistor-transistor logic (TTL) level signaling of the parallel standard.

The switch from parallel to serial has become ubiquitous and the legacy buses still can be found, even in today's chip sets. The peripheral component interconnect (PCI) bus followed the ISA bus, which still exists as the low-pin count (LPC) bus connecting super I/O devices on PC motherboards.

The parallel PCI bus also has undergone a serialization and has become the universal interconnection standard for both

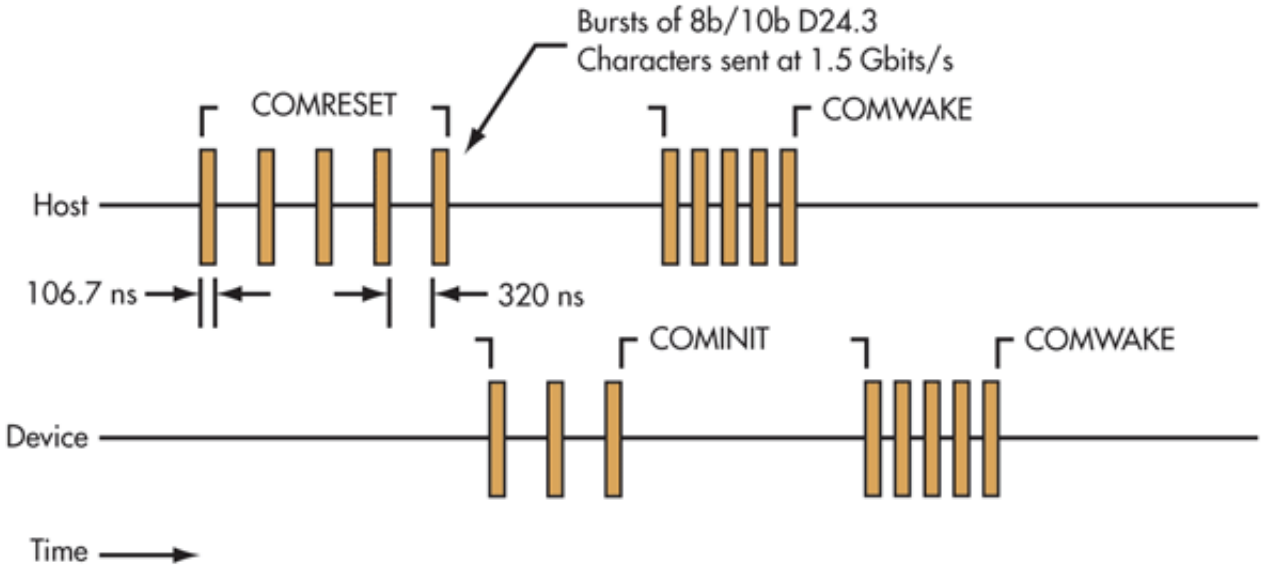
inside and between computing platforms and peripherals. In addition, the small computer systems interface (SCSI) has been serialized and has become simply serial attached SCSI or SAS.

Out-Of-Band Signaling

An interesting problem faced by committee engineers was to find a way to provide forward and backward compatibility when the clock rate is unknown. Also, control information needed to be passed to devices before the device was fully initialized, such as bringing a drive out of standby. This was accomplished by placing those control signals "out of band" (OOB).

OOB communication is simply a lower-bit-rate signaling scheme that utilizes the same channel. In SAS and SATA, the OOB symbols are created by intervals of 8b/10b encoded characters (D24.3 characters are used for COMRESET and COMWAKE) running at 1.5 Gbits/s.

By changing the intervals and counts of these bursts, information can be sent to any SAS or SATA drive independent of the standard revision it supports. This future-proofs the drives and allows backward compatibility with older host controllers. Figure 1 illustrates a SATA host adapter talking to a drive during initialization.



Breaking The Serialization Rate Barrier

An interesting consequence of serialization is the instant increase in per-channel data rate. The original insulation displacement connectors (IDC) and ribbon wire of the PATA and SCSI interfaces worked fine due to the low signal rate of each channel or bit. Simply increasing the width of these parallel buses increased the bandwidth without increasing the channel speed. In serial bus architectures, the transmission rate is one knob that can be turned to increase throughput and often has been used as standards evolve.

An example of this is the migration from SATA 1.0 to SATA 2.0 where the bit rate was increased from 1.5 to 3.0 Gbits/s while keeping the rest of the encoding the same (8b/10b). This is also true of other standards such as PCI Express (PCIe), which is now working on revision 4 targeting a 16-Gbit/s PHY data rate.

More efficient coding can improve the throughput at higher speeds. PCIe generation 3 moved from the previous 8b/10b encoding to 128b/130b. This reduces the encoding overhead to approximately 1.54% down from 20% for PCIe generation 2:

$$P_e = 100\frac{B_e - B}{B_e}$$

In the calculation for encoding overhead, P_e is the percentage encoding overhead, B is uncoded bits, and B_e is encoded bits. For example, P_e = 100*(10–8)/10 = 20% for 8b/10b. This allows the PHY rate of 8 Gbits/s while still maintaining a doubling of the throughput compared to the prior revision.

High-frequency losses, impairments, and reflections affect the shape of the waveform that represents the bits in the stream as transmission speeds increase. If left unchecked, these characteristics can lead to errors in receiving and decoding the stream.

PCIe 1.0 used a 2.5-Gbit/s data rate that, in many cases with careful layout, can run the length of a server (30 inches or more) and still adhere to the standard at the PCIe connector. However, take that same careful layout using PCIe 3.0 and it may fail to interoperate with standard PCIe peripherals due to an increased bit error rate.

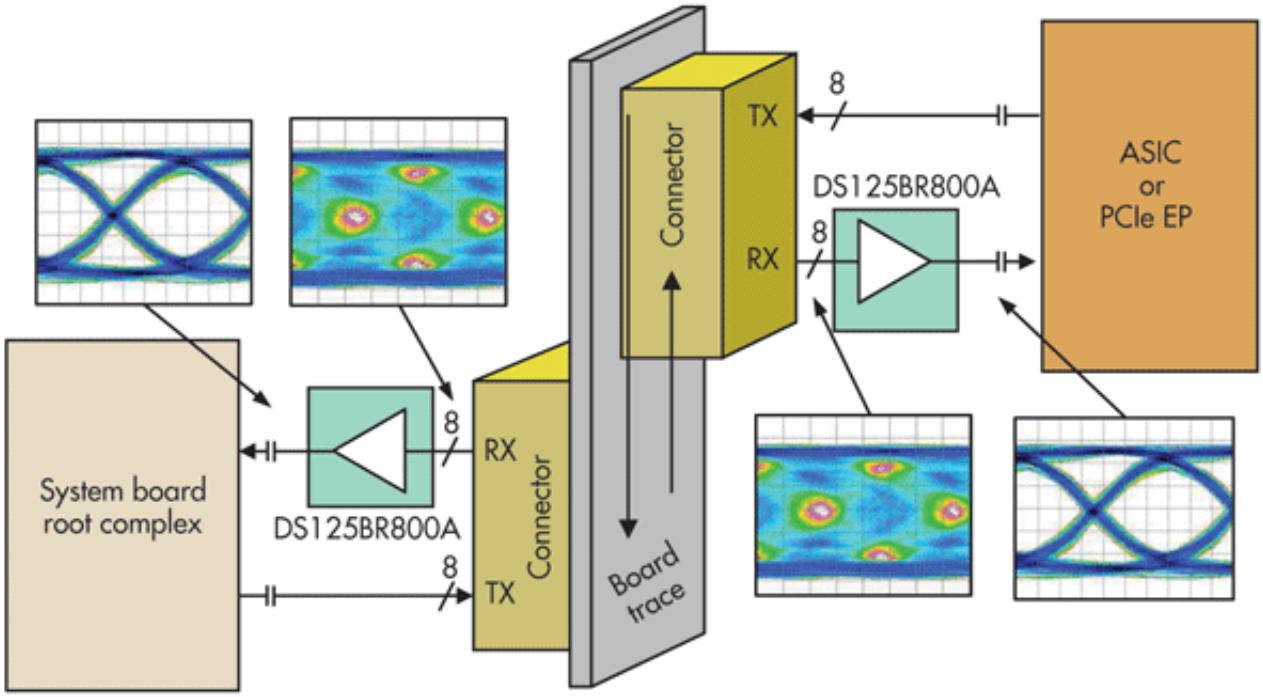
To solve this problem, an engineer can employ several options. One is to use a lower-loss dielectric such as Nelco N4000-13 or something more exotic such as Panasonic's Polytetrafluoroethylene-based Megtron 6. These reduce the high-frequency linear loss characteristics of the transmission line, so more of the signal can reach the receiver. The problem with this approach is the increased cost of the material as well as limited supply and availability of fabricators.

Another approach is to provide active methods to compensate for channel loss. This is accomplished by placing a *repeater* device comprising a receiver capable of equalization, which adds spectral gain to compensate for the linear loss, and a driver with de-emphasis. De-emphasis also aids in compensating for loss by compressing lower frequencies so the waveform is pre-equalized when it reaches the receiver. The combination of both of these functions reduces the loss, which in turn lowers deterministic jitter and improves the bit error rate.

However, there are issues with buffer-repeater devices for applications such as PCIe and SAS/SATA. As mentioned previously, these standards use OOB methods for passing initialization and channel training messages. Many active repeaters are tailored for specific rates, though they may not properly pass the lower-frequency OOB signals since they may appear as their name implies "out of band" to the equalizer's filters.

To solve this problem, component vendors are creating a new generation of multi-protocol devices that can operate over several rates as well as protocols. These devices are designed to improve the signal integrity of transmission lines, as well as pass the OOB signaling to allow the channel to properly train.

The Texas Instruments DS125BR800A multi-protocol, low-power, 12.5-Gbit/s repeater includes input equalization and output de-emphasis. In one typical application, a server main board may connect to a mid-plane and then a mezzanine card that may stretch over 30 inches and several connectors *(Fig. 2)*. This device is designed to also pass the OOB signaling for PCIe, SAS/SATA, 10G-KR Ethernet, and more.



Conclusion

With the evolution of serialized bus architectures and the move to higher physical data rates, designers will continuously deal with channel loss as well as additional complexities such as OOB and rate adaption. Careful layout techniques can mitigate some (or all) of the channel loss for some standards.

As rates pass 6 Gbits/s, high-frequency loss in the channel may be too severe to operate reliably without active devices to compensate for the impairment. The latest generation of devices is now making it much easier to improve signal integrity by supporting multiple protocols and rates with a single device, enabling FR-4 to remain the dielectric of choice for mainstream applications.

Richard Zarr *is a technologist at Texas Instruments focused on high-speed signal and data path technology. He has more than 30 years of practical engineering experience and has published numerous papers and articles worldwide. He is a member of the IEEE and holds a BSEE from the University of South Florida as well as several patents in LED lighting and cryptography.*

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