DON TUITE | Analog/Power Editor
don.tuite@penton.com

ADC MAKERS CHALLENGE CONVENTIONAL WISDOM About SAR Speed And Resolution

Texas Instruments, Analog Devices, Maxim Integrated, and Linear Technology have launched 18-bit and even 20-bit resolution SARs at sampling rates of 500 to 5000 ksamples/s.

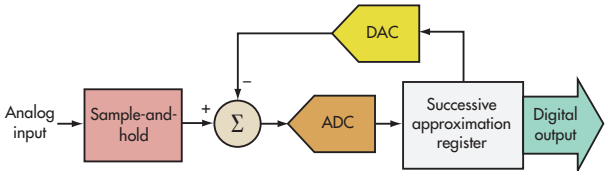
2013 has been a remarkable year for performance improvements in successive-approximation architecture (SAR) analog-to-digital converters (ADCs). While there were a few announcements about new delta-sigma (ΔΣ) and pipeline-architecture ADCs, SARs dominated *(see "Only TI Added New Pipeline And ΔΣ ADCs In 2013," p. 32)*.

The conventional wisdom about ADCs used to say that if circuit designers wanted high resolution, they had to look to the ΔΣ architecture. If designers wanted to look at more rapidly changing data, they had to use a converter built on the SAR architecture. As of 2013, that's only partly true. The newest ΔΣs still offer the very highest precision.

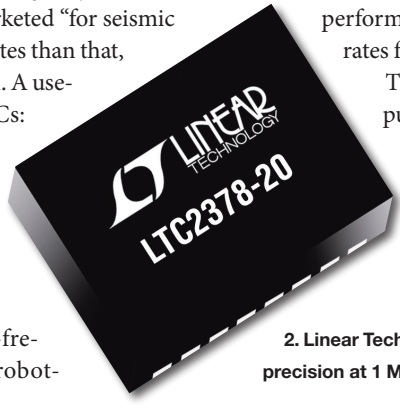
If you're searching for oil reserves out on the patch, for example, Texas Instruments' ADS1282 will give you 31-bit precision at 4 ksamples/s. (It is, in fact, marketed "for seismic and energy exploration.") To run at faster rates than that, even the latest ΔΣs must sacrifice resolution. A useful document, "Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs," from Maxim Integrated noted that some high-bandwidth ΔΣ converters have reached bandwidths of 1 to 2 MHz, but they are limited to 12 to 16 bits of resolution.[1]

If, however, you want to look at higher-frequency data, say for industrial control, robotics, automotive, or instrumentation applications, and you want both precision and high conversion rates, several new SAR ADCs are exhibiting remarkably high precision performance—18 and even 20 bits—and sampling rates from 0.5 to 5 Msamples/s.

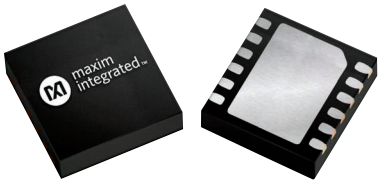
That's with zero latency. The data on the output bus represents the voltage on the sample-and-hold right now. This year, there have been five new SARs in that performance range *(see the table)*. That's not counting the members of each family that bin out just a little slower or less precise.



1. SAR converters compare the analog input voltage against a descending series of voltages (1, 1/2, 1/4, 1/8, 1/16... 1/2N times the reference, up to the resolution of the ADC) and accumulate the results.



2. Linear Technology's LTC2378-20-1 SAR ADC boasts 20-bit precision at 1 Msample/s.



3. The Maxim Integrated MAX11156 SAR ADC offers 18-bit performance with no missing codes at 500 ksamples/s.

SAR REFRESHER

To digitize the voltage on a sample-and-hold circuit, SAR converters compare the sampled input voltage against a series of successively smaller voltages *(Fig. 1)*. Each voltage represents one of the bits in the digital output code. These voltages are fractions of the full-scale input voltage (1/2, 1/4, 1/8, 1/16... 1/2N, where N = number of bits).

The first comparison is made between the analog input voltage and a voltage representing the most significant bit (MSB). If that analog input voltage is greater than the MSB voltage, the value of the MSB is set to 1. If it isn't greater than the MSB voltage, it's set to 0.

The second comparison is made between the analog input voltage and a voltage representing the sum of the MSB and the next MSB. The value of the second MSB is then set accordingly. The third comparison is made between the analog input voltage and the voltage representing the sum of the three MSBs. The process repeats until the value of the least significant bit (LSB) is established.

THE LATEST SAR LINEUP

These SAR ADCs began to appear in late May. At that time, Linear Technology announced the highest-precision device of the lot: its no-latency, 20-bit, 1-Msample/s LTC2378-20-1 *(Fig. 2)*. The SAR ADC has an internal clock, but it requires external references, which can range from 2.5 to 5.1 V. Normally, it operates from a single 5.5-V supply.

For power-critical applications, though, it can be operated down to 2.5 V, where it consumes a maximum of 21 mW. To minimize power consumption, the converter automatically powers down between conversions. The power reduction scales with sampling rate.

Another approach to power reduction is to use the device's differential input with single-ended signals. For circuit designers who choose this digital gain compression (DGC) on the LTC2378 and other Linear Technology SARs, the first amplifier is configured as a unity gain buffer and the single-ended input signal directly drives the high-impedance input of the amplifier.

DGC requires the full-scale input swing to be limited between 10% and 90% of the $\pm V_{Ref}$ analog input range. The internal driver then can be powered off a single positive supply. The LTC2378's data output is serial via a daisy-chainable, SPI-compatible (serial peripheral interface) bus that supports 1.8-, 2.5-, 3.3-, and 5-V logic levels.

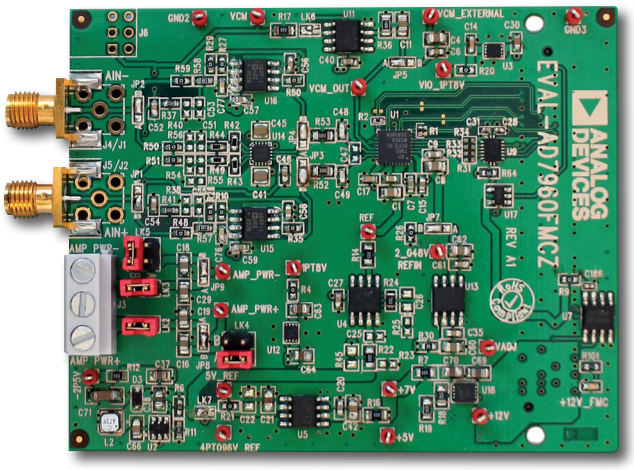
At roughly the same time that Linear brought out the LTC2378, Maxim Integrated announced product availability for the MAX11156 *(Fig. 3)*. This 18-bit, no-missing-codes SAR ADC samples at 500 ksamples/s with its reference and reference buffer built in, but still squeezes into a 3- by 3-mm thin dual-inline flat package (TDFN). "No missing codes" implies that as the input voltage is swept over its range, all output code combinations will appear at the converter output.

The tiny package saves at least 70% board space over competing solutions, according to Maxim. The company also notes its "Beyond-the-Rails" technology, meaning it can handle a ±5-V input signal while operating from a single positive 5-V power rail.

Beyond these specs, Maxim touted the MAX11156's monotonic transfer characteristic, fast settling time, and lack of latency. The ADC's typical dc performance is ±0.5-LSB differential non-linearity (DNL) and ±2.5-LSB integral non-

HIGHEST-PERFORMANCE SAR ADCs INTRODUCED IN 2013

Supplier	Linear Technology		Maxim Integrated	Texas Instruments	Analog Devices
Part number	LTC7378-20	LTC2338-18	MAX1156	ADS8881	AD7960
Resolution (bits)	20	18	18	18	18
Maximum sample rate (kbits/s)	1000	1000	500	1000	5000
I/O type	SPI	SPI	SPI	SPI	Serial LVDS
Differential nonlinearity (± LSB)	–0.5, +0.5	–1, +1	0.5 (typical)	–0.99, +1.5	–0.99, +0.00
Integral nonlinearity (± LSB)	–2, +2	–4, +4	2.5 (typical)	–3, +3	–2, +2
SNR (dB)	101 (minimum)	93.5 (mininum)	91.5 (mininum depends on reference mode)	98.5 (mininum)	95
SINAD (dB)	101 (mininum)	93 (mininum)	93 (mininum depends on reference mode)	98 (mininum)	94.5
Power (mW)	25 mW (maximum)	56 (maximum at 1 Msample/s)	38.5 or 26.5 depending on reference mode	7.2 (maximum at 1 Msample/s)	76.4 (maximum)
Unit price (per/1000)	$29.50	$29.10	$16.90	$19.95	$31.00



4. The Analog Devices AD7960 PulSAR ADC supports the company's high-precision, 18-bit, 5-Msample/s, low-power, data-acquisition signal chain.

linearity INL. Its ac performance is 94.6-dB signal-to-noise ratio (SNR) and –105-dB total-harmonic distortion (THD). For multichannel applications, multiple devices can be paralleled via its SPI-compatible serial interface. Pricing for the MAX11156 starts at $16.90.

Later, in September, Linear Technology also introduced its 18-bit, 1-Msample/s, no latency LTC2338-18 ADC with conversion speeds from 250 ksamples/s to 1 Msample/s. Operating from a single 5-V supply, it has a wider (±10.24 V), fully differential, bipolar input range. Its data sheet SNR is 100 dB, and its THD is –110 dB There also is an internal 2.048-V (20 ppm/°C max) reference and reference buffer. An input divider network scales and level shifts the input signal, eliminating complicated circuitry required to directly interface true bipolar signals. I/O is via a SPI bus.

Linear anticipates a pin-compatible 16-bit and 18-bit family with pseudo-differential true bipolar inputs (LTC2328-18). The proprietary internal reference buffer maintains less than 1-LSB error during sudden bursts of conversions, enabling true one-shot operation after lengthy idle periods. These ADCs operate from a single 5-V supply and consume just 50 mW at 1 Msample/s. Power further reduces linearly at slower sample rates. A shutdown mode dissipates only 300 µW when idle.

Supporting the new part, Linear's DC1908A demonstration board enables easy evaluation of the LTC2338 family in con-

ONLY TI ADDED NEW PIPLEINE AND ΔΣ ADCS IN 2013

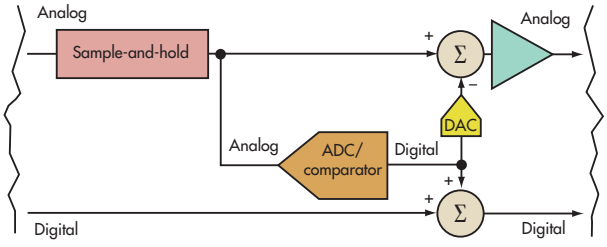
WHILE NEW SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) popped up all year with remarkable new levels of precision and conversion rates, there was less activity in the world of pipeline and delta-sigma (ΔΣ) architectures. In fact, up to the middle of October, only Texas Instruments was announcing new non-SAR devices.

In the first stage of a pipelined ADC, the sample-and-hold (S/H) samples the analog signal, and the flash ADC converts it to an M-bit digital code *(Fig. 1)*. This code represents the most significant bits (MSBs) of the ADC's final output. The same code is fed to the digital-to-analog converter (DAC), which converts code to an analog voltage. This voltage is subtracted from the voltage held by the S/H. The next stage in the pipeline samples and converts the resulting voltage. The number of stages depends on the required resolution and the resolution of the flash ADCs used in each stage.

ΔΣ ADCs feature a ΔΣ modulator and a 1-bit DAC *(Fig. 2)*. The ΔΣ modulator consists of an analog integrator and a comparator, with feedback through the DAC. After the DAC's output is subtracted from the analog input signal voltage, the resulting difference voltage is fed to the integrator and the comparator. The other input to the comparator is a reference voltage. The output of the comparator drives the DAC.

The process is clocked at a very fast oversampled rate, although the actual quantization time is comparatively long because the binary output stream from the comparator is a serial succession of ones and zeros. The ratio of ones to zeros is a function of the input signal's amplitude. In the final step, a binary output representing the value of the analog input is obtained by digitally filtering and decimating this stream of ones and zeroes.

In early January, TI announced a new pipeline-architecture device, the eight-channel, 12-bit, 100-Msample/s ADS5295. Target applications include



1. In the first stage of a pipelined ADC, the S/H samples the analog signal, and the flash ADC converts it to an M-bit digital code. The same code is also fed to the DAC, which converts it to a voltage that is subtracted from the voltage on the S/H. This process is repeated down the pipeline.

junction with the DC590B (QuikEval) or DC718C (PScope) data collection boards. The fully differential LTC2338-18 and pseudo-differential LTC2328-18 families are available in small MSOP-16 packages in commercial, industrial, and automotive temperature grades. Pricing begins at $29.10 in 1000-piece quantities.

Also in September, Analog Devices introduced its 18-bit AD7960 PulSAR ADC with 5-Msample/s throughput *(Fig. 4)*. ADI says the device targets low-power signal chains, multiplexed systems such as digital X-ray, and oversampling applications including spectroscopy, MRI gradient control, and gas chromatography. The AD7960 also achieves its 5-Msample/s performance while consuming only 39 mW. It boasts ±0.8-LSB INL and (99-dB SNR) at full throughput and a noise floor (22.4 nV/√Hz) relative to full scale.

Meanwhile, ADI's AD7961 16-bit PulSAR ADC achieves excellent SNR performance (95.5 dB) and INL (±0.2-LSB INL) at 5 Msamples/s. I/O is not via a SPI bus but by means of a 300-MHz, low-noise low-voltage differential signaling (LVDS) interface.

Finally, Texas Instruments launched its 18-bit SAR ADS888 over the summer. The unipolar, no-latency ADC available operates with a 2.5-V to 5-V external reference, which can be higher than the supply voltage, offering a wide selection of signal ranges without additional input signal scaling. The reference voltage setting is independent of, and can exceed, the analog supply voltage. ed

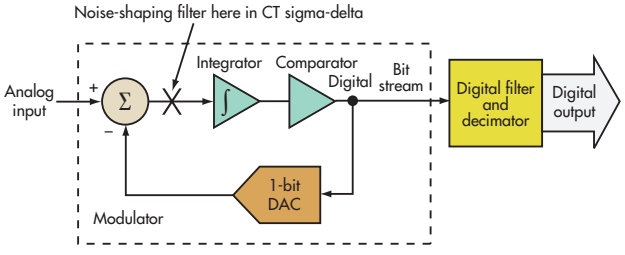
REFERENCE

"Understanding SAR ADCs: Their Architecture and Comparison with Other ADCs," Maxim Integrated, www.maximintegrated.com/app-notes/index.mvp/id/1080

ultrasound, instrumentation, and communications. Its low power consumption and integrated multiple channels in a compact package make it attractive for very high-channel-count data acquisition systems. Output is via one or two wires of low-voltage differential signaling (LVDS) pins per channel.

At high sample rates, the two-wire interface helps keep the serial data rate low, allowing the use of low-cost FPGA-based receivers. Tight channel matching is accomplished by an internal reference. A low-frequency suppression mode, digital filtering options, and programmable mapping functions are also provided internally. There are low-pass, high-pass, and band-pass digital filter options too, as well as filters to remove dc-offset. Unit pricing is $70 in quantities of 1000.

In May, TI announced the ADS4449, a four-channel, 250-Msample/s pipeline device that enables receiver systems to support up to 125 MHz of instantaneous bandwidth in applications that must accommodate extremely small footprints such as multiple-input multiple-output (MIMO) basestations and munitions guidance devices *(Fig. 3)*. TI also expects the ADC to find application in electrically scanned array (AESA) and other phased-array radars. Unit pricing is $199.85.



2. Sigma-delta ADCs employ a sigma-delta modulator and a 1-bit DAC. The DAC's output is subtracted from the analog input signal voltage, and the resulting difference voltage is fed to the integrator and the comparator, which relates the difference to a reference voltage. The binary output stream from the comparator is a serial succession of ones and zeros whose ratio is a function of the input signal's amplitude. In the final step, this stream is digitally filtered and output.

On the ΔΣ side, last March, TI introduced a converter for automotive applications such as battery monitoring systems in hybrid electric/electric vehicles (HEV/EVs) and for fuel or oil-pressure sensing. The 16-bit, 860-sample/s ADS1115-Q1 integrates a voltage reference, a programmable gain amplifier (PGA), a multiplexer, and an oscillator. It also has the industry's only integrated programmable comparator, which makes it easy to implement over-voltage or under-voltage threshold monitoring. Unit pricing is $2.60.

And yes, you read that correctly. Three different ICs were reported with at-introduction "budgetary" pricing for 1000-unit quantities of, respectively, $70, $200, and $2.60 per unit. All devices came from the same supplier. The variation takes some getting used to. Consider budgetary pricing values to be indices of development costs versus potential sales volume. ■

3. The Texas Instruments ADS4449 four-channel, 250-Msample/s pipeline device enables receiver systems to support up to 125 MHz of instantaneous bandwidth in applications that must accommodate very small footprints such as MIMO basestations and munitions guidance devices.