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USE PSPICE TO VERIFY FEEDBACK AMPLIFIER STABILITY

FEEDBACK SYSTEMS HAVE a wide range of applications including different types of amplifiers, signal conditioners, power supplies, and voltage regulators. Obtaining their reliable stability sometimes becomes a serious challenge for engineers, which can be simplified by using a computer simulation. Let's dig into this task by first looking at a model of a negative feedback amplifier and its gain equation *(Fig. 1)*.

A_{OL} and β, as well as their product βA_{OL}, which is called the loop gain, are complex functions of frequency. They both have magnitude and phase properties. For negative feedback, βA_{OL} maintains a phase shift of 180° at dc. Function 1/β, which is also called noise gain, is equivalent to V_O/V_I for non-inverting configurations of amplifiers.

At a certain frequency, $\beta A_{OL} + 1$ may become equivalent to zero ($\beta A_{OL} = -1$) and V_O/V_I $\beta \rightarrow \infty$. As a result, the negative feedback turns to the positive. In turn, the system gets unlimited gain, and due to power-supply limitations, it starts to oscillate or becomes stuck near the power-rail level. Close to this point, the system becomes marginally stable and exhibits significant gain peaking, ringing, and distortion of the output signal.

Feedback Stability Theory states that the system is stable if, as the frequency increases, the magnitude of βA_{OL} reaches 0 dB before the phase shift reaches ±180° (±360° in total). There are two measures of stability: phase margin and gain margin. Phase margin is the difference between 180° and the phase angle of βA_{OL} at the frequency, where its magnitude decreases to 0 dB. Gain margin is the amount of the gain magnitude below 0 dB at the frequency, where the phase delay reaches 180°.

BODE PLOT

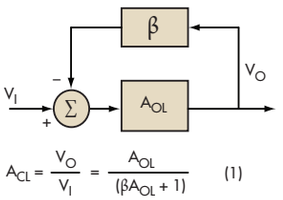
A Bode plot graphically represents the gain and/or the phase of complex values versus frequency. It shows magnitude in decibels and the phase in degrees on the linear y-axis and frequency on the logarithmic x-axis. It's a powerful tool for estimating a feedback system's stability.

Figure 2a presents a Bode plot for A_{OL} and 1/β. Because:

$$\beta A_{OL} = \frac{A_{OL}}{\frac{1}{\beta}} = A_{OL}(dB) - \frac{1}{\beta(dB)}$$

The loop gain (βA_{OL}) can be plotted as the difference in decibels between the A_{OL} and β graphs *(Fig. 2b)*.

In this example of an unstable system, the A_{OL} curve is shown with a pole at the frequency (fp) and the 1/β curve is shown with a zero at the frequency (fz). The zero creates an additional pole on the loop-gain curve and the phase shift reaches 180° before βA_{OL} reaches 0 dB.

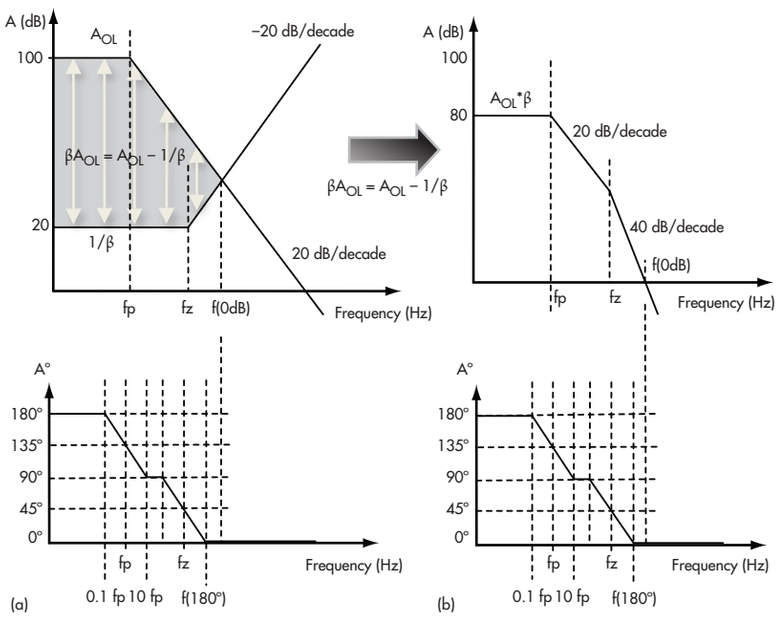


If $\beta A_{OL} \gg 1$, then $\frac{V_O}{V_I} = 1/\beta$

If $\beta = 0$, then $\frac{V_O}{V_I} = A_{OL}$

A_{CL} = closed-loop gain
A_{OL} = open-loop gain
β = feedback factor, a portion of the output signal returning to the amplifier's input

1. Shown is a model of a negative feedback amplifier, along with equations in terms of its gain. A portion of the output signal of the amplifier with a gain A_{OL} returns back to its input in inverted polarity by a feedback network with the gain β. When β = 0, the amplifier has no feedback. When βA_{OL} is much greater than 1, the feedback determines the amplifier's gain. The negative feedback improves the amplifier's performance, but may cause its instability and oscillation.



2. In these Bode plots for open-loop gain (A_{OL}) and 1/β (a), loop gain (βA_{OL}) can be plotted as the difference in dB between the A_{OL} and β graphs (b).

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There are two ways to look at system stability when using Bode criteria:

- Use a 1/β plot over A_{OL} plot: The feedback system is unconditionally stable if 1/β intersects A_{OL} at a slope no greater than 20 dB/decade. The system will have a marginal stability and may oscillate if this slope is 40 dB/decade or greater.
- Use the loop gain: The feedback system is unconditionally stable if the loop gain intersects the 0-dB point at a slope no greater than 20 dB/decade. The system will have a marginal stability and likely will start to oscillate if this slope is 40 dB/decade or greater. This is often more convenient than plotting 1/β over A_{OL}, because the βA_{OL} plot can be easily obtained directly from PSpice simulation.

Each pole adds an additional 90° in the phase shift *(phase plots in Figs. 2a and 2b)*. A single-pole system is unconditionally stable because it may have a total phase shift of 270° maximum. That gives 90° of phase margin, and the feedback never becomes positive. Unfortunately we mostly have to deal with potentially unstable multipole systems and use frequency-response correction to ensure system stability.

A check for the closing rate on the Bode plot is a simple first-order stability test, but it's also important to verify the phase margin for the loop gain on the phase plot. To ensure reliable stability and to prevent significant gain peaking, the phase margin should exceed 45°. A good compromise between minimum gain peaking and fast setting time is a phase margin of 60°.

Three methods can be used to obtain open-loop Bode plots via PSpice or other Spice-based simulators: using precise bias points; injecting ac signal in the loop using a large inductor and capacitor; and directly injecting the ac signal in the feedback loop.

USING PRECISE BIAS POINTS

Theoretically, obtaining the loop gain of a feedback amplifier involves:

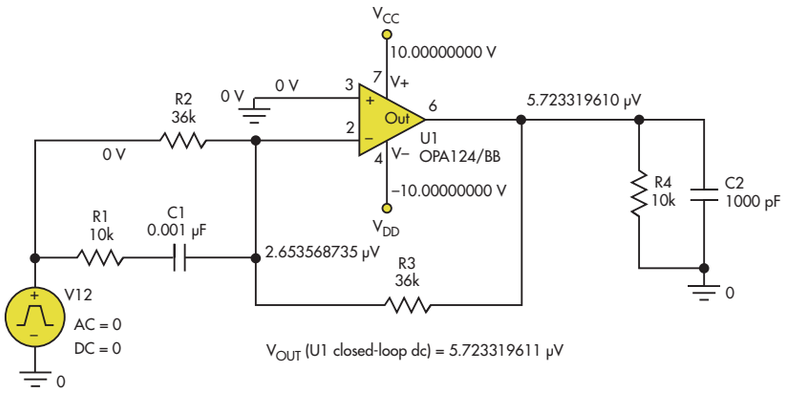
- Breaking the feedback loop at the point with the lowest impedance
- Inserting an ac sweeping voltage source in series with a dc bias voltage source between the "input" of the open loop and ground
- Choosing the level of the dc bias to keep the system in the linear region
- Measuring the loop output voltage versus frequency and plot results in Bode format

Unfortunately, it's impossible in real life because the input signal is multiplied by the amplifier's high open-loop gain. Even with a very precise dc bias source, any fluctuations will bring the output signal to saturation.

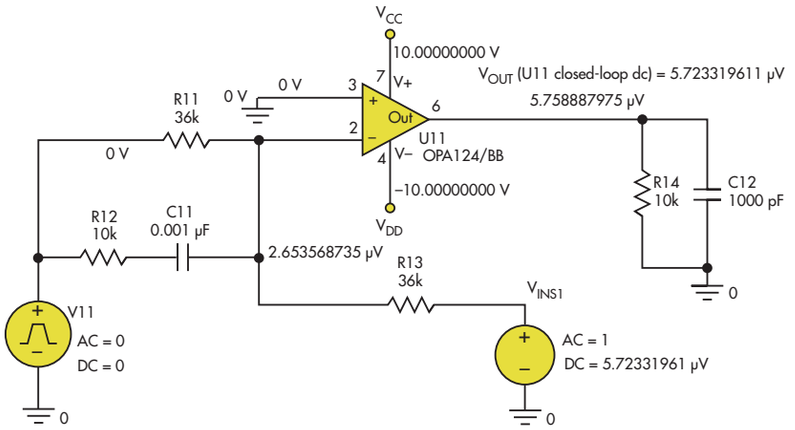
Nevertheless, this method usually can be realized with PSpice. First, the bias point analysis should be run with the closed loop. Then the display bias voltages on the schematic page are displayed with the maximum number of digits.

By default, PSpice displays four digits in the results. Set display options for 10 significant digits. In OrCad Capture, for example, open the "PSpice" down menu, next open "Bias Points" and "Preferences…," and then set the "Display Precision" box for 10 significant digits. For instance, an equalization amplifier is shown with bias points enabled and set to 10 digits after the bias point simulation *(Fig. 3)*. The amplifier's gain is boosted at high frequencies by capacitor C1 in its feedback network, prompting concern about the amplifier's stability.

In Figure 3, the loop's lowest impedance is the output of V1. The connection of V1 output to R3 becomes a good point to break the loop. Its precise bias value should be copied to the clipboard. It can be used as a dc attribute of an added voltage source in the next simulation. Then take the following steps:



3. This equalization amplifier has its bias points display set to 10 after simulation.



4. A voltage source is placed between ground and the input of the open loop.

- Break the loop at the chosen point and place the voltage source V_{INS1} between ground and the "input" of the open loop *(Fig. 4)*.
- Set the dc attribute of V_{INS1} to the value copied from the clipboard and the ac attribute of V_{INS1} to 1 V.
- If there are other ac sources in the schematic, set their ac attributes to 0.

Now the bias-point analysis can be run again. (Also check the value at U1's output.) It's acceptable if U1's output voltage is within several hundred millivolts from the original value. Otherwise, in rare cases, several digits of the V_{INS1} dc attribute may need adjust-

ment, followed by running the analysis again, until there's an approximate initial value at U1's output.

Finally, ac analysis can be run, and the Bode plot graphs can be obtained in the "probe window" *(Fig. 5)* as βA_{OL} as a difference in dB between the output of U11 and positive terminal of V_{INS1}:

DB(V(U11:OUT))-
DB(V(V_{INS1}:+))

A_{OL} as a difference in dB between the output U11 and its negative input:

DB(V(U11:OUT))-
DB(V(U11:-))

1/β as a difference in dB between the positive terminals of V_{INS1} and the negative input of U11:

DB(V(V_{INS1}:+))-
DB(V(U11:-))

To obtain the phase portion of the loop plot in the same probe window, add a new y-axis to the Plot menu and place a trace:

P(V(U11:OUT))-
P(V(V_{INS1}:+))

Appropriate Bode plots also can be obtained for other components of Equation 1 *(Fig. 1, again)*:

A_{OL} magnitude graph:

DB(V(U11:OUT))-
DB(V(U11:-))

A_{OL} phase graph:

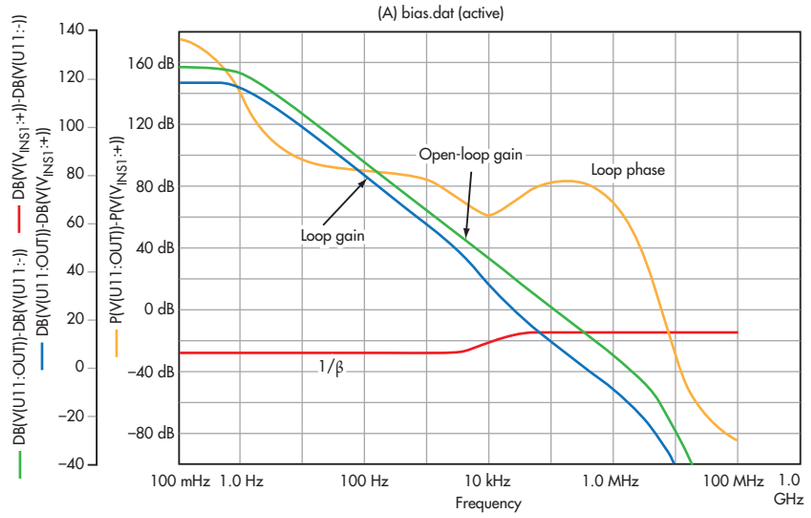
P(V(U11:OUT))-
P(V(U11:-))

1/β magnitude graph:

DB(V(V_{INS1}:+))-
DB(V(U11:-))

1/β phase graph:

DB(V(V_{INS1}:+))-
DB(V(U11:-))



5. Bode plots can be achieved via the probe window, such as in this example for an equalization amplifier.

From the probe windows, it's determined via the cursor function that the amplifier's phase margin is 55.62°, which means it's reliably stable.

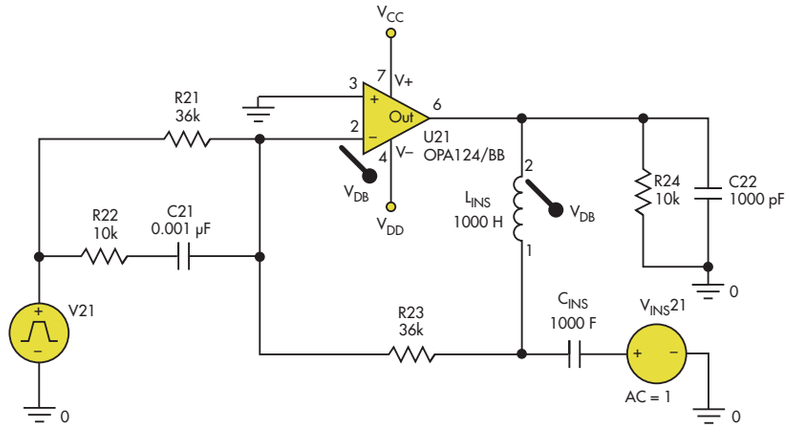
INJECT AN AC SIGNAL IN THE LOOP USING LARGE L AND C

Another PSpice method involves inserting a large inductor (L_{INS}) in the amplifier's feedback loop *(Fig. 6)*. It opens the loop for the ac signal, but keeps it closed for dc. A voltage source (V_{INS21}) injects an ac signal in the loop using a large capacitor (C_{INS}). Note that very large values for L_{INS} and C_{INS} are perfectly acceptable to PSpice simulations in this case.

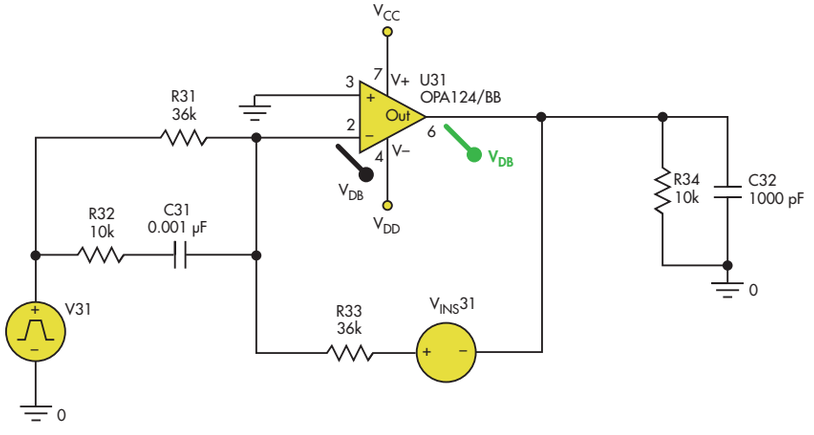
After ac simulation, the magnitude portion of the loop-gain plot can be obtained by plotting the difference in dB between the upper and lower terminals of the inductor. The phase portion of the plot will be the phase difference between the same terminals. In addition, as in the previous example, all other graphs of Equation 1 are obtainable. Results will be exactly the same as those from the first method *(Fig. 5, again)*.

INJECT AN AC SIGNAL DIRECTLY INTO THE FEEDBACK LOOP

To create the simulation circuit for this method, a floating ac source (V_{INS31}) is inserted directly in the feedback loop *(Fig. 7)*. This keeps the loop closed for the dc signal. The ac attribute for the source may have any value, since it doesn't affect the simulation. However, 1 V is considered a convenient value in this scenario.



6. This PSpice method inserts a large inductor (L_{INS}) and large capacitor (C_{INS}) in the amplifier's feedback loop.



7. Here, a floating ac signal is directly injected into the amplifier's feedback loop.

To minimize the possibility of an error, the breaking point in the loop with the lowest impedance was chosen. V_{INS31} injects an ac signal in the loop, creating an ac voltage (V_inj-) on its negative terminal with the respect to ground. This voltage is multiplied by βA_{OL} in the loop and can be measured with respect to ground as V_inj+ on the positive terminal of V_{INS31}.

After ac simulation, it's possible to obtain the loop gain βA_{OL} by plotting the ac voltage difference in dB between positive and negative terminals:

DB(V(V_{INS31}:+))-DB(V(V_{INS31}:-))

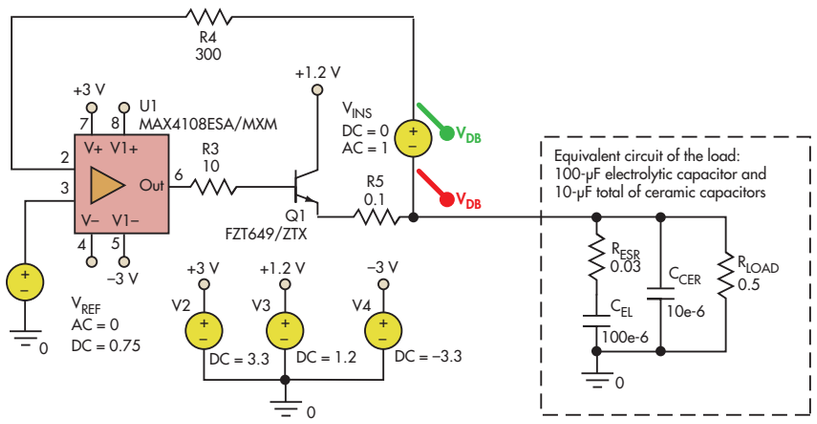
This simulation also gives us exactly the same results as in previous examples *(Fig. 5, again).*

Overall, it's the simplest and often the most convenient method, particularly if additional ac analysis is planned for later in the design process. V_{INS31} can be kept in the PSpice schematic without having to change the schematic for a different type of analysis—simply set ac and dc attributes to zero. In this case, V_{INS31}doesn't affect the circuit or the simulations because it represents a shorted point.

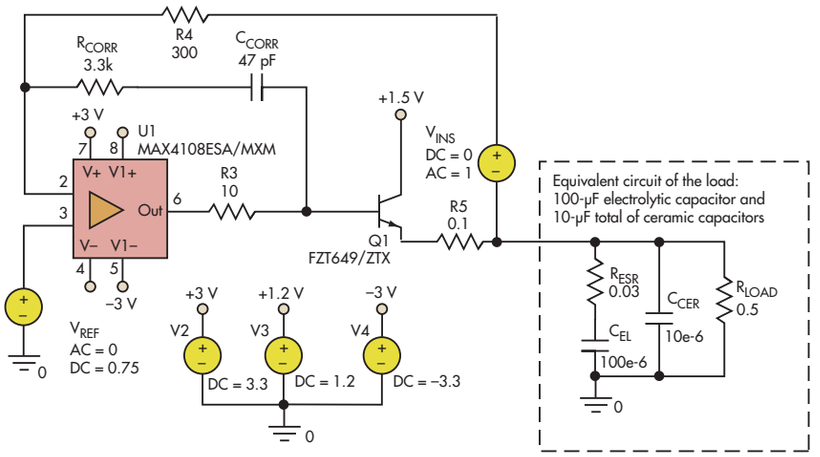
For example, direct injection is used to estimate the stability of a 0.75-V, 1.5-A linear regulator *(Fig. 8).* Based on the simulation results we will correct the loop frequency response if necessary.

The regulator contains an op amp (U1) and an output emitter follower (Q1). Together they're configured as a non-inverting amplifier with the gain of one. The 0.75-V reference voltage source is connected to the amplifier's positive input.

The regulator powers a circuit board with a number of ICs and



8. Direct injection is used to estimate stability of a 0.75-V, 1.5-A linear regulator.



10. This schematic shows a corrected version of the linear regulator in Figure 8, thanks to the use of compensation.

bypass capacitors, a 100-µF electrolytic capacitor, and several ceramic capacitors that equal 10 µF in total capacitance. The output network of the regulator is formed by the electrolytic capacitor (Cel) in series with its ESR resistor (Resr), the total value of ceramic capacitors (C_cer), and the load resistor (R_Load). This network adds two poles and one zero to its open-loop Bode plot and creates an uncertainty on the loop stability.

To obtain the Bode plot, an ac source (V_ins) was inserted in the low impedance point of the loop, between R4 and R5. After simulation, the probe window shows the magnitude of the βA_{OL}:

DB(V(V_{INS}:-))-
DB(V(V_{INS}:+))

with y-axis 1, and its phase curve:

P(V(V_{INS}:-))-P(V(V_{INS}:+))

with y-axis 2 *(Fig. 9)*. Note that $\beta = 1$ and $\beta A_{OL} = A_{OL}$.

Measurements indicate that the βA_{OL} intersects the x-axis with the slope of 40 db/decade or more, the negative phase margin of –35°, and the negative gain margin of –15. This indicates an unstable linear regulator that requires a frequency correction.

There are many compensation methods. Figure 10 presents one possible solution. The compensation network consists of a 3.3k resistor R_corr in series with a 47-pF capacitor and C_corr between the negative input of U1 and the base of Q1. Together with R4 this network creates an additional zero in A_{OL} and ensures the reliable stability.

Simulation results of the compensated network show that βA_{OL} provides a stable 20-dB/decade rate of closure, 11 dB of gain margin, and 67° phase margin *(Fig. 11)*. This indicates that the linear regulator is reliably stable with the chosen correction.

ACKNOWLEDGEMENT

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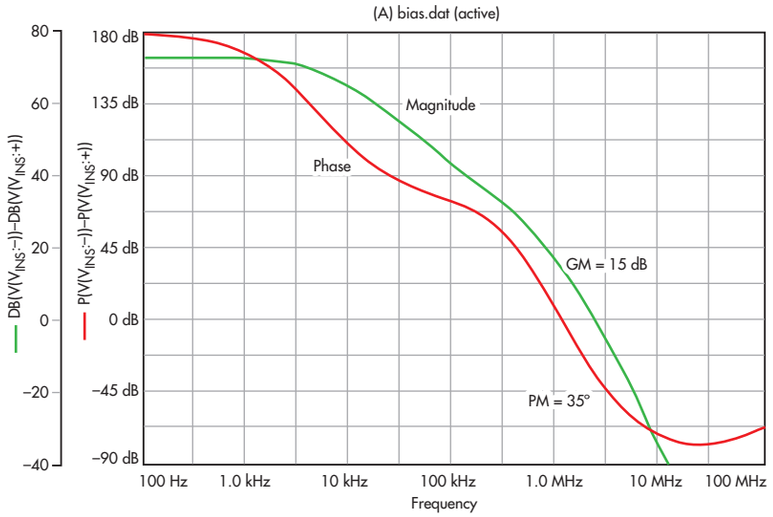
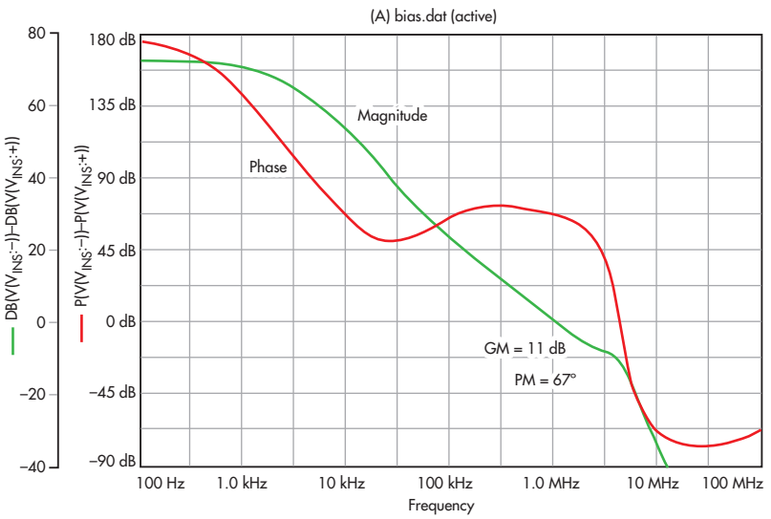


9. The Bode plot created for the linear regulator in Figure 8 indicates that it's unstable.



11. The βA_{OL} Bode plot of the corrected regulator in Figure 10 reveals that the device is reliably stable.

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REDUCE AMPLIFIER NOISE PEAKING TO IMPROVE SNR

MANY AMPLIFIERS EXHIBIT an increase in voltage noise spectral density (NSD) as they approach the unity-gain crossover frequency. This noise peaking can cause your circuits to have 39% higher noise than you expected. This is especially troublesome in unity-gain circuits, also called buffer or voltage-follower applications.

Such peaking occurs when the spot noise becomes greater than the noise floor of the amplifier, and this behavior can extend for several octaves beyond crossover. These effects are present at frequencies well beyond what is shown in most manufactures' datasheets, and most textbooks don't discuss the issue at all. The topic remains "out of sight" until you are working with a low-noise, low-gain circuit that seems to have excessive amounts of noise.

The amplifier is set up as a unity gain buffer *(Fig. 1)*. It has a –3-dB bandwidth of 16 MHz, and the noise floor is 16 nV/√Hz at 100 kHz. Notice how the noise density starts to increase around 2 MHz. To make matters worse, the –3-dB noise bandwidth is about 30 MHz.

An academic analysis states that the total noise is equal to the noise floor multiplied by the square root of the noise bandwidth, which is π/2 times larger than the –3-dB bandwidth, for a single-pole rolloff. This calculation shows that the total noise is 80 μV_{RMS}. If you integrate the NSD over the entire bandwidth, the total noise is 111 μV_{RMS}, which is 39% higher.

Unfortunately, this amount of error is about as good as it gets. Many amplifiers are much worse. Peaks that are 10 times greater than the noise floor are possible. Most amplifiers will have a peak that is 50% to 200% greater than the noise floor.

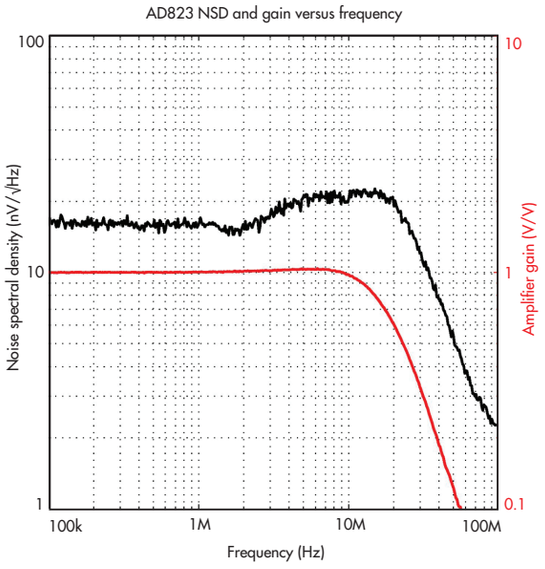
There are two causes of noise peaking:

- Intrinsic noise peaking: This type of noise peaking is set by the design of a particular op amp. Once a specific model of op amp is chosen for a circuit, the intrinsic noise peaking is set.
- Stability noise peaking: This type is affected by the way the amplifier is used in the circuit.

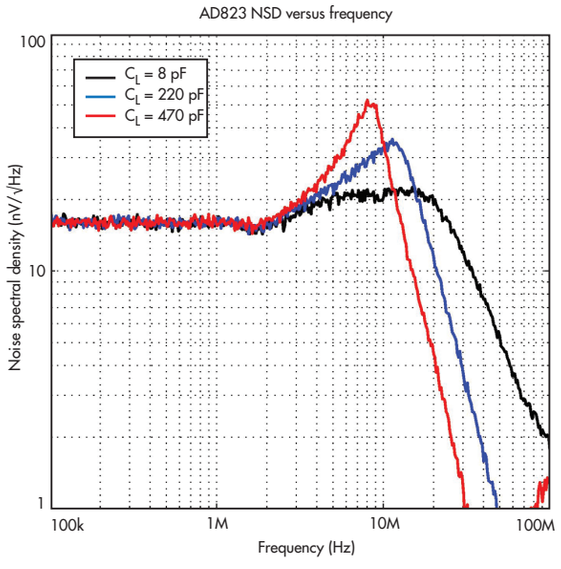
Most amplifiers are designed so the input stage dominates their noise performance. All of the transistors in an amplifier contribute noise, but their noise is reduced by application of negative feedback. Any gain that precedes a noise generator will reduce the noise that is contributed to the amplifier by that generator.

At most frequencies, there is plenty of gain ahead of all of the transistors except the input stage. Great care and significant amounts of current are spent to make the input stage achieve the noise performance required for the amplifier. This works well enough at lower frequencies.

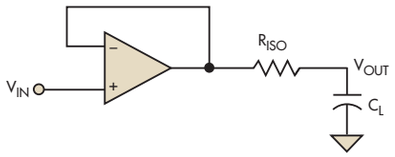
At higher frequencies around the amplifier's unity-gain crossover frequency, there is no gain to suppress any noise generated by the transistors inside the amplifier. Any noise that makes its way to the output with a magnitude greater than the noise floor of the amplifier will dominate the total noise. The specific transistors that dominate



1. The frequency response of the AD823 op amp in a unity-gain configuration rolls off predictably (red), while the voltage noise spectral density plot shows noise peaking (black).



2. Adding load capacitance at the output intending to filter the noise reduces phase margin and increases noise peaking.



3. Instead of adding a load capacitance for filtering, use a series resistor-capacitor network to properly filter noise

are unique to every amplifier design.

The stability noise-peaking effect is present in all feedback structures, including the output buffers of voltage references and voltage regulators. A mediocre amplifier may have a noise floor that's so high that it masks any intrinsic noise peaking. A high-performance, low-noise amplifier has flat-band noise that's low enough that you can observe the effects of noise peaking.

The feedback-loop stability controls the stability noise peaking. As previously noted, the negative feedback of an amplifier suppresses the noise generated from most of the transistors. As the phase margin degrades, this feedback is no longer negative. The signals near the unity crossover frequency are fed back more in phase with the incoming signal. This causes the closed-loop response to peak near the crossover frequency. The same mechanism responsible for frequency peaking of the signal also causes frequency peaking of the noise.

Avoid destabilizing the feedback loop, because doing so has a detrimental effect on the noise performance. Well-intentioned engineers will place a capacitor at the output of an op amp to "filter" noise. This makes the noise much worse, because the capacitive load adds more phase shift to the feedback loop *(Fig. 2)*.

As you load the output of the amplifier with more capacitance, the noise peak grows. The log scales on this plot mask the true severity of the situation. The total noise at the output is the value of the noise spectral density integrated over the entire bandwidth. There is much more bandwidth from 2 MHz to 16 MHz than there is from dc to 2 MHz.

This means the noise is completely dominated by the noise peak and has nothing to do with the thermal noise floor. To compare these results, assume that the rest of the system has limited the –3-dB bandwidth to 16 MHz (25-MHz noise bandwidth). The total integrated noise for C_L of 8 pF, 220 pF ,and 470 pF is 95 μV_{RMS}, 110 μV_{RMS}, and 115 μV_{RMS}, respectively.

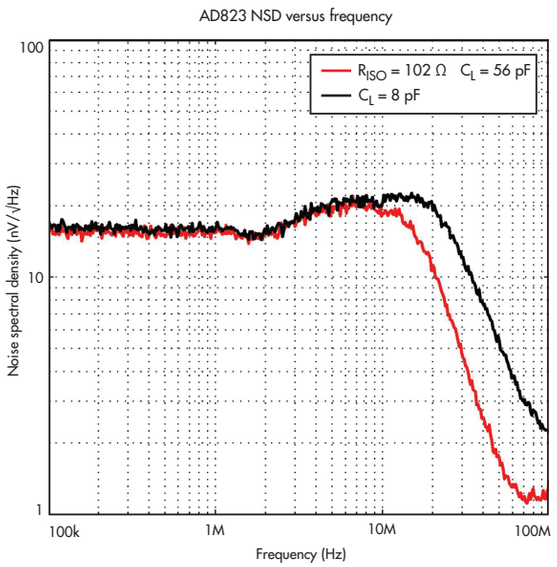
The proper way to filter the output of a buffer is to place an RC filter at the output *(Fig. 3)*. The resistor makes the amplifier load appear resistive at high frequencies, which avoids adding phase shift to the feedback loop. This technique will reduce the accuracy of the buffer if it is resistively loaded.

This example assumes the entire 16-MHz bandwidth of the buffer is required in the application. The pole frequency of the filter is set approximately 28 MHz. The filter causes a substantial reduction of the out-of-band noise *(Fig. 4)*. The total integrated noise without the filter is 111 μV_{RMS}, while the total noise with the filter is 84 μV_{RMS}. This represents a 25% reduction in noise without affecting the signal bandwidth.

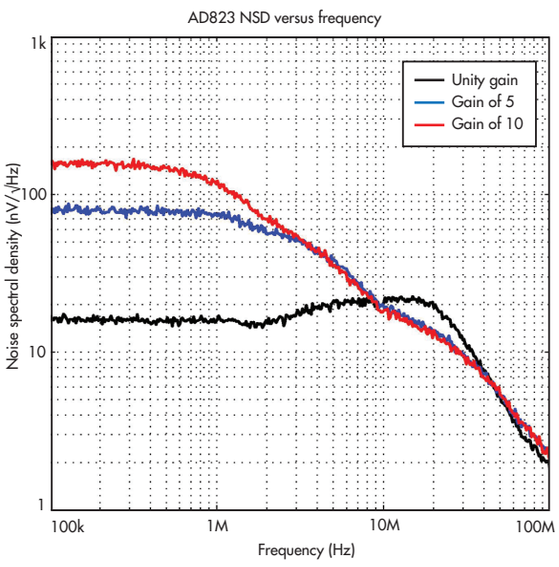
Better performance can be obtained when the RC filter limits the signal bandwidth of the amplifier. In this case, the filter sets the –3-dB bandwidth of the signal as well as the noise bandwidth of the amplifier.

The lowest-noise results occur when this filter frequency is set before the noise floor starts to peak. This would be approximately 2 MHz in the case of the AD823. Under these conditions, it is possible to approach the theoretical limit of the noise floor, multiplied by 1.57 × f_{-3dB}. The designer must determine if it is appropriate to throw away a significant amount of amplifier bandwidth to improve the noise of the circuit.

At this point, circuit designers may wonder why amplifier data sheets tout their 1/f noise and the



4. Using the RC filter, the noise spectral density improves over frequency as out-of-band noise is reduced.



5. A graph of the AD823 op amp's output NSD versus frequency clearly shows that the significance of the noise peaking is reduced as the gain increases.

thermal-noise performance specifications, when they have nothing to do with total noise in an amplifier. The answer is that they do matter, but only in higher-gain configurations. Great things happen when an op amp is placed in a gain configuration. The loop stability improves, so the noise peaking induced by phase shift is reduced to an insignificant level.

The intrinsic noise peak remains, but it becomes less significant compared to the thermal noise floor *(Fig. 5)*. This is because the intrinsic sources feed directly into the output of the amplifier without any gain. As a result, they remain relatively constant, no matter how the amplifier is set up. The thermal noise floor becomes much more significant because it is "gained up" by the amplifier. The intrinsic noise peaking is visible as bumps in the rolloff region of the higher gain curves.

There are many practical implications of noise peaking to consider. First, the noise peak will dominate the total noise in low-gain configurations. Designers should plan for this occurrence and test several amplifiers, if it is critical for the application. Two different amplifiers with the same noise floor can have vastly different amounts of total integrated noise.

Second, filter the outputs correctly with passive RC filters. These filters can have a significant impact on the total system noise. Never add capacitance directly to the amplifier's outputs (or inputs). This only serves to degrade the feedback-loop stability.

Finally, design the signal path to take as much gain as possible early in a system's signal chain. This is the best solution if it is possible, since the total noise performance of the system is dominated by the high-gain front-end amplifier.

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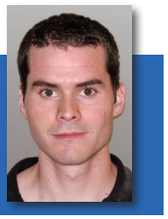

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ADVANCED DIGITAL ISOLATION TECHNOLOGIES BOOST SOLAR POWER INVERTER RELIABILITY

TODAY'S PHOTOVOLTAIC (PV) power systems offer a sustainable alternative to fossil-fueled power plants, providing lower long-term operating costs, modular scalability, higher efficiency, and a smaller carbon footprint. These power systems use PV panels to convert sunlight into dc voltage and solar power inverters to transform the dc voltage into ac voltage suitable for a commercial grid.

In addition to performing this essential dc-ac conversion, the solar inverter provides grid-disconnect capabilities to prevent the PV system from powering a disconnected utility. An inverter remaining online during grid disconnect or delivering power through an unreliable connection can cause the PV system to back-feed local utility transformers, creating thousands of volts at the utility pole and endangering both the system and utility workers. Upon reconnect, the inverter cannot deliver power until it detects rated utility voltage and frequency over a five-minute period.

The inverter compensates for environmental conditions that affect power output. PV-panel output voltage and current are susceptible to variations in temperature and light intensity per cell unit area (called "irradiance"). The cell output voltage is inversely proportional to cell temperature, and cell current is directly proportional to irradiance. Wide variations in these parameters cause the optimum inverter voltage/current operating point to move significantly.

The inverter addresses this issue by using closed-loop control to maintain operation at the maximum power point when the product of voltage and current is at its highest value. The inverter also provides manual and automatic input/output disconnect for service operations, EMI/RFI conducted and radiated suppression, and ground fault interruption. Encased in a ruggedized package, the inverter is designed to remain in full-power operation for more than 25 years.

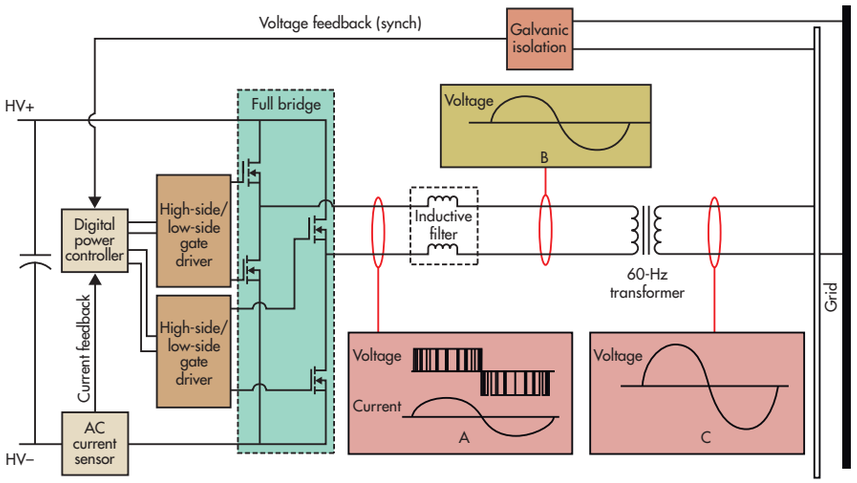
The single-phase PV inverter uses a digital power controller and isolated high-side/low-side gate drivers to pulse-width modulate a high-wattage, full-bridge power stage *(Fig. 1)*. Using feedback from the local ac mains and the power stage, the controller modulates the MOSFETs to synthesize a discrete-time, grid-synchronized 60-Hz high-voltage

ac switching pattern. This discrete switching pattern is then filtered to remove high-frequency noise components and delivered to the grid through an isolation transformer.

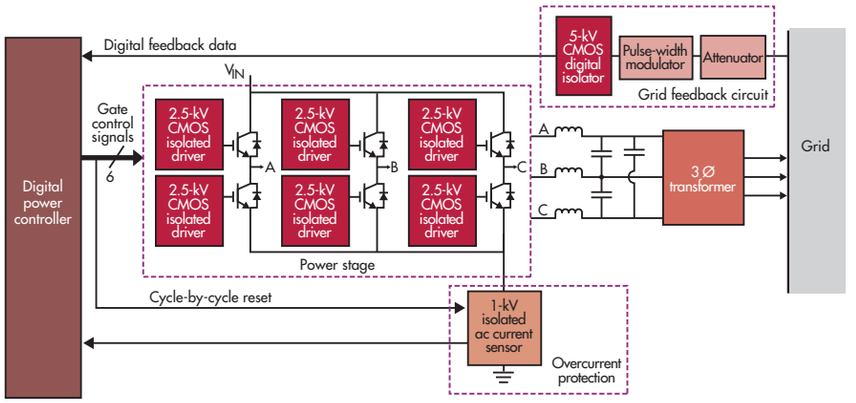
A PV inverter's hardware design is full of tradeoffs that can be problematic if the designer makes the wrong choice. For example, PV systems are expected to operate reliably and at full rated output for at least 25 years, and yet they must be competitively priced, forcing the designer to make tough cost/reliability tradeoffs.

The high efficiency requirements of inverters often require the use of more expensive gate drivers, power switches, and magnetic components. Twenty-five-year system life in an outdoor environment increases the cost of inverter system packaging due to the higher costs of advanced insulation and potting compounds. These considerations and the cost-competitive nature of the inverter market combine to create difficult decisions for the designer.

The PV inverter's exposure to extreme heat and cold for 25 years should cause the designer to take a major pause when considering inverter components. For example, electrolytic capacitors that filter out ripple, as well as optocouplers that provide galvanic isolation, have no chance of "going the distance" in lifetime longevity. Electrolytic capacitors dry out and fail, and the optocoupler's LED brightness gradually fades in the face of excessive heat and input current. Workarounds for these delicate components include replacing electrolytic capacitors with costly film capacitors and substituting modern CMOS isolators for the optocouplers.



1. The single-stage, single-phase inverter incorporates a PWM full-bridge converter.



2. The transformer-based three-phase inverter uses CMOS isolation components as part of the gate-driver circuitry.

CMOS technology offers high reliability, cost effectiveness, high-speed operation, small feature size, low operating power, and operating stability over voltage and temperature extremes. Unlike the gallium-arsenide (GaAs) technology used in optocouplers, CMOS devices have no intrinsic wear-out mechanisms. The CMOS isolation cell is capacitive, fully differential, and optimized for tight timing performance, low-power operation, and high immunity to data errors caused by external fields and fast common-mode transients.

The advantages of CMOS, combined with proprietary silicon product design, enable robust isolation devices that offer higher functional integration, superior reliability (greater than 60-year isolation barrier lifetime), –40°C to 125°C continuous operation at maximum V_{DD}, and substantial gains in performance, power efficiency, board-space savings, and overall ease-of-use.

PV-inverter architectures do not end with the single-phase, transformer-based inverter shown in Figure 1. Other common types include high-frequency, bipolar, three-phase, transformerless, and battery-powered inverters. While these topologies vary, they share the need for the same component solutions. The block diagram in Figure 2 shows several CMOS isolation devices used in a transformer-based, three-phase inverter.

In this classic closed-loop architecture, the digital controller modulates the power-switch duty cycle to force the PV system's output-voltage amplitude and phase to match that of the grid. Individual 2.5-kV isolated gate drivers are typically preferred in inverter designs because they simplify printed-circuit board (PCB) layout.

Current feedback to the controller is provided by a single, CMOS, isolated-ac current sensor that offers a wider temperature range, higher accuracy, and higher reliability than current-sense transformers. The sensor is reset on a cycle-by-cycle basis using the inverter gate-control signals generated by a digital controller, eliminating the need for external reset circuitry.

Like other emerging technologies, PV systems will continue to evolve to meet market demands for higher capacity, lower cost, and higher reliability. As this happens, PV inverters will expand in functionality, and designers will demand more integrated, application-specific component-level devices that will further leverage and drive innovation in CMOS isolation. As these events unfold, PV power systems will become more widespread and ultimately a viable member of the utility mainstream that will significantly reduce our dependence on fossil fuels.

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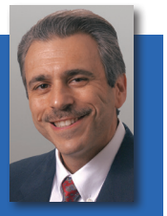

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SECOND-ORDER STATE VARIABLE FILTER CONSUMES LESS THAN 3 µA

FILTERS ARE USED in many applications to remove unwanted frequency components from incoming signals, enhance incoming signals, or both. In portable and non-portable medical applications, for example, the heart-rate functionality must detect a range of frequencies. Similarly, handheld communication products like walkie-talkies must be able to monitor multiple tones.

In these and other applications, the combination of a low pass, high pass, and band pass filter is very useful where the quality factor (Q), the gain, and the cutoff frequency of the circuit can be set separately. A state variable filter can be used. With a single low-power quad op-amp IC, an integrated, low-power state variable filter that consumes less than 3 µA can be implemented to achieve multiple design objectives using only three of the four available op amps.

Figures 1 and 2 show the complete circuit design and frequency response of a state variable filter with an op amp. In this case, a Touchstone Semiconductor TS1004 low-power quad op amp was selected.

The state variable filter offers an independent selection of the Q factor, pass band gain, and cutoff frequency of the circuit. In addition, high pass, low pass, and band pass outputs are available concurrently. The gain of each filter can be set independently where the gain of the band pass filter is the state variable filter's overall Q factor. To design the circuit, we used Equation 1 where R = R1 = R2 = R3 = R4 = R5 = R7 = 530 kΩ, as well as Equations 2, 3, and 4.

$$\text{Filter Q} = \text{band pass section gain} = \left(\frac{R + R6}{3R}\right) \quad (1)$$

Low pass and high pass corner frequency,

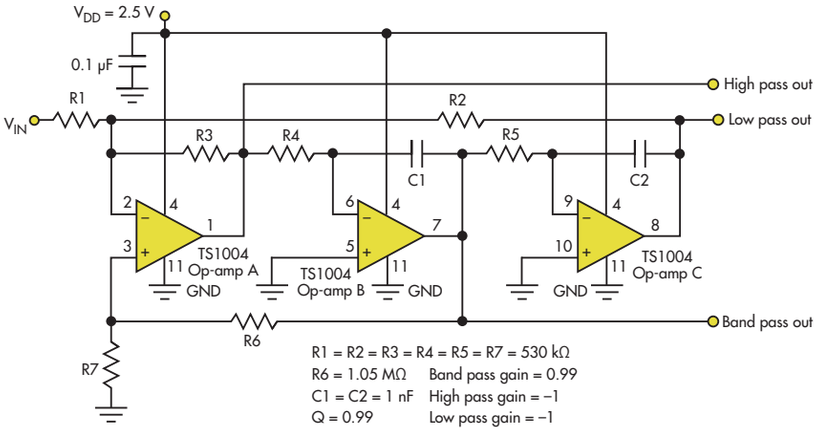
$$f_O = \frac{\sqrt{\frac{1}{R4 \times C1 \times R5 \times C2}}}{2\pi} = \frac{\sqrt{\frac{1}{530\ \text{k}\Omega \times 1\ \text{nF} \times 530\ \text{k}\Omega \times 1\ \text{nF}}}}{2\pi} = 300\ \text{Hz} \quad (2)$$

$$\text{Low pass section gain} = -\frac{R2}{R1} = -\frac{530\ \text{k}\Omega}{530\ \text{k}\Omega} = -1 \quad (3)$$

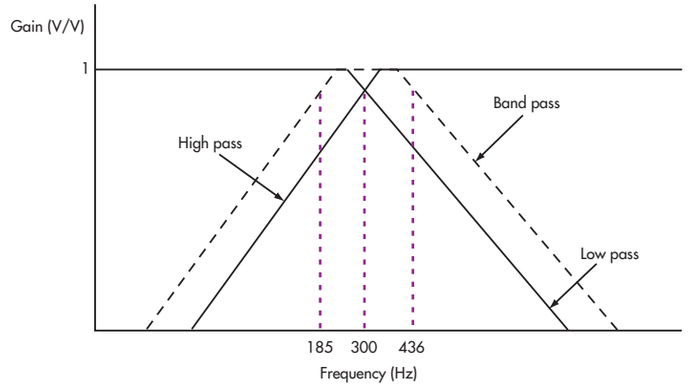
$$\text{High pass section gain} = -\frac{R3}{R1} = -\frac{530\ \text{k}\Omega}{530\ \text{k}\Omega} = -1 \quad (4)$$

By substituting the component values shown in Figure 1 into Equations 1 through 4, the low pass and high pass filter sections have a gain of approximately –1 and the band pass filter section has a gain of approximately 0.99. Thus, the overall Q factor is also 0.99. The cutoff frequency for the low pass and the high pass filter section is approximately 300 Hz. The pass band of the band pass filter section is approximately 251 Hz from approximately 185 Hz to 436 Hz.

With three of the four op amps in use, the entire circuit consumes only 3 µA of supply current! To minimize variations in section gain, Q, and cutoff frequency, 1% tolerance resistors are recommend-



1. This state variable filter with a TS1004 quad op-amp IC circuit maximizes printed-circuit board (PCB) space while saving power.



2. This state variable filter frequency response shows a low pass, high pass, and band pass filter.

ed. Since the op amp has a gain bandwidth product of 4 kHz, increasing filter section gain will reduce the bandwidth of the individual filter sections accordingly.

Being able to integrate a low pass, high pass, and band pass section in a single circuit with the ability to design each section separately is useful in many applications such as heart monitors, audio equalizers, alarm systems, and portable communication devices. A state variable filter offers integration and flexibility by providing low pass, high pass, and band pass sections simultaneously with the ability to design the Q, the gain, and the cutoff frequency separately. Using a low-power quad op amp to design a state variable filter provides an integrated and simple low-power solution with a total circuit supply current of only 3 µA.

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SIMPLE CIRCUIT INTERFACES 1-WIRE TEMPERATURE SENSOR TO A MICROCONTROLLER

TEMPERATURE-INDICATOR AND TEMPERATURE-BASED products have generated wide interest. There are numerous applications for such devices with many possible solutions, each with its own advantages and disadvantages.

This idea discusses a sensor interface that offers high accuracy while using less board real estate. The article also discusses some software issues and provides code samples that users can integrate into their system and adapt to their environments. Designers can add to the features offered by the circuit as well.

The simple circuit interfaces a 1-Wire temperature sensor (DS18S20) to a Cypress microcontroller (CYBC26443). But the technique can be extended to any other 1-Wire device with little modification of the hardware and code. The MCU can be any processor, but I chose a programmable system-on-a-chip (PSoC) because it offers flexibility in terms of choosing and implementing hardware blocks on the silicon. The PSoC also provides an application program interface (API) so novices can easily work on and troubleshoot their ideas.

The 1-Wire products provide functions such as memory and mixed-signal capabilities via a single wire over a serial interface, with both power and communication delivered using the serial protocol. These devices are easy to interface and use where minimum interconnect complexity is required.

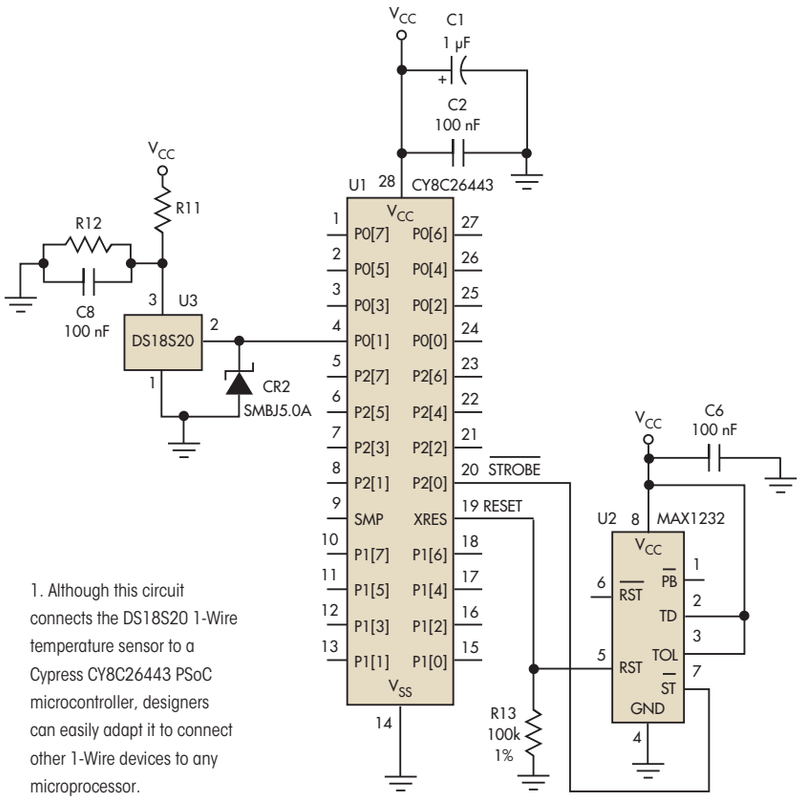
I chose the DS18S20 digital thermometer because it is a very cost-effective 1-Wire device and has an accuracy of 0.5°C, although the overall design achieves 1°C of accuracy including measurement error due to hardware limitations and test tools, etc. The DS18S20 also supports parasitic power mode, has a programmable temperature threshold, and operates from –55°C to 125°C. With additional hardware and software, it can operate over a distance of a few feet.

Using the DS18S20 in the TO-92 package, pin 1 is connected to ground, pin 2 is the open-drain 1-Wire interface pin used for data input/output and power, and pin 3 is connected to V_{CC} or, if the parasitic power mode is used, to ground. For the device in an SO-8 package, the corresponding pins are 5, 4, and 3, with the remaining pins not connected. Figure 1 shows the circuit schematic. Since the circuit uses power from the board, the device is connected to V_{CC}.

This version of the interface connects the DS18S20 directly to the MCU, essentially on the printed-circuit board (PCB) as if the sensor was part of the microcontroller. The board size assumes that parasitic components are negligible and have no effect on the signal.

Using the PSoC, you can either instantiate the 1-Wire module for the interface or write your own protocol. Instantiating the module reduces the software overhead, but I chose to write my own protocol. Although this added firmware overhead, I avoided using a two-port pin, which the PSoC module requires for data exchange between the MCU and the sensor.

The circuit is very simple. CR2 protects the sensor from surges. R12 is not used in the normal mode. In the parasitic mode, R12 is inserted and R11 and C8 are out. U2, a MAX1232 microprocessor supervisory circuit, is a reset con-

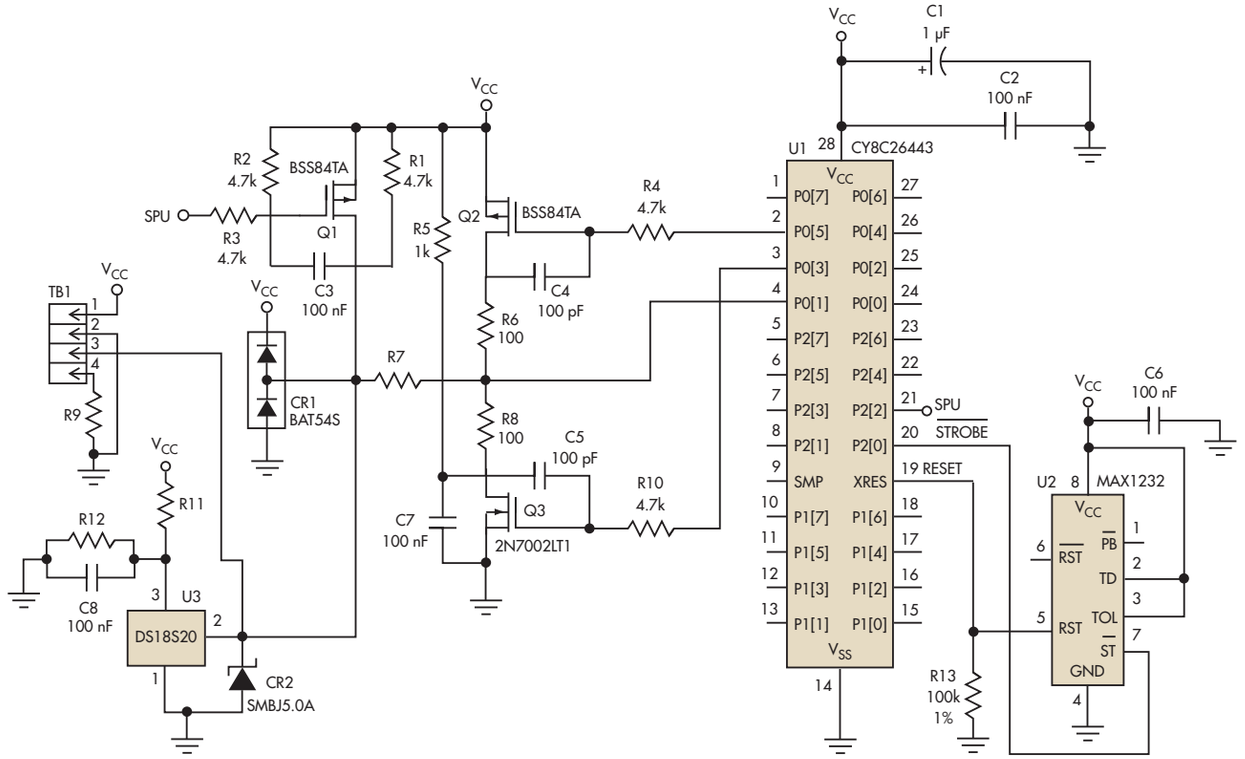


1. Although this circuit connects the DS18S20 1-Wire temperature sensor to a Cypress CY8C26443 PSoC microcontroller, designers can easily adapt it to connect other 1-Wire devices to any microprocessor.

troller and the MCU will strobe it at regular intervals. The code blocks for this interface circuit, along with comments, can be found with the online version of this article at *electronicdesign.com*. The PSoC integrated development environment is available without charge from *www.cypress.com*.

For use at longer distances, the circuit can be extended over several feet with the modifications shown in Figure 2. The additional components ensure that enough source and sink currents are passed through so the timing parameters can be maintained.

The temperature sensor converts and stores the digital data in two registers *(Fig. 3)*. Essentially the resolution of the readout is 9 bits. The least significant byte stores the temperature readout. The most significant byte provides the sign for the readout. In the case where the sign bit is negative (0xFF), the LSB data is two's complemented. Bit 0 in LSB provides the decimal value for temperature: 0.5°C for a logic 1 and 0 for a logic 0. Software is needed to take steps to avoid erroneous readings.



2. With some added components that ensure enough source and sink currents to maintain timing parameters, the sensor can operate up to several feet away from the MCU circuitry.

The circuit additionally includes nonvolatile (EEPROM) memory locations, a T_H and T_L register, to store high and low threshold levels. After the DS18S20 performs a temperature conversion, the temperature value is compared to the user-defined two's complement alarm trigger values stored in the 1-byte T_H and T_L register *(Fig. 4)*. The T_H and T_L register resolution is 8 bits, as opposed to 9 bits for the temperature conversion register.

The circuit's memory map includes a SRAM scratchpad with nonvolatile EEPROM for the T_H and T_L register *(Fig. 5)*. If the alarm trigger function is not required, the T_H and T_L register can serve as general-purpose memory.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LS byte	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MS byte	S	S	S	S	S	S	S	S

S = Sign

3. The sensor stores digital data in two registers. The least significant byte holds the temperature readout. The most significant byte provides the sign for the readout.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

4. If required by the application, the sensor interface can include a nonvolatile memory (EEPROM) register to hold high and low threshold two's complement alarm trigger temperatures.

Resolution greater than 9 bits can be calculated using the data from the registers in the scratchpad—temperature, COUNT REMAIN, and COUNT PER °C, using the equation below, where:

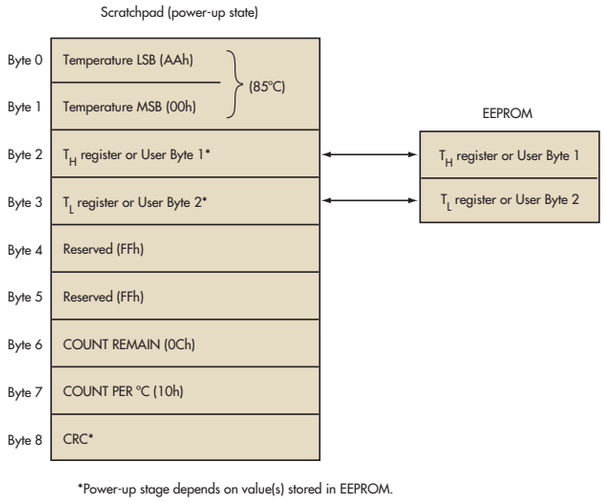
$$\text{Temperature} = \text{TempRead} - 0.25 + \frac{\text{CountPerC} - \text{CountRemain}}{\text{CountPerC}}$$

Temperature = resolution higher than 9 bits

TempRead = temperature obtained by truncating the 0.5°C bit (bit 0) from the temperature data

Count Per °C = COUNT PER °C (byte 7 from scratchpad) = 16 (0x10)

Count Remain = COUNT REMAIN (byte 6 from scratchpad)



*Power-up stage depends on value(s) stored in EEPROM.

5. Besides the EEPROM register for the high and low alarm triggers (T_H and T_L), the DS18S20's memory includes a SRAM scratchpad.

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