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READER SUBMISSIONS DRIVE OUR MOST POPULAR DEPARTMENT

In each issue and online, Electronic Design is proud to present articles spanning the entire electronics industry, from probing Engineering Features by our own staff to insightful columns from our Contributing Technical Experts to practical Design Solutions written by engineers at leading companies.

Overall, though, we get the best feedback about our Ideas for Design. You appreciate these brief articles most of all because they offer hands-on advice for everyday quandaries. In other words, you can go right to your workbench, open up your latest issue of *Electronic Design*, and get to work.

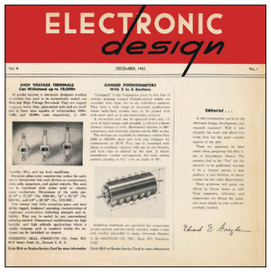
BACK IN TIME

This year, we celebrate *Electronic Design*'s 60th Anniversary with a special look at our most popular department. Electronic Design launched in December 1952, and in the February 1953 issue, Editor Edward E. Grazda asked for submitted articles that are "informative, with practical design information of direct value to the electronic designer." Those early readers responded. That issue also featured what could be called the first IFD, though it didn't carry the department name: "'Hipersil' Design Data Curves" by Paul Muchnick of Sorensen & Company Inc. After a series of articles under the "Design Forum" banner, the first official IFD appeared in the March 15, 1956 issue: "Applying Tape Resistors In Design" by Harlan R. Hansen of Hansen Electronics Company.

Since then, we've published thousands of Ideas for Design. In an introduction to a 1996 supplement compiling the best submissions of that year, Editor Stephen E. Scrupski estimated a collection of more than 4000 articles. And we've only grown since then. In this issue, we look at how the department has evolved, reprinting classic submissions from 1956, 1962, 1972, 1982, 1993, and 2002 just as they originally appeared. Analog/Power Editor Don Tuite offers some commentary on each of these gems, explaining how they were unique to their time—or perhaps something that would still work today.

Also in this issue, we present a selection of contemporary Ideas for Design (p. 39). Some of these IFDs are a bit longer than usual, with more schematics or equations. We're happy to present them here, where they have a little more space than our typical issues. We're also reprinting some of the most popular IFDs, based on Web traffic, of the past three years *(p. 53)*. If you missed them the first time around, or if you'd like a second look, you can take advantage of them here.

Finally, the Ideas for Design department doesn't work without you. Your passion for design is evident in your work and in the comments you send us. Many of you began in your youth, building hobby kits, and that inspiration continues today *(see "The Rise And Fall Of Heathkit—And Rise Of SparkFun," p. 17)*. We want to share your enthusiasm and your innovations with the industry at large. So why not submit an IFD of your own? For details on how you can do that, go to http://electronicdesign.com/Article-Submission. We pay $150 for each IFD published. And who knows? Maybe we'll publish it again in our next anniversary issue. ed



ETCHED BOARD TEST POINTS *JUNE 1, 1956*

NEAL HESS OF HUGHES WEAPONS Systems Development Labs describes how to fabricate a test-probe head that plugs into plated-through holes in a printed-circuit board (PCB). This is more than a year before Sputnik. Even though it was possible to buy a "nine-transistor," battery-powered, AM radio built on a PCB, consumers still were paying a premium for Philco TV sets because of the excellence and reliability of their hand-wired chassis. To most people's minds, the PCB, even with through-hole-mounted components, was newfangled and potentially unreliable.

However, here's an engineer at an aerospace research and developmentfacility talking about the mechanics of test probes. One can imagine going back in a time machine to snatch Mr. Hess and bring him forward to show him the wafer probers that could be found in one of today's semiconductor fabs. The change in scale would impress him, but fundamentally, we're carrying through on what the engineers at Hughes were doing in 1956.

Ideas for Design

1950s

Etched Board Test Points

Neal Hess
Electronic Engineer
Hughes Weapon Systems Development Laboratories

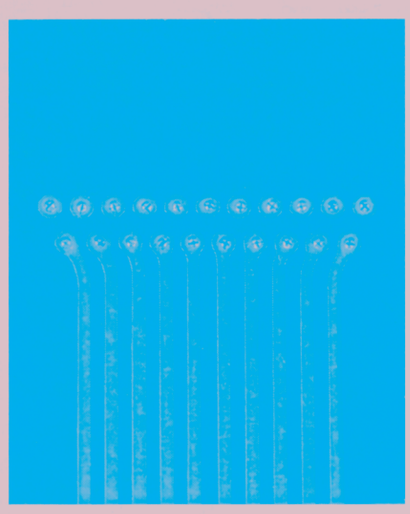


Fig. 2. Bottom side of test board.

TESTING and aligning of electronics circuits fabricated on etched circuit board may be simplified by using plated-through eyelets on the etched board as female test points. The plated eyelet in a standard hole for component lead insertion has approximately a two mil copper plate buildup.

A male pin which mates the plated hole is shown in Fig. 1. The pin is made of beryllium copper and is fired to half hard. The minimum diameter of the pin shaft which is inserted into the etched hole is one mil larger than the maximum hole diameter. Crosscut slots in the pin are eight to ten mils wide allowing any pin produced within tolerance to snugly mate any plated hole within tolerance. When four segments of the male pin are pushed inward by the copper walls the resilient nature of the beryllium copper forces these segments to make a very low resistance contact with the plated walls. A test board before and after a male connector is inserted is shown in Fig. 3. The inserted portion of the male pin length need be no longer than the depth of the etched board as shown in Fig. 2.

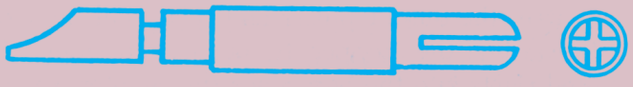


Fig. 1. Pin is made of half-hard beryllium copper.

In most cases the male pin need be inserted only a few times for production testing and trouble shooting. However, typical units produced at Hughes Weapon Systems Development Laboratories have withstood 3000 insertions and withdrawals with very little sign of wear on the male pin and copper plated wall. Temperature cycling had no deleterious effect on the contact.

The male pin was so designed as to fit into commercially available male connector bodies. If any specific configuration is desired, special bodies may be fabricated to retain the male pins. In practice to date, the configuration has been limited to simple row. A typical male connector is shown in Fig. 4.

Use of the plated eyelet reduces the need for wiring in test connectors or the use of test terminals. They allow a higher packing factor to be obtained as single or double test points may be placed in very small areas. Future use of this type of connection is anticipated as a complement to the present etched male connector.

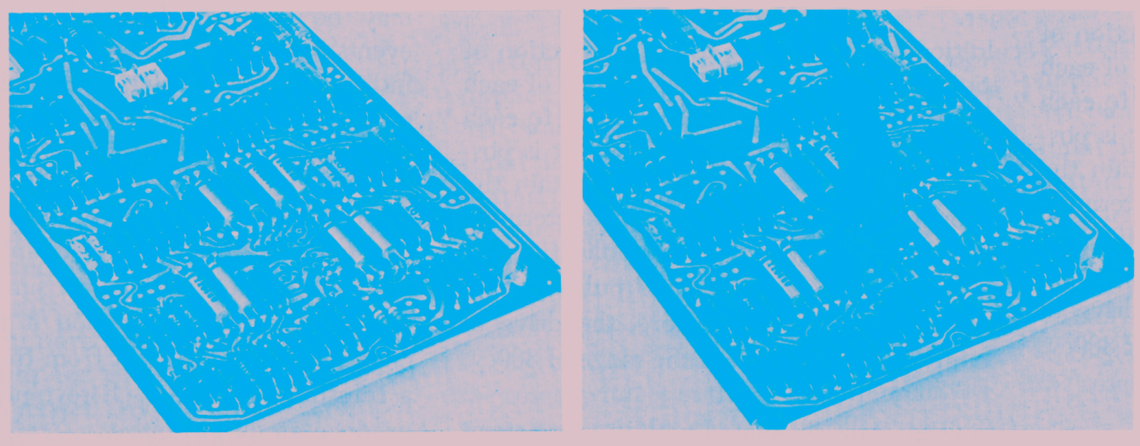
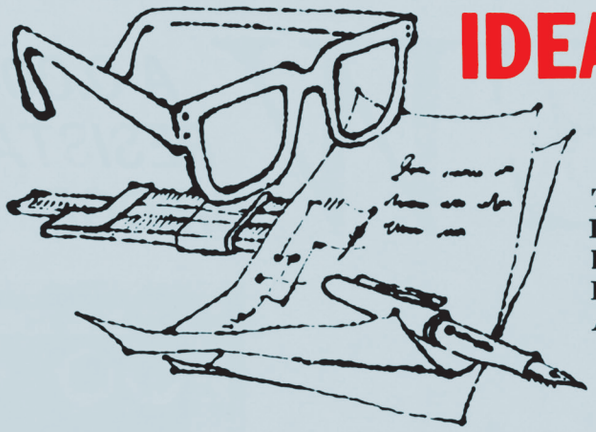


Fig. 3. Test board before and after pin insertion. Pins are mounted in connector bodies as shown in Fig. 4.

Fig. 4. Male pin mounted in standard connector body.

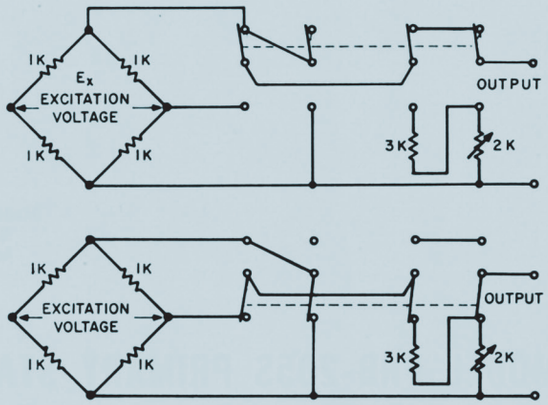


IDEAS FOR DESIGN

Technique For Simulating Strain-Gage-Transducer Signal

107 It is generally agreed that shunt-resistance signal simulation is not suitable for the semiconductor strain-gage transducer. This is due to the relatively large change in bridge resistance with applied input and the high temperature sensitivity of the semiconductors. However an alternate method could be used. The components needed are shown in the diagram.

When a simulation signal is required, the output terminals of the transducer are shorted out, and one of the output connections is transferred to one of the input terminals. The voltage across the output leads will be close to half of the excitation voltage, dependent on the matching of bridge resistors.



Attenuation section of strain-gage signal simulator could be incorporated in common signal conditioner.

The ratio between this voltage and the rated output voltage is slightly more than 2 to 1. To bring the simulated signal down to a voltage suitable for recording or transmission, an attenuator, or voltage divider is used. Using a 3-K and 2-K resistance in series will provide a voltage across the 2-K resistance of about $2/5 \times E_x/2$. With 25-v excitation this will produce a signal fairly close to that of rated output. The described resistance combination will also provide an input impedance to the signal conditioner or recorder, similar to that of the transducer proper.

Any malfunction of the strain-gage bridge will show up as a drastic change in the simulated signal. The latter is in a fixed ratio relationship with the rated output and also directly proportional to the excitation voltage.

The temperature effect on the simulated signal is negligible, amounting to less than 0.2 per cent of rated output over a temperature change of 200 F.

The difference in simulated signal with no pressure or rated pressure applied to the transducer, is about 0.5 per cent of rated output.

This form of simulation also is applicable to the standard wire-type strain-gage transducer. For a 500-ohm bridge with a 10-v excitation and 30 mv rated output the attenuation would be about 200 to 1, which could be accomplished with a 100-K and a 500-ohm resistor in series. Again the impedance presented to the recording or readout device basically would be unchanged. In a telemetry system this method will have the advantage of the elimination of the calibration resistor. The attenuator will be common for all similar transducers. Shorting the output terminals and switching over the output lead easily can be done on a stepping switch, which also will introduce the attenuator into the output circuit when signal simulation is required.

Sigmund Meieran, engineer, The Boeing Co., Seattle, Wash.

If this Idea is valuable to you, give it a vote by circling Reader-Service number 107.

October 11 Winner

John H. Phelps, *manager application engineering,*
General Electric Co., Semiconductor Products Dept.
Syracuse, N. Y.

Mr. Phelps' idea "Unijunction Oscillator Has Frequency Trim Control" has been voted the $50 Most Valuable of Issue Award.

1960s

TECHNIQUE FOR SIMULATING STRAIN-GAUGE-TRANSDUCER SIGNAL *DECEMBER 20, 1962*

SIGMUND MEIERAN OF BOEING DESCRIBES a mechanical switching arrangement that switches an excitation voltage between the output of a bridge sensor and a voltage divider. The object is to validate the performance of the measurement system by simulating a change in sensor output, while continuing to present constant impedance to the test electronics.

Graphically, the schematic requires a little effort to comprehend. Then you realize that it's all based on a four-pole, double-throw switch. In one position (top), the output is connected normally—to the top and bottom terminals of the bridge. In the other switch position, the top and bottom nodes of the bridge are shorted and connected to the lower output terminal, and the right terminal of the bridge is connected to a trimmable voltage divider, with the divided output connected to the upper output terminal.

Conceptually, allowing for today's lower excitation voltages (the 1962 article mentions 25 V), the technique should still be handy. As it was back in 1962, industrial process control continues to use bridge sensors. The difference is in the signal conditioning and processing downstream.

Unrelated to this particular IFD, this magazine page includes an announcement of the previous issue's "Most Valuable" IFD award, as judged by readers—$50. That would be about $380 in today's currency.

Looked at another way, it would have bought 167 gallons of gasoline. Unfortunately, the reward did not kept up with inflation, disappearing eventually because, before the Internet, counting bingo-card mail-in ballots every month came to represent just too much overhead.

The December 20 issue also featured "DC-Servo Amplifier Has Single-Ended Drive" by Richard Shaum of Sandia Corp., "Pulse Detection Circuit Monitors Computer Operation" by V. Lemley of Librascope Inc., "Four Design Techniques For Two-Terminal Regulators" by Ronald Zane of UC Berkeley, and "Audio Frequency Amplifier Responds Over 10-Cps Bandwidth" by Paul Fung of Westrex Co.

Eliminate troublesome common-mode output voltages in IC video amplifiers

There are problems when the dc common mode output voltage is removed from a video amplifier. They include temperature drift and frequency-response degradation. The circuit shown in Fig. 1 avoids these problems. A series string of diodes shifts the voltage and the output voltage can be made independent of temperature.

Other approaches that the designer might be tempted to take—such as the circuits shown in Figs. 2a and 2b—do not compensate for the temperature dependence of the diode voltage drops, while the use of a current source (Fig. 2c) degrades the high-frequency response.

In the circuit of Fig. 1 the output of the IC amplifier is fed to emitter follower Q_1 which provides isolation. A resistive divider, R_1 and R_2, in the Q_1 emitter circuit shifts the output level. Emitter follower Q_2 isolates the load from the level-shifting network. If we assume that $V_{BE(Q1)}$, $V_{BE(Q2)}$ and V_D (the voltage drop per diode) are equal, then N, the number of diodes, can be calculated so that the output voltage is independent of temperature. (Diode strings, such as the CA 3039, or a transistor array, such as the CA 3046, satisfy these requirements.)

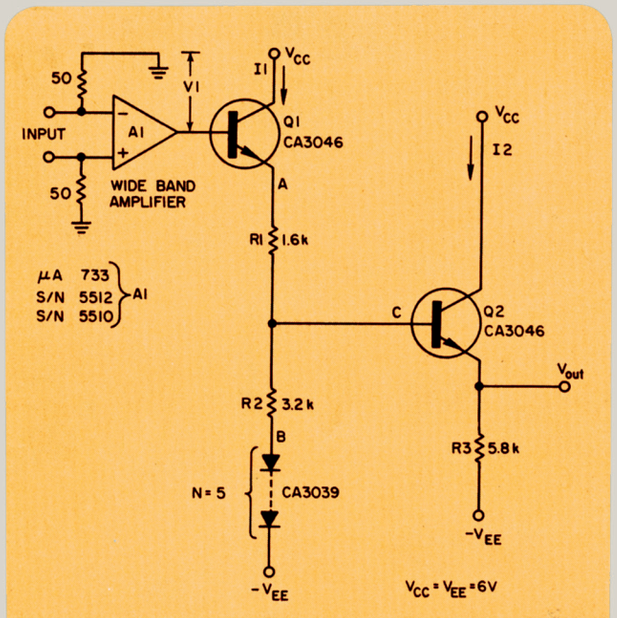
A design example will illustrate the technique. Assume that V_{BE} and V_D are both equal to 0.7 V while V_{EE} equals 6 V. Also let $V_1 = 3.0$ V and N equal 5. Then V_A equals 2.3 V and V_B equals −2.4 V. If I_1 is set at 1 mA, R_1 and R_2 are computed to be 1.6 kΩ and 3.2 kΩ, respectively. Thus V_C is 0.7 V and V_{OUT} is zero.

Next, assume a negative 2 mV/°C temperature coefficient for the diode and transistor junctions. And let the temperature rise from 25 C to 75 C. Then, at 75 C, $V_A = 2.4$ V, $V_B = -3.0$ V and $V_C = 6$ V. Hence V_{OUT} is still zero.

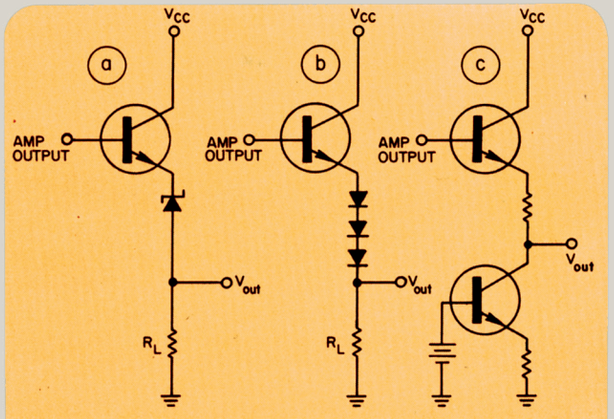
This circuit removes common-mode output voltages from 2.4 to 3.4 V, which are found in commercially available video amplifiers. One should apply appropriate bias at the input of the IC to make its dc output voltage correspond to an integral number of diodes.

S. Sareen, Design Engineer, Aertech Industries, 325 Steward Dr., Sunnyvale, Calif. 94086.

CIRCLE NO. 311



1. **Temperature drift and poor response are avoided** with this configuration. Q_1 changes the output level and Q_2 unloads the resistive divider.



2. **Circuits a and b remove the common-mode output** but are temperature-sensitive. Circuit c degrades the frequency response.

ELIMINATE TROUBLESOME COMMON-MODE OUTPUT VOLTAGES IN IC VIDEO AMPLIFIERS

DECEMBER 7, 1972

BY THE TIME THIS COLLECTION hits the early 1970s, monolithic op amps were common. However, they weren't without "gotchas," including output common-mode voltages that were inconvenient if the circuit designer were using direct coupling to the following stage. Here, S. Sareen of Aertech Industries explains how to (and how not to) remove the offending offset from the output of video op amps.

The concept is based on using an an emitter follower with a voltage divider in the emitter lead that includes a string of diodes along with resistors. The signal is picked off at the point where the output offset is cancelled, as in Figure 2.

The problem is that what we would call V_f today (which the author calls V_D), varies inversely with temperature by -2 mV/°C The IFD provides an algorithm for picking the resistive elements of the emitter-bias totem pole to compensate for the temperature effects. The author also points out that the constant-voltage-drop (diodes or Zener) elements must be on the lower side of the pick-off point in the voltage divider.

1980s

IdeasForDesign

D-type flip-flop ends FIFO multiple pulsing

A D-type flip-flop with an asynchronous clear function lends itself nicely to the task of preventing multiple output pulsing from a first-in, first-out (FIFO) memory. A brief look at how a FIFO works shows the occasional need for additional hardware to ensure that only one byte of data is processed for each shift pulse.

Data is clocked into a FIFO when the proper pulse is applied at the Shift In terminal. When the device is full, the Input Ready line goes low, serving to inhibit the input of more data. Similarly, the Shift Out pulse serves to put out data. The Output Ready line will be high only when data can be shifted out, and it will go low when the FIFO is empty.

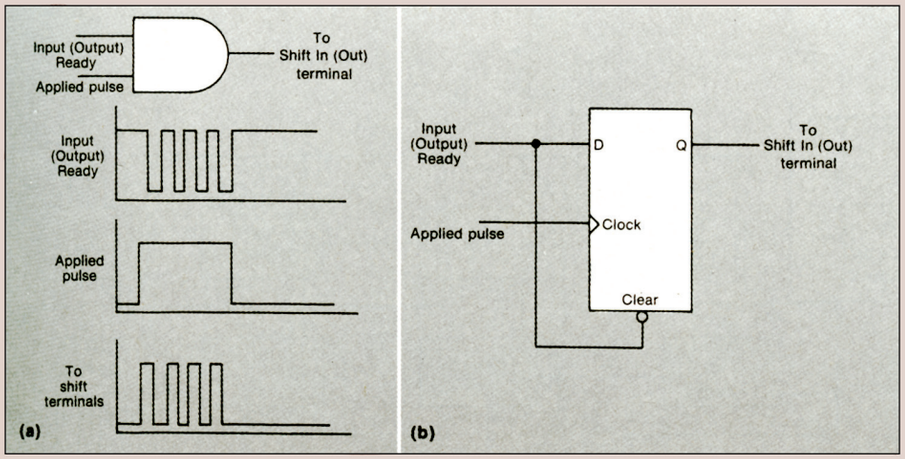
The Input Ready and Output Ready lines mean just that: during the brief interval following the Shift In pulse, the Input Ready line goes low, and it remains low until after the incoming data has been "digested." In a like manner, the Output Ready line goes low immediately after the Shift Out pulse appears, and it remains low until the next byte can be shifted out. Therein lies the problem.

Although it is tempting to direct the shift pulse and the corresponding ready line to the inputs of an AND gate, this may cause multiple shift pulses (a). The asynchronous clear line on the flip-flop, connected to the Input or Output Ready lines (b) guarantees that each shift pulse will result in the processing of just a single byte of data.

Another potential pitfall exists for the inexperienced FIFO user who has not delved deeply into published specifications. Although a data rate of 15 MHz may be attributed to a device, careful reading may show that the first byte of data requires 2.2 μs to "fall through" so that it can be shifted out.

Finally, some FIFOs of recent manufacture will clear all data upon command—both the data stored in the device and that present on the output pins. However, earlier versions may leave the data on the output pins untouched after a clear command. That can cause vexing problems when FIFOs are cascaded to process multiple bytes.

Irwin Feerst, Consulting Electronics Engineer, 368 Euclid Ave., Massapequa Park, N.Y. 11762.



An AND gate, a seeming problem solver for the slightly delayed responses of a FIFO's Input Ready and Output Ready lines, turns out not to be the sought solution. Application of the Ready signal with an applied pulse may result in multiple pulses (a). The asynchronous clear function of a D-type flip-flop prevents that (b).

D-TYPE FLIP-FLOP ENDS FIFO MULTIPLE PULSING

OCTOBER 28, 1982

THE AUTHOR OF THIS BIT of advice about how to properly clock a FIFO is none other than Irvin Feerst, the most vigorously outspoken champion of the working engineer of the second half of the twentieth century and perennial thorn in the side of the IEEE, which he felt helped encourage a surplus of engineers, helping companies drive down salaries.

This IFD demonstrates the clarity of his writing style. It's 1982, so many designers are using discrete FIFOs to buffer data. Feerst reminds readers of the basics of FIFO timing. Then he points out that if the designer falls for the trap of ANDing SHIFT-IN or SHIFT-Out and the corresponding READY lines, he can cause multiple shift pulses, as in Figure a. Syncing everything up with a D flip-flop, as in b, prevents the problem. He then points out the need to realize that first-byte latency is not the same as clock rate, except in continuous operation, and that older flip-flops do not clear the data from the last cycle after a "clear" command —another potential "gotcha."

CIRCLE 521

BUILD A DIGITAL TEMP MONITOR

JIM HULSEBUS
Miltope Corp., 76 Pearl St., Springfield, VT 05601.

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award.

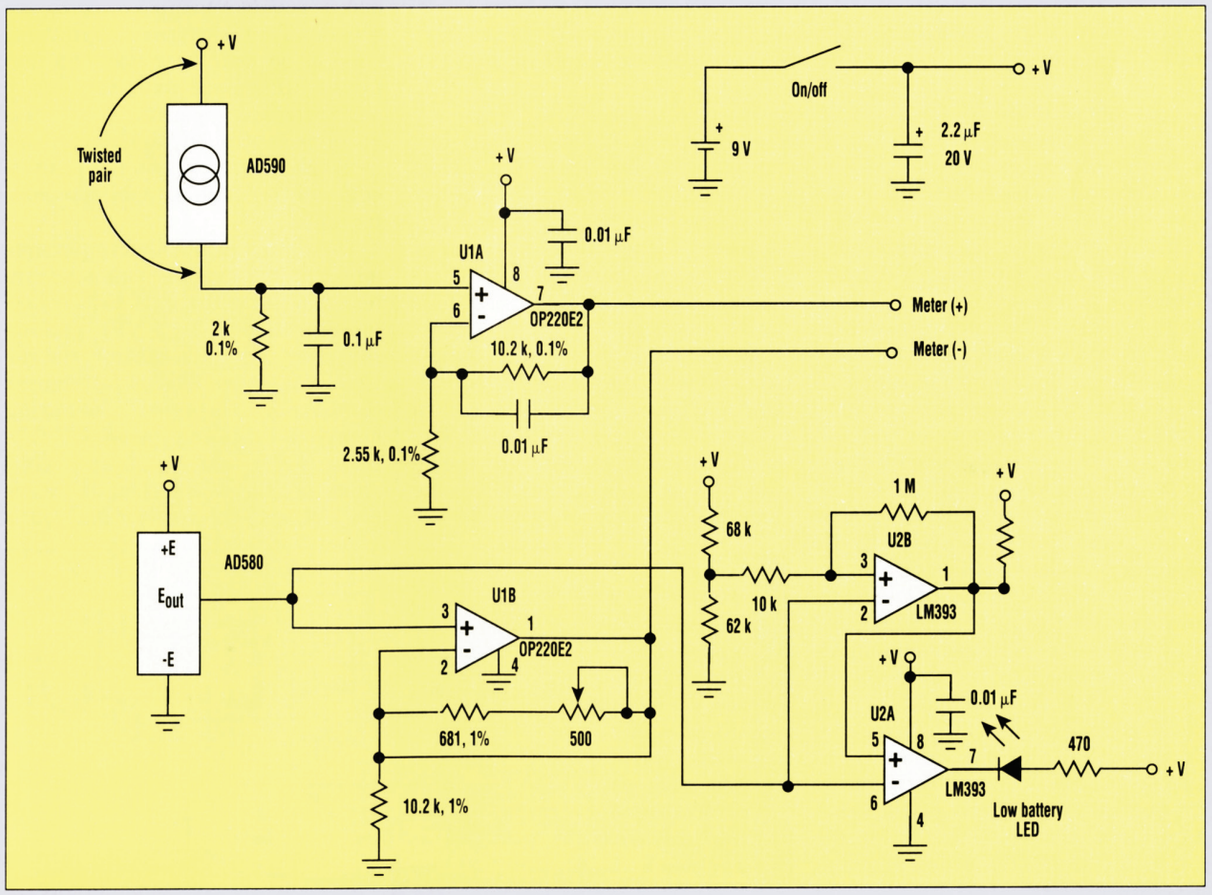
The AD590 proportional-to-absolute - temperature (PTAT) device combined with an autoranging digital multimeter (DMM), such as Fluke's Model 77, can make a stable digital temperature-monitoring device. This holds true particularly for long distance temperature measurements, up to 100 ft.

Looking closely at the circuit *(see the figure)*, U1A forms a current-to-voltage and voltage-amplifier circuit for the total range of the AD590, –50°C to +150°C. The output of U1A then becomes the positive lead of the DMM. U1B forms a 0°C reference and calibration circuit, based upon the AD580 precision voltage reference device. This, in turn, becomes the negative lead of the DMM. The AD590 has a certain amount of calibration error, depending upon the device's grade. The 500-Ω trimmer pot removes the error at 25°C.

U2 is a basic comparator that forms a low battery voltage circuit. If the battery falls below 5.1 V, the LED will turn on, signaling that the battery should be replaced.

To calibrate the device, U1B's output should be set to 2.730 V (0.0°C) by adjusting the 500-Ω pot. Next, the AD590 must be attached as shown in the figure. Then, with a calibrated temperature measuring device, the 500-Ω pot should be adjusted for the correct temperature reading at 25°C. The reading on the DMM will have to be moved two decimal places to the right for final reading. For example, if the meter reads .285, the actual temperature is 28.5°C. An autoranging DMM, such as the Model 77 or an equivalent, is recommended.

The battery will last about two weeks in continuous operation. If its shut off when not operating, it will obviously last much longer.□



A STABLE DIGITAL TEMPERATURE MONITOR can be created by combining the AD590 proportional-to-absolute-temperature device with an autoranging DMM. It is particularly effective for long-distance measurements up to 100 ft.

BUILD A DIGITAL TEMP MONITOR

DECEMBER 2, 1993

THE BEST IFDS COMBINE SIMPLICITY with utility. Here, Jim Hulsebus explains how to set up an Analog Devices' AD590 sensor to remotely read temperatures over as much as 100 feet and output the results directly on the voltage display of a digital multimeter (DMM).

There isn't much need for a mental conversion. As Hulsebus says, a reading of 0.285 V on the multimeter means 28.5°C at the sensor. The active devices comprise an ADI AD580 2.5-V voltage reference and the two halves of an OP220 dual op amp. A separate LM393 circuit does duty as a battery monitor with an LED that stays lit until the battery needs replacing or recharging. The schematic shows a conventional 9-V battery, and the short description says it should last two weeks in continuous use.

Hulsebus worked for Miltope, a military weapons contractor. With a 9-V battery for power and a stock multimeter for readout, it's clear this design isn't borrowed from a weapons application. Instead, it's the kind of thing that makes IFDs popular in the first place—the product of an engineering mind that can't stop thinking, "Wouldn't it be neat if...."

For Just Pennies, Boost Current From Negative Linear Regulator

Chad L. Olson

Maxim Integrated Products Inc., Sunnyvale, CA; e-mail: Chad_Olson@maximhq.com

CIRCLE 521

Adding four components to a negative linear regulator (U1 in the figure) increases the load current by 60%. The additional pass transistor and associated resistors cost less than $0.17 in 1000-unit quantities.

Connecting the SET terminal to ground keys U1's output voltage to –2.5 V. U1's maximum load current is 200 mA. The extra components (Q1, R1, R2, and R3) draw another 120 mA maximum from the load. This produces a total maximum load current of 320 mA without degrading the output regulation.

In addition to reducing the power dissipated in Q1, R1 prevents thermal runaway in Q1 and provides momentary protection against a short-circuited output. By limiting gain in the Q1 loop, R1 also prevents oscillation. Current flowing through U1 from OUT to V_{SS} produces a voltage drop of V_{R2} across R2 and R3, which enables Q1 to conduct load current as V_{R2} approaches the base-to-emitter threshold of Q1. This threshold (V_{BE}) is approximately 0.7 V at room temperature.

Choose the values of R1, R2, and R3 to ensure that R2, R3, and Q1 dissipate maximum power at the maximum load current (320 mA in this case). At 320 mA, U1 conducts 200 mA and Q1 conducts 120 mA. Component power dissipation at maximum load is as follows:

$$P_{R1} = I_{R1}^2 \cdot R1 = 120\ mA^2 \cdot 9.1\ \Omega = 131\ mW$$

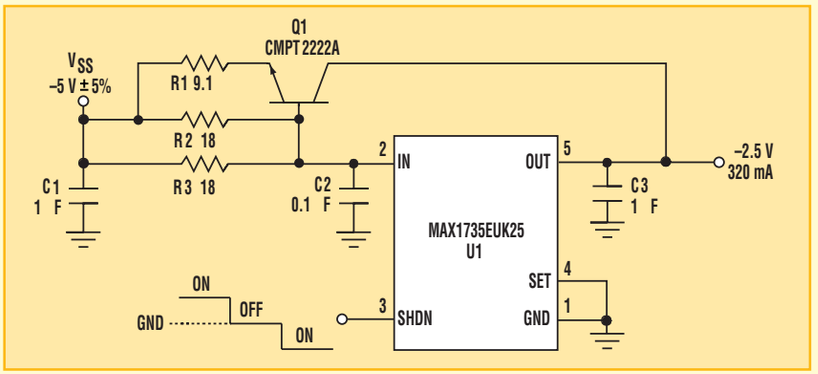
$$P_{Q1} = V_{Q1} \cdot I_{Q1} = (V_{SS} \cdot V_{R1} \cdot V_{OUT}) \cdot I_{Q1} = (5\ V \cdot 1.1\ V \cdot 2.5\ V) \cdot 120\ mA = 168\ mW$$

$$P_{R2} = I_{R2}^2 \cdot R2 = 100\ mA^2 \cdot 18\ \Omega = 180\ mW$$

$$P_{R3} = I_{R3}^2 \cdot R3 = 100\ mA^2 \cdot 18\ \Omega = 180\ mW$$

$$P_{U1} = V_{U1} \cdot I_{U1} = (V_{SS} \cdot V_{R2} - V_{OUT}) \cdot I_{U1} = (5\ V \cdot 1.8\ V \cdot 2.5\ V) \cdot 200\ mA = 140\ mW$$

To provide higher load current, you can easily modify the circuit by increasing the power-dissipation ratings of R1, R2, R3, and Q1. The table details the components shown for a 320-mA load current. For power dissipation, the circuit board should have ample copper connected to the leads of power-dissipating components. Heat then conducts through the component leads to the circuit board, spreads into the copper areas, and exits the board through convection.



COMPONENTS USED IN EXAMPLE CIRCUIT

Component	• Manufacturer • Part Number • Description	Package	Power dissipation	Allowable power dissipation at 85°C
R1	Kamaya Inc. RMC18-9R1JB 9.1-Ω ±5% resistor	1206	250 mW derate 4.55 mW/°C above 70°C	181.75 mW
R2, R3	Kamaya Inc. RMC18-18RJB 18-Ω ±5% resistor	1206	250 mW derate 4.55 mW/°C above 70°C	181.75 mW
Q1	Central Semiconductor Corp. CMPT2222A NPN transistor	SOT23-3	350 mW derate 2.8 mW/°C above 25°C	182 mW
U1	Maxim Integrated Products MAX1735EUK25 200-mA negative LDO	SOT23-5	571 mW derate 7.1 mW/°C above 70°C	464.5 mW

FOR JUST PENNIES, BOOST CURRENT FROM NEGATIVE LINEAR REGULATOR

NOVEMBER 25, 2002

WHAT DO WE KNOW ABOUT November of 2002? The technology boom of the previous decade had imploded, military action in Iraq was in the cards, and nobody knew what to expect next. It was a bad time to splurge. What could be more appropriate than an IFD that took an existing analog voltage regulator and boosted its maximum load current by 60% at a parts cost of less than two dimes? That's what Maxim Integrated's Chad Olson gave us. In the process, he provided a general lesson in how to add an external pass device to any monolithic regulator.

Not surprisingly, he chose one of Maxim's regulators. The Electronic Design staff has internal debates about using ideas written by apps engineers who work for the companies whose products are featured in the schematic. Our policy is that, if the idea is generic enough and helpful enough, either as a solution to a tricky problem, or as an illustration of a general approach, we're happy to present it. (Just be sure to talk it over with your company's marketing department first.)