

by Arild Kolsrud

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ADC Signal-To-Noise Ratio Performance—Finding The Right Balance Between Clock-Signal Quality And Jitter

Predicting SNR requires a comprehensive computation plan involving specification of numerous variables and measurement of different clock speeds, clock-line filter bandwidths, encode and signal levels, and signal frequencies.

By Arild Kolsrud, akolsrud@aol.com

High-dynamic range radio receivers for systems like OFDM and WCDMA rely heavily on the analog-to-digital converter (ADC). If each bit resolution of the ADC is theoretically worth 6.02 dB of dynamic range $(20 \times \log_{10} (2^N) = 6.02N(dB))$, a 14-bit ADC would yield 84-dB dynamic range.

However, imperfections in the real world, such as thermal noise, Johnson noise, random fluctuations in semiconductor devices' transconductance, and jitter, will more likely result in a 73-dB signal-to-noise ratio (SNR). Many noise sources are labeled and modeled in semiconductor circuits (e.g., shot noise, flicker noise, popcorn noise, etc.).^{1,2} This paper, however, will focus on jitter, which relates the system's clock quality to ADC performance.

Typically, the ADC on a radio receiver is clocked from a fundamental harmonic sinusoidal signal. This sine-wave signal then goes to a single-ended-to-differential transformer; two Schottky diodes are connected in parallel but opposite of each other on the output of the transformer (*Fig. 1*).^{3,4}

In this scenario, the transformer used on both of the radio's boards is a standard surface-mount, low-frequency, 1-to-4 impedance transformer, and the Schottky diodes are low 1/f noise standard Avago HSMS-2812 devices. The Schottky diodes would simultaneously square the sine-wave signal and limit the voltage swing to about 0.4 V p-p.



1. A single-ended-to-differential clock squaring circuit typically contains two Schottky diodes connected in parallel.

Computing RMS Clock Jitter

A common specification for sine-wave clock-signal purity is phase noise, or widening in power spectrum. Phase noise is defined as "noise power in a 1-Hz bandwidth at a frequency f(Hz) away from the carrier/power level of the carrier."⁵ The first step in calculating equivalent clock jitter from the given phase noise involves summing or integrating the total noise power in the sideband.

There are two ways to obtain total noise power:

• Approximate the slope of the phase noise to sections of major constant slopes described as a function of frequency or $1/f^n$, where n equals the steepness of the slope.^{6,7}

• Take an actual measurement of the sine-wave with a phase-noise measurement instrument and perform a numerical integration of the data points collected from the test.

The first method yields a fairly accurate result when handling sine-waves with equivalent clock jitter roughly 10 ps and below, but fails to accurately compute the high picosecond clock-jitter signals. Numerical integration of the measured data points, which must be a two-dimensional data array with columns frequency offset and $\mathscr{L}(f_m)$, can be done simply in Excel, MathCad, or Matlab. First, the data points must be converted into a linear scale:

$$\Psi_{i} = 10^{\frac{\Phi_{C} - \Phi_{i} dB}{10}} (\mathsf{mW}_{Hz})$$
(1)

where Ψ_i is the phase noise of the *i*-th data point (mW/Hz); Φ_C is the amplitude of the fundamental harmonic (dBm); and Φ_{i_dB} is the original measured phase noise of the *i*-th data point (dBc/Hz). Then, numerical integration of the two-dimensional array can be calculated:

$$P_{SSB} = \sum_{i=f_2}^{f_M} \left[(f_i - f_{i-1}) \cdot \left(\frac{\Psi_i + \Psi_{i-1}}{2} \right) \right]$$
(mW) (2)

where P_{SSB} is the total noise power (mW) in a single sideband, f_2 is the second data point (Hz) of the phase-noise measurement, and f_M is the last data point taken (upper limit) of the phase-noise measurement (Hz).

The first term in Equation 2 represents the bandwidth between two data points taken, and the second term averages the power spectra between the two data points. This paper uses rectangular approximation windowing. To obtain the total noise power, simply multiply the result in Equation 2 by two, assuming the two sidebands are identical. The relationship between relative phase fluctuation and resulting phase noise $\mathscr{L}(f_m)$ (described as Lorentzian power spectra) is not covered here.

By treating the total noise (obtained via numerical integration in Equations 1 and 2) as phase modulation, rms jitter can be converted in seconds by using:

$$t_{j} = \frac{\sqrt{2 \cdot \frac{P_{SSB}}{\Phi_{C}}}}{2 \cdot \pi \cdot f_{C}} \quad (sec)$$
(3)

where f_C is the frequency of the measured clock signal to be analyzed. If P_{SSB} is in dBm, then substitute Equation 3 with:

$$t_{j} = \frac{10^{\frac{3+P_{SSB(dBm)} - \Phi_{C(dBm)}}{20}}}{2 \cdot \pi \cdot f_{C}} \quad (sec)$$
(4)

where the 3+ $P_{SSB (dBm)}$ doubles the single sideband noise to accommodate for both sidebands (same as the $\sqrt{2 \cdot P_{SSB(mW)}}$ term in Equation 3).

In Equations 3 and 4, the ratio of noise power over carrier power determines the clock jitter. Since $\mathscr{L}(f_m)$ equals the noise power relative to the carrier power, a simpler approach would be to use Equation 1 without considering the carrier power. Combining Equations 1 and 2 (by taking advantage of the ratio of powers), the final equations for rms clock jitter becomes:

$$P_{SSB} = \sum_{i=f_2}^{f_M} \left[(f_i - f_{i-1}) \cdot \left(\frac{10^{\frac{\Phi_i}{10}} + 10^{\frac{\Phi_{i-1}}{10}}}{2} \right) \right]$$
(5)
$$t_j = \frac{\sqrt{2 \cdot P_{SSB}}}{2 \cdot \pi \cdot f_C}$$
(6)

In an illustration of phase noise and clock jitter (*Fig. 2*), the signal S(t) consists of two major terms—the fundamental harmonic and a summation term of the noise components defined by a random variable (ξ). If a higher-order harmonic is employed as a clock signal, the same procedure obtains the rms clock jitter; however, the sideband noise's integration is now performed around the harmonic used.



2. In this analogy between phase noise and clock jitter, signal S(t) consists of the fundamental harmonic and a summation term of noise components.

ADC Clock Jitter Versus SNR Performance

When relating the clock jitter of the sinusoidal signal clocking the ADC to SNR performance, the most commonly used equation is: 3,4,8,9,10

$$SNR = 20 \cdot \log_{10} \left(2\pi f_{signal} \cdot t_j \right)$$
(dB) (7)

where f_{signal} is the frequency (Hz) of the analog input signal at the ADC; and t_j is the rms clock jitter in seconds. The derivation of this equation is shown in Appendix A.

Equation 7 would yield a correct SNR of a perfect discrete sampler, but it's too conservative when computing for rms clock jitter in a real-life ADC environment. For this scenario, the author wrote a Matlab program to simulate and verify the equation. Appendix B describes the source code developed, as well as several issues that arose.

The SNR obtained from Equation 7 gives the best theoretical performance achievable for any ADC given the rms clock jitter. Figure 3 (and later on in Figures 5 and 6) shows that this is not the case, though (to be described in greater detail later in the paper).



3. Shown is a comparison of results obtained from Equation 7 and a Matlab-simulated ADC device.

Agilent/HP's HP8648C, HP8642b, HP8644B and HP81110A generators were used to clock AD6644, Analog Devices' 14-bit high-speed ADC. In addition, two low-cost (\$2.00 per device) square-wave crystal oscillators clocked the device under test (DUT). The crystals, from Oak Frequency Control (OFC) and CTS Corp., oscillated at 62.208 MHz and 66.6666 MHz,

respectively. Appendix C provides the phase-noise plots of the fundamental harmonic of these devices. Table 1 shows the corresponding single sideband noise power and resulting rms clock jitter.

Source	$P_{SSB}/P_C (dB)^*$	f_{C} (MHz)	<i>t_j</i> (rms ps)
HP8642B	-48.90	68.00	11.89
HP8644B	-67.81	68.00	1.35
HP8648C	-51.01	68.00	9.32
HP81110A	-34.48	68.00	62.52
OFC 62.208 MHz	-45.31	62.208	19.64
CTS 66.6666 MHz	-27.91	66.6666	135.79

 Table 1: Calculated P_{SSB}, t_i For The Six Clock Sources

 ${}^*P_{SSB}/P_C$ gives the ratio of the power level of total single sideband noise power to center frequency power measured in 1-Hz bandwidth. This column is simply 10·log₁₀ (Equation 5). Integration was performed from 1 Hz to 1 MHz.

Examples of calculating rms clock jitter from measured phase noise are carried out in Appendix D. That section also reveals how the method suggested in J. Adler's "Clock-Source Jitter: A Clear Understanding Aids Oscillator Selection," *EDN*, was performed and then compared with actual measured data.⁶ As will be explained later, the method presented in the aforementioned article and M.Kolber's "Predict Phase-Noise Effects in Digital Communications Systems," *Microwaves & RF*, doesn't yield the correct answer for rms clock jitter.^{6,7}

The 14-bit AD6644 was clocked with the six clock sources *(Table 1)*. The HP8664B, HP8642B, HP8648C, and HP81110A signal generators had two independent variables adjusted during test—frequency and signal level. Because the two square-wave crystal oscillators had fixed amplitude and frequency, they could not be adjusted. The analog input signal's amplitude was always adjusted to be –0.5 dBFS (dB below full scale) of the ADC.

SNR was recorded for six different analog input frequencies: 15, 40.4352, 62.208, 80, 100, and 150 MHz. The three lowest analog input frequencies were filtered with Piezo Technology Inc.'s four-pole, 20-kHz crystal bandpass filter. The 80-MHz frequency was filtered with a 12-MHz bandpass filter from K&L, and standard tubular bandpass/lowpass filters from Mini-Circuits filtered the two highest frequencies. Results for SNR versus analog input frequency and encode level, when clocked from HP8648C signal generator, are shown (*Fig. 4*). Appendix E provides the block diagram of the test circuit and all SNR plots of the signal generators used in the test.

68-70 66-68 70 64-66 68 62-64 66 60-62 64 **58-60** 62 56-58 60 54-56 58 52-54 SNR (dBm) 56 50-52 54 48-50 52 46-48 50 44-46 48 42-44 46 40-42 15 38-40 44 12 42 40 Encode Level 38 Incident (dBm) 3 15 40.4352 62.208 0 80 100 150 Analog Input Frequency (MHz)

HP8648c as Clock Source Without Clock Filtering

4. Tests performed on Analog Devices' AD6644 ADC reveal the SNR versus both analog input frequency and encode level. The device was clocked by the HP8648C signal generator, and no noise-limiting filters were on the clock line.

Figure 4 indicates the ADC's performance improves with higher encode, or clock, levels. That's because the slew rate of the squared sine-wave clocking the DUT is much faster for higher encode levels. The SNR for a 15-MHz analog input frequency at an encode level of 0 dBm is 59 dB; at a 15-dBm encode level, it improves to 70 dB.

As shown in Appendix E, the ADC's SNR improves steadily for higher encode drive levels. When dealing with high phase-noise clock sources, SNR improves significantly by increasing the encode level. Clock-line noise filtering plus an increased encode level further enhances SNR. Overall, noise bandwidth-limiting filtering applied to the clock signal will augment SNR (*Figs. 5 and 6*). Appendix F shows the frequency response of the filters.



5. The HP8648C signal generator was used as the clock source when testing the AD6644 ADC for SNR.



6. The HP81110A signal generator was used as a clock source when testing the AD6644 ADC for SNR.

Another plot shows the phase noise of the HP8648C signal generator when filters are applied *(Fig. 7)*. The equivalent rms clock jitter is extracted from the measured phase-noise data points by means of numerical integration, as seen in Equations 5 and 6, and can be summarized in Table 2.



7. Different clock-line filters were applied to test the HP8648C's phase noise.

Clock-line filtering	Clock frequency (MHz)	RMS clock jitter (ps)
None	68.000	9.04
Broadband	68.000	9.39
Narrowband	62.208	9.84

 Table 2: HP8648C RMS Clock Jitter With Different Filters

Broadband clock-line filtering yields a higher jitter number than no filtering at all, which is most likely caused by a small error in the measurement of phase noise from 1 Hz to 10 Hz (*Fig. 7, again*). The 20-kHz clock-line filtering (narrowband) yields a 0.8-ps higher jitter number versus

no filtering, which is due to lower frequency of operation. This is because the jitter equation is inversely proportional to frequency of operation, as seen in Equations 3 and 6. However, despite the small difference in calculated rms clock jitter, the ADC experiences significantly improved SNR performance (*Fig. 5, again*). The same situation occurs with the HP81110A signal generator (*Fig. 6, again*).

The HP81110A pattern generator had a 62.5-ps rms clock jitter at 68-MHz frequency of operation. Furthermore, a 3.4-ps rms clock jitter (as obtained from using Equation 6) is plotted on the SNR versus frequency plot if the device is used as an ADC clock (*Fig. 6, again*).

When broadband clock-line filtering is applied (which doesn't change the close-in phase noise), a 1.9-ps rms clock jitter curve can be plotted over the measured SNR performance of the DUT. The same development occurs with the HP8648C signal generator, which has a 9-ps jitter number at 68 MHz. A 2.7-ps theoretical jitter curve can be plotted over the measured SNR performance when there's no clock-line filtering.

However, when narrowband clock-line filtering is applied to both HP8648C and HP81110A, it's impossible to fit the theoretical SNR-clock jitter curve so that it follows the DUT's measured SNR performance. Thus, it can be concluded that Equation 7 doesn't hold for modern conversion devices. Using this equation will result in over-specification of the required phase noise for certain SNR performances of ADCs.

Searching For A New SNR Equation

As mentioned, applying Equation 7 for SNR is too simple; clock jitter can't be extracted directly by integrating the phase noise of the clock source. The expression for SNR in Equation 7 might be accurate for low-resolution, high-speed converters. However, it doesn't predict the performance of high-speed, high-resolution converters, where the converter's smallest quantization step (q) falls dangerously close to minimum achievable resolution limited by the speed and the physics of semiconductors. For example, the thermal noise of a 100-MHz bandwidth spectrum in a $50-\Omega$ system is:

$$V_{rms} = \sqrt{4 \cdot 1.38 \cdot 10^{-23} \cdot 295 \cdot 10^8 \cdot 50} = 8.99 \mu \text{V}$$

If the ADC has 1-V p-p full scale, the resolution for 14- and 16-bit devices becomes 21.6 μ V rms and 5.4 μ V rms, respectively. To repeat, ADC SNR performance is a function of encode level, analog input frequency, noise bandwidth on the clock line, and the shape of the clock source's phase noise. It's apparent that the equation for describing the SNR will contain multiple terms with multiple variables.

To find a new equation that more accurately describes ADC SNR performance, one must first distinguish the types of jitter in the sampling system. There are two types of jitter: sampling circuit jitter (or aperture uncertainty jitter), and the instability of the signal source that's clocking the sampler device (clock jitter). Sampling circuit jitter is the instability in the timing of the sampling gate's switch. This jitter is caused by the amplitude noise of both the sampler's amplifiers and the sampling clock signal generator. Since the clock jitter tracks the analog input signal's SNR performance over different amplitude levels as well as the analog input signal's frequency.



8. SNR is compared to the analog input signal's amplitude and frequency when a HP8648C signal generator clocks a specific ADC at 68 Msamples/s.

The total voltage error due to both clock jitter and sampling circuit noise (derived in Appendix G) is:

$$SNR = 10 \cdot \log_{10} \left(\frac{V^2_{signal,rms}}{v_{e_jitter}^2 + v_{e_sampler}^2} \right)$$
(8)

where $v_{e_j itter} = \sqrt{2\pi f} V_0 \cdot t_j$, which is the noise voltage due to clock jitter (*f* is the analog-inputsignal frequency (Hz); V_0 is the peak amplitude (V) of the analog input signal; t_j is the rms clock jitter (in seconds) for 1 standard deviation; and $v_{e_sampler}$ is the rms noise voltage created by the circuit elements in the sampling front end.

Referring to Appendix G, clock jitter and sampler-circuit noise voltage can be determined by using Equations G6 and G7 on the measured results shown in Figure 8. If Equation G7 is rewritten to solve for $v_{e-sampler}$, it results in:

$$v_{e_sampler,rms} = \frac{V_{in_p-p}}{2\sqrt{2} \cdot 10^{\frac{SNR}{20}}}$$
(9)

which, from Figure 8, yields 128.4 μ V rms at 1 mV_{in} p-p, 125.5 μ V rms at 10 mV_{in} p-p, and 118.4 μ V rms at 100mV_{in} p-p.

The aperture equivalent clock jitter can be extracted by using Equation G6, thus becoming:

$$SNR = 10 \cdot \log_{10} \left(\frac{\left(\frac{V_{0,p}}{\sqrt{2}} \right)^2}{\left(\sqrt{2}\pi f \cdot t_j \right)^2} \right) = 20 \cdot \log_{10} \left(2\pi f \cdot t_j \right)$$
(10)

which is the same Equation A3 as derived in Appendix A. The equivalent aperture clock jitter extracted from Figure 8 is approximately 2.5 ps—much smaller than 9.04 ps as calculated in Appendix D and shown in Table 2.

However, the graph in Figure 8 was for an incident clock level of 15 dBm (or $1.778 V_P$ in this case). When information in Figure 4 is re-plotted as a 2D plot together with two theoretical SNR clock-jitter curves (Equation A3), it's evident that a clock slew-rate term must be included in Equation 10 (Fig. 9). Figure 5 plots the AD6644 ADC's measured SNR versus analog input frequencies for three different cases of clock-line filtering, which indicates that a noise bandwidth term must be added to Equation 10, too.



9. This plot shows the SNR of the AD6644 versus analog input frequency for different encode, or clock levels, when clocked from an HP8648C generator without clock-line filtering.

A rigorous but incomplete model was proposed in "Jitter Analysis of High-Speed Sampling Systems" by M. Shinagawa, et al, *IEEE Solid-State Circuits*.¹² A method for obtaining the three

jitter components was shown and proved, but the jitter-suppressing bandwidth function was briefly mentioned and it omitted the clock slew rate. Consequently, a sampling-speed term must be added as well (*Figs. 10a and 10b*). This term will also depend on the phase-noise characteristic of the sinusoidal clock.

Figures 10a and 10b can be divided into two regions. Region I corresponds to performance degradation due to aperture uncertainty (or clock jitter) on the samples taken. The sampling-speed limitation of the ADC's sampler front end dominates region II. (Figure 10 was extracted from DUTs that max out at 65 Msamples/s.)



10. SNR versus encode rate (sampling speed), with a -0.5-dBFS, 15-MHz analog signal at the input, is given for an SNR device (a) and a clock-jitter device (b).

As seen in Figures 10a and 10b, the sampler performs satisfactorily at a maximum specified sampling rate for high phase-noise clock signals (high jitter), but maintains poor performance at slower sampling rates. When clocked by a low-jitter clock source, the sampler performs uniformly well over a wide range of sampling speeds up to the breakdown of the sampler front end.

An equation for approximating the behavior of the three jitter components was proposed by Shinagawa, et al:¹²

$$t_{j}^{2} = t_{S}^{2} + \left[t_{clk0}\frac{f_{clk0}}{f_{clk}}\right]^{2} + \left[t_{sig0}\frac{f_{sig0}}{f_{sig}}\right]^{2}$$
(11)

where t_j represents the overall jitter; t_s is the aperture uncertainty of the sampler itself; t_{clk0} is the clock source jitter; t_{sig0} is the jitter component (amplitude jitter) of the analog signal source; and f_{clk0} and f_{sig0} are two constants. By applying Equation 11 to the numbers in Table 3 (that partially make up the high phase-noise curve in Figure 10b), an approximation equation can be made as seen in Shinagawa et al.¹²

<i>f</i> _{CLK}	f_{SIG} (MHz)	t_j (ps)
(Msamples/s)		-
28	15	5.97
70	15	3.13
59	80	2.81
43	15	4.42

 Table 3: High Phase-Noise Clock Jitter Performance

The three first rows in Table 3 are used to obtain three sets of equations to solve for t_s , t_{clk0} , and t_{sig0} :

$$5.97^{2} = t_{s}^{2} + \left[t_{clk0}\frac{70\cdot10^{6}}{28\cdot10^{6}}\right]^{2} + \left[t_{sig0}\frac{15\cdot10^{6}}{15\cdot10^{6}}\right]^{2}$$
(12)

$$3.13^{2} = t_{s}^{2} + \left[t_{clk0} \frac{70 \cdot 10^{6}}{70 \cdot 10^{6}}\right]^{2} + \left[t_{sig0} \frac{15 \cdot 10^{6}}{15 \cdot 10^{6}}\right]^{2}$$
(13)

$$2.81^{2} = t_{s}^{2} + \left[t_{clk0} \frac{70 \cdot 10^{6}}{59 \cdot 10^{6}}\right]^{2} + \left[t_{sig0} \frac{15 \cdot 10^{6}}{80 \cdot 10^{6}}\right]^{2}$$
(14)

The resulting equation for approximating the ADC's overall clock-jitter performance becomes:

$$t_j^2 = 0.887^2 + \left[2.22\frac{70\cdot10^6}{f_{clk}}\right]^2 + \left[2.013\frac{15\cdot10^6}{f_{ana\log}}\right]^2 \text{(ps)}$$
(15)

This particular equation holds true for HP8644B as the analog-signal generator, HP8648C as the clock generator without clock-line filtering, and AD6644 as the ADC. Looking at Equation 15, when clock-generator jitter improves (as is the case when using narrowband clock filters), the overall resultant clock jitter will simply be $\sqrt{0.887^2 + 2.013^2} = 2.2 \text{ ps}$. This is represented by the low phase-noise generator clock-jitter curve in Figure 10b.

Clocking the ADC at different clock levels will improve SNR performance (*Fig. 11*). The ADC circuit's clock-level limiter limits the clock swing to 0.4 V p-p, while the ADC chip itself limits the clock level to 0.2 V p-p. Performance improves substantially with a high-jitter clock source and an increased slew rate of the clock signal. When clocking a low-jitter clock source with a faster slew rate, SNR improvement is minimal due to the ADC front-end sampler limitation.



11. SNR performance improves when clocking an ADC at different clock levels.

The incident encode level (clock level) to the ADC evaluation board can be translated into voltage level by using:

$$V_{p-p} = \sqrt{8 \cdot Z_0 \cdot 10^{\frac{dBm-30}{10}}}$$
(16)

where Z_0 is the characteristic impedance of the clock line and dBm is the sine-wave power level.

It's been proven a clock signal's high slew rate creates a jitter-reducing effect (*Figs. 9 and 11, again*). Figures 5 and 6 illustrate the jitter-reducing effect noise-limiting clock-line filters have on an ADC's SNR performance. If these factors are combined with Equation 11, a more complete equation for overall jitter of the ADC system can be written as:

$$t_j^2 = t_s^2 + \left(\frac{BW}{BW_0} \cdot \frac{Enc_0}{Enc} \cdot t_{CLK0} \cdot \frac{f_{CLK0}}{f_{CLK}}\right)^2 + \left(\frac{BW}{BW_0} \cdot \frac{Enc_0}{Enc} \cdot t_{SIG} \cdot \frac{f_{SIG0}}{f_{SIG}}\right)^2$$
(17)

where BW is the 3-dB bandwidth of the noise-limiting clock line filter; BW_0 is a constant that roughly corresponds to the 3-dB bandwidth of the front end sampler; *Enc* is the clock level (in volts); and *Enc*₀ is a constant (in volts) that corresponds to the maximum SNR performance versus clock level.

Effects Of Non-Harmonic Spurious Content

Since the conversion of the analog domain incident on an ADC always folds down to the first Nyquist zone, any harmonic of the clock frequency will fold over to either dc or fs/2. Hence, it will not show up in an FFT plot. Such is not the case with non-harmonic spurs on the clock line. When the jitter noise consists of a single-frequency sinusoid, the jitter signal will mix with the

input signal and produce two distinct tones around the input frequency. To prove the sensitivity of a modern high-speed, 14-bit ADC, several tests were performed on different ADCs (*Fig. 12*).



12. This test setup was used to verify an ADC's sensitivity to non-harmonic spur content on the clock line.

A non-harmonic signal was deliberately injected onto the clock line at an offset of 1 MHz away from the main encode clock. It wound up modulated around the analog input signal at an offset of 1 MHz (*Fig. 13*).

The amplitude of the spur is 67.2 dB below the analog signal, which creates a clock-input to analog-input isolation of 67.2 dB - 56.5 dB = 10.7 dB. In other words, the ADC is a highly sensitive mixer—the clock input is comparable to the LO port of a mixer, an ADC's analog input is comparable to a mixer's RF input, and an ADC's digital output is simply a mixer's IF output. However, a mixer has between 15 to 25 dB LO-RF and LO-IF isolation, and this particular ADC had only 10.7dB. Other ADCs under test showed up to 20-dB isolation.



13. Shown is the measured response of a DUT when a non-harmonic clock spur was injected onto the clock line.

The behavior illustrated in Figure 13 can be explained by looking at the ADC as a multiplier of the signals present at both clock and analog input. The clock signal can be written as:

$$V_{clk}(t) = V_C \cdot \sin(2\pi f_{clk} t) \tag{18}$$

and the non-harmonic spur on the clock line can be written as:

$$V_{spur}(t) = V_N \cdot \sin\left(2\pi f_{spur}t\right) \tag{19}$$

The sampler's clock circuit can be explained as a multiplier of the clock-line signals, hence:

$$V_m(t) = V_{clk}(t) \cdot V_N(t) = V_C \cdot \sin(2\pi f_{clk}t) \cdot V_N \cdot \sin(2\pi f_{spur}t)$$
(20)

and by using the trig identity:

$$\sin x \cdot \sin y = \frac{1}{2}\cos(x - y) - \frac{1}{2}\cos(x + y)$$
(21)

the resultant signals are produced by the sampler's clock circuit:

$$V_m(t) = V_1 \cdot \cos\left(2\pi \left(f_{clk} - f_{spur}\right)\right) + V_2 \cdot \cos\left(2\pi \left(f_{clk} + f_{spur}\right)\right)$$
(22)

where V_1 and V_2 are the resultant voltage levels after multiplication and suppression in the sampler's front end. The width of the Nyquist zone is $f_{clk}/2$; all signals above this frequency will fold over into the first Nyquist zone. The folding and its resultant signal can be described as:

$$V_{FNZ_even} = V_0 \cdot \sin\left(2\pi \left(\frac{f_{clk}}{2} \cdot N - f_{signal}\right)t\right)$$
(23)

when the original signal was located in an even numbered Nyquist zone. Also:

$$V_{FNZ_odd} = V_0 \cdot \sin\left(2\pi \left(f_{signal} - \frac{f_{clk}}{2} \cdot (N-1)\right)t\right)$$
(24)

when the signal was located in an odd zone. *N*, the number of the Nyquist zone, is ≥ 2 . As is the case in Figure 13, $f_{clk} = 68$ MHz and $f_{spur} = 67$ MHz. The resultant frequencies become 1 MHz and 135 MHz. The 135 MHz is located in the fourth Nyquist zone. Equation 23 is used to obtain the "folded down" frequency of 68 MHz \cdot 0.5 \cdot 4 – 135 MHz = 1 MHz. The two resultant frequencies from Equation 22 will fold back on to the same frequency.

Now, the resultant signal (V_m) in Equation 22 is multiplied with the analog input signal, which is switched by the sampler's track-and-hold amplifier through to the quantitizer:

$$V_{f inal}(t) = V_{FNZ}(t) \cdot V_{ana \log}(t) = V_{f nz} \cdot \sin\left(2\pi \left(\left|f_{signal} - \frac{f_{clk}}{2} \cdot N\right|\right)t\right) \cdot V_0 \cdot \sin\left(2\pi f_{ana \log}t\right)$$
(25)

Equations 21 and 25 then will obtain:

$$V_{f inal}(t) = V_x \cdot \cos\left(2\pi \left(f_{ana \log} - \left|f_{signal} - \frac{f_{clk}}{2} \cdot N\right|\right)t\right) + V_y \cdot \cos\left(2\pi \left(f_{ana \log} + \left|f_{signal} - \frac{f_{clk}}{2} \cdot N\right|\right)t\right) + V_{ana \log} \cdot \sin\left(2\pi f_{ana \log}t\right)$$
(26)

As is the case in Figure 13, the three resultant frequencies would be 53 - 1 = 52 MHz; 53 + 1 = 54 MHz; and 53 MHz. When folded into the first Nyquist zone, they become 68 - 52 = 16MHz; 68 - 54 = 14 MHz; and 68 - 53 = 15 MHz.

Conclusion

It's been shown that the direct translation of phase noise to rms clock jitter (or one standard deviation clock jitter), as derived in Equations 1 and 6, is too conservative. Equation 7 offers a simplistic way to determine an ADC's SNR performance (derived in Appendix A), but it doesn't hold up for modern high-speed, high-resolution ADC systems.

To predict an ADC's SNR performance, many variables must be specified. Thus, as shown, the variables identified and evaluated empirically were the clock signal's slew rate, bandwidth of noise-limiting clock-line filters, ADC sampler front-end noise, front-end sampler jitter (aperture jitter), clock jitter, and signal-source amplitude jitter.

Different clock speeds, clock-line filter bandwidths, encode levels, signal levels, and signal frequencies must be measured to fully characterize a modern ADC. From these measurements, it's then possible to devise a complete behavioral to compute expected SNR performance.

References:

1. Wacker, M., "Frequency Stability Characterization in the Time Domain", Application Note, Oak Frequency Control, 1997.

2. "Phase Noise Theory and Measurement," Application Note, Aeroflex, Plainview, NY, 1995.

3. AD6640 Datasheet Analog Devices, Norwood Mass.

4. AD6644 Datasheet from Analog Devices, Norwood, Mass.

5. Cheng, B., "Signal Generator Spectral Purity Considerations in RF Communications Testing," *Microwave Journal*, Aug. 1999.

6. Adler, J., "Clock-Source Jitter: A Clear Understanding Aids Oscillator Selection," *EDN*, Feb. 18, 1999.

7. Kolber, M., "Predict Phase-Noise Effects in Digital Communications Systems," *Microwaves & RF*, Sept. 1999.

8. Kessler, W., High Speed Design Techniques, Analog Devices, Norwood, Mass., 1996.

9. Demler, M., *High-Speed Analog-to-Digital Conversion*, Academic Press, San Diego, Calif., 1991.

10. Tsui, J., *Digital Techniques for Wideband Receivers*, Artech House, Boston, Mass., 1995. 11. Harris, F., "On The Use of Windows for Harmonic Analysis with Discrete Fourier Transform," *Proc. of IEEE*, Vol. 66, No. 1, Jan. 1978.

12. Shinagawa, M., et al, "Jitter Analysis of High-Speed Sampling Systems," *IEEE Solid-State Circuits*, Vol. 25, No. 1, Feb 1990.

Related articles:

"Jitter And Its Measurements," Louis E. Frenzel,

http://electronicdesign.com/article/communications/jitter-and-its-measurements3781

"When Testing Jitter, Which Results Should You Believe?" Paul G. Schreier, <u>http://electronicdesign.com/article/test-and-measurement/when-testing-jitter-which-results-should-you-belie</u>

"Clocking Data Converters," Don Tuite, <u>http://electronicdesign.com/article/analog-and-mixed-signal/clocking_data_converters</u>

"Free Noise With Every ADC (While Supplies Last)," Dave Van Ess, <u>http://electronicdesign.com/article/analog-and-mixed-</u> <u>signal/free_noise_with_every_adc_while_supplies_last_</u>

Appendix A

An ADC's theoretical SNR, provided in Equation 5,^{9,10,11} is derived using a sinusoidal signal and sampling at the signal's point of highest slew rate. To find the theoretical signal's slew rate, the derivative of the signal is taken:

Slew Rate =
$$\frac{\partial V}{\partial t} = \frac{\partial V_0 \sin(2\pi f)}{\partial t} = 2\pi f V \cdot \cos(2\pi f)$$
 (A1)

At the maximum of the derivative, slew rate occurs naturally for $n \cdot \pi$ where $n = -\infty \dots \infty$. This establishes, as expected, that the fastest slew rate is at zero crossing of the sine wave. Then the sampling error is given by:

$$V_{\Delta} = V_0 \sin\left(2\pi f \cdot t_j\right) \approx V_0 \cdot 2\pi f t_j \tag{A2}$$

where t_j represents the rms clock jitter or sampling point deviation; f is the frequency of the sinewave; and V_o is the absolute amplitude of the signal. Because t_j is very small, the expression for V_a can be approximated by ignoring the sine function of the frequency term as seen in Equation A2.

Subsequently, signal-to-noise ratio (SNR) is defined as the rms of the signal of interest versus rms sampling error. It can can be expressed as:

$$SNR = \frac{V_0}{V_{\Delta}} = \frac{\frac{V_0}{2\sqrt{2}}}{\frac{V_0}{2\sqrt{2}} \cdot 2\pi f \cdot t_j} = \frac{1}{2\pi f \cdot t_j}$$
(A3)

which is expressed in dB as:

$$SNR = 20 \cdot \log_{10} \left(\frac{1}{2\pi f \cdot t_j} \right) \tag{A4}$$

The expression for theoretical SNR obtained in Equation A4 is plotted for different rms clock jitter over frequency (*Fig. A1*). The graph illustrates the resulting SNR (worst case) when sampling a sinusoidal signal for a given rms clock jitter (*Fig. A2*).

Theoretical SNR of Different rms Clock Jitter over Frequency



A1. The expression for theoretical SNR obtained in Equation A4 is plotted for different rms clock jitter over frequency.



A2. In this case, sampling error is due to aperture error or clock jitter.

Appendix B

A Matlab test program was written to simulate SNR performance of a perfect ADC when clock jitter is present in the system. The source code can be found at the end of this appendix. Four-term Blackman-Harris was chosen as the windowing function for the fast Fourier transform (FFT) operation, thus ensuring very low side-lobes and virtually no overlap.¹¹



B1. An FFT plot of a 14-bit ADC with 1-ps rms clock jitter displays "uniform" distribution.

Figures B1 and B2 show the FFT plot of a 14-bit ADC sampled at 68 Msamples/s and with a 51-MHz analog-input-signal frequency. Both plots illustrate the effect of 1-ps rms clock jitter. Figure B1 indicates "uniform" distribution of the jitter, resulting in a 74.5-dB SNR. Figure B2 shows "normal" distribution of the jitter, resulting in a 63.4-dB SNR. The difference in SNR is more evident in Figure B3, which plots the resulting SNR of both noise distributions versus analog input frequency.



B2. This FFT plot of a 14-bit ADC with 1-ps rms clock jitter displays "normal" distribution.



B3. The difference in SNR becomes apparent when comparing uniform versus normal distributed 1-ps rms clock jitter.

```
function jitter
%4-term Blackman-Harris Window coefficients.
a0=0.35875;
a1=0.48829;
a2=0.14128;
a3=0.01168;
menu=input('Do you want to read in a data file (1=yes, 2=no) ? ');
if menu==2
   fs=input('What is the sampling frequency in Msps ? ');
  fs=fs*10^6;
  fc=input('What is the analog input frequency in MHz ? ');
  fc=fc*10^6;
   fft v=input('How big FFT (256, 512, 1024, 2048, 4096, 8192, 16384) ? ');
   t=0:1/fs:fft v/fs; %Scale fft v sampling-points to sampling
frequency.
  N=input('What is the resolution of the A/D ? (in bits) ');
  fullscale=input('What is the full-scale of the A/D ? (Vp-p) ');
                                %Minimum resolution of A/D Converter.
  q=fullscale/2^N;
  tj=input('What is the rms clock jitter ? (in ps)');
  tj=tj*10^-12;
  %Assume a signal at full-scale of A/D Converter.
  %Treat q/sqrt(12) as quantization error.
   8
      t+tj*randn[size(t)] adds the rms clock jitter, tj, to the sampled
   8
       signal
   8
      which is analogous to having aperture jitter on the sampler.
  x=fullscale*sin(2*pi*fc*(t+tj*randn(size(t))));
   %Add quantization error to the signal x(t).
  x=x+q/sqrt(12)*randn(size(t));
end
if menu==1
   disp('The datafile must have two columns containing time and data.')
  disp('Column 1 = absolute time and Column 2 = data value.')
  name=input('What is the file name and path (i.e. c:\\temp\\CDMA.txt) ?
', 's');
   fid=fopen(name);
  b=fscanf(fid,'%g %g',[2 inf]); %The file has two rows.
  fclose(fid);
  b=b';
                                    %Do transpose of array b.
  x=b(:,2);
  ccc=b(:,1);
  fs=1/(ccc(2)-ccc(1));
  fft v=length(x)-1;
  x=x';
end
%Calculate 4-term Blackman-Harris Window.
w=a0-a1*cos(2*pi*(1:fft v+1)/fft v)+a2*cos(2*pi*2*(1:fft v+1)/fft v)-
a3*cos(2*pi*3*(1:fft v+1)/fft v);
%Use 4-term Blackman-Harris Window on samples.
x=w.*x;
%Main FFT routine.
x2=fft(x,fft v);
                      %Do a fft v point FFT of the sampling-point array x
pxx=abs(x2).^2/(fft v+1);
                           %Convert the FFT points to energy by a crude
                             8
                                 approximation of Welch's method.
f=fs*(0:fft v/2)/fft v;
                             %Scale the FFT plot according to sampling
                                  frequency.
                             8
pyy=10*log10(pxx);
                             %Convert the FFT points to dBFS.
```

```
8-----.
pyy=pyy-max(pyy);
plot(f, pyy(1: (fft v/2)+1));
%Plot the result of the FFT routine.
grid on;
                           %Activate the grid lines on the plot.
axis([0 max(f) -130 0])
                            %Scale the x and y axis xmin=0, xmax=fs/2,
                            % ymin=-130, ymax=0
set(gca, 'YTick', -130:10:0)
                                  %Y scale in 10 dB increments.
xlabel('Analog Input Frequency (Hz)') %Label the x-axis
vlabel('(dBFS)')
                                     %Label the v-axis
%Calculate SNR for the system.
%Temporary variable that contains maximum value for strongest signal in FFT
    spectrum
8
temp=max(pxx);
%Find frequency bin that contains the FFT spectrum's strongest signal
for i=1:(fft v/2)+1
   if pxx(i) == temp
      center freq=i; %This variable points to the frequency bin with the
                    % strongest signal
   end
end
%Seek out the lowest frequency bin belonging to max signal
for i=center freq-1:-1:1
   if (pyy(i) > pyy(i+1)) \& (pyy(i) > pyy(i+3))
      start freq=i;
     break;
   end
end
%Seek out the highest frequency bin belonging to max signal
for i=center freq+1:1:fft v/2+1
   if (pyy(i)>pyy(i-1)) & (pyy(i) > pyy(i-3))
      stop freq=i;
     break;
   end
end
if (center freq>round(fft v*.01))&(center freq<round(fft v*(1-0.01)))
   %Plots a marker at strongest signal
  hold on
                  %Plot multiple plots/lines/markers on the same plot.
  bin v(1:start freq-1)=-10000;
  bin v(start freq:stop freq)=10000;
  bin v(stop freq+1:fft v/2+1) =-10000;
  plot(f,bin v(1:(fft v/2)+1),'r') %Marker is ('r') RED.
  hold off;
  %Calculate Signal-to-Noise-Ratio
  SNR=0;
  noise=0;
  signal=0;
  for i=1:1:start freq-1
     noise=noise+pxx(i);
   end
   for i=stop freq+1:1:fft v/2+1
     noise=noise+pxx(i);
   end
   for i=start freq:1:stop freq
     signal=signal+0.25*pxx(i);
   end
   SNR=10*log10(signal/noise)
end
```

Appendix C

A number of sources with different phase-noise characteristics were used to test Analog Devices' AD6644, a 14-bit ADC. The plots were obtained using a phase-noise test system. The phase-noise plots of the square-wave crystal oscillators were also obtained from the same test system, which was tuned to the fundamental harmonic.

Phase-noise plots were created for Agilent/HP's HP8642B, HP8644B, HP8648C, and HP81110A signal generators (*Fig. C1*). In addition, phase-noise plots are provided for the two crystals used in the test—a 62.208-MHz crystal from Oak Frequency Control, and a 66.6666-MHz version from CTS (*Fig. C2*). The HP81110A pattern generator had the internal phase-locked loop (PLL) chosen (to achieve higher phase noise so that it could measure noticeably lower SNR) and 50% duty cycle of the square-wave clock signal.



C1. These phase-noise plots represent the output (at 68.00 MHz) of the four signal generators used to clock the AD6644.



C2. The fundamental harmonic of the two square-wave crystals used to clock the AD6644 produced this phase-noise plot.

Appendix D

There are two ways to obtain the equivalent clock jitter for HP's HP8644B signal generator. The first method employs numerical integration of the measured phase noise taken from the phasenoise test system. The second method breaks down the signal generator's phase noise into sections of major slopes, and then, through the use of closed-form equations, obtains the overall noise power in the side-lobes and converts it to rms clock jitter.⁶ Figure D1 shows the measured phase noise of the device and suggested partitions of major slope sections.



D1. This phase-noise plot represents the HP8644B signal generator, which was used in two different methods to obtain equivalent rms clock jitter.

The first example of obtaining the rms clock jitter uses the measured phase noise of the device stored in an array consisting originally of two columns; offset frequency and the relative noise power. The numerical integration, as shown in Equation 5, breaks down into steps *(Table D1)*.

i	Frequency	$\mathcal{L}(f_m)$	Φ_{i_dB}	$\Psi_i + \Psi_{i-1}$	$\Delta f(Hz)$	Last two
	(Hz)	(dBc/Hz)	$\Psi_i = 10^{-10}$	2		columns
		· · · ·				multiplied
1	0.97656	-62.17	6.0674E-7			
2	1.0254	-65.2	3.02E-7	4.5437E-7	0.04884	2.2191E-8
3	1.0742	-64.78	3.3267E-7	3.1734E-7	0.0488	1.5486E-8
4	1.123	-65.7	2.6915E-7	3.0091E-7	0.0488	1.4684E-8
5	1.1719	-65.83	2.6122E-7	2.6519E-7	0.0489	1.2968E-8
6	1.2207	-68.8	1.3183E-7	1.9653E-7	0.0488	9.5907E-9
7						
8						
2025	991210	-149.87	1.0304E-15			
2026	993650	-151.24	7.5162E-16	8.9101E-16	2440	2.174E-12
2027	996090	-151.22	7.5509E-16	7.5336E-16	2440	1.838E-12
2028	998540	-149.46	1.1324E-15	9.4375E-16	2450	2.312E-12
Sum all numbers in last column to get the ratio of total noise power in					1.657E-07	
a single sideband to the carrier power (in 1 Hz bandwidth)						

Table D1: Numerical Integration Of Single Sideband Noise Power

The rms clock jitter is now obtained by using Equation 6:

$$t_j = \frac{\sqrt{2 \cdot 1.65695 \cdot 10^{-7}}}{2 \cdot \pi \cdot 68 \cdot 10^6} = 1.347 \cdot 10^{-12} \text{ seconds}$$

The clock jitter for this generator is calculated to be 1.35 ps.

The second method utilizes closed-form equations for integration; there's no need for the summation of vast arrays. As noted earlier, the phase-noise plot can be broken up into five major slope sections (*Fig. D1, again*). Limits of integration are recognized for the sections marked as A, B, C, D and E (*Table D2*).

	-	-			
Section	Lower frequency	Upper frequency	Lower-side phase noise	Higher-side phase noise	Slope factor $n \begin{pmatrix} 1 \end{pmatrix}$
	(Hz)	(Hz)	(dBc/Hz)	(dBc/Hz)	$\prod_{n=1}^{n} \left(\frac{f^n}{f^n} \right)$
А	1	3	-65	-92	5.66
В	3	13	-92	-100	1.26
С	13	151	-100	-100	0.00
D	151	6,225	-100	-150	3.10
Е	6,225	1,000,000	-150	-150	0.00

Table D2: Limits Of Integration For HP8644B Slope Sections

The slope factor *n* is found by:

$$n = \frac{Lower \ Side \ Phase \ Noise}{10 \cdot \log_{10} (Higher \ Frequency) - 10 \cdot \log_{10} (Lower \ Frequency)}$$

(D1)

The total area, or noise power, under each major slope section is found by:

$$P_i = 10^{\frac{\xi}{10}} \cdot \alpha^n \int_{\alpha}^{\beta} \frac{1}{f^n} df$$
(D2)

where ξ is the phase noise at the lower frequency limit (in dBc/Hz); α is the lower frequency limit; and β is the higher frequency limit (both in Hz). The integration over the major slope terms yields:

$$P_{A} = 10^{\frac{-65}{10}} \cdot 1^{5.66} \cdot \frac{\left(3^{-5.66+1} - 1^{-5.66+1}\right)}{-5.66+1} = 6.745 \cdot 10^{-8}$$
$$P_{B} = 10^{\frac{-92}{10}} \cdot 3^{1.26} \cdot \frac{\left(13^{-1.26+1} - 3^{-1.26+1}\right)}{-1.26+1} = 2.308 \cdot 10^{-9}$$

$$P_{C} = 10^{\frac{-100}{10}} \cdot 13^{0.00} \cdot \frac{\left(151^{-0.00+1} - 13^{-0.00+1}\right)}{-0.00+1} = 1.38 \cdot 10^{-8}$$

$$P_{D} = 10^{\frac{-100}{10}} \cdot 151^{3.1} \cdot \frac{\left(6,225^{-3.1+1} - 151^{-3.1+1}\right)}{-3.1+1} = 7.188 \cdot 10^{-9}$$

$$P_{E} = 10^{\frac{-150}{10}} \cdot 6,225^{0.0} \cdot \frac{\left(1,000,000^{-0.0+1} - 6,225^{-0.0+1}\right)}{-0.0+1} = 9.938 \cdot 10^{-10}$$

The clock jitter is now calculated by using Equation 6:

$$t_j = \frac{\sqrt{2 \cdot \sum_{i=A}^{E} P_i}}{2 \cdot \pi \cdot 68 \cdot 10^6} = 1.003 \cdot 10^{-12} \text{ seconds}$$

Using numerical integration, the rms clock jitter was found to be 1.35 ps. With closed-form integration over approximated major slope sections, clock jitter was found to be 1.00 ps. This suggests that using measured data points to perform numerical integration will yield a more accurate clock-jitter estimate (or $\frac{(1.00-1.35)100\%}{1.35} = -26\%$ difference).



D2. This phase-noise plot represents the HP81110A clock generator, which was used in two different methods to obtain equivalent rms clock jitter.

When computing equivalent clock jitter of a higher phase-noise generator, such as the HP81110A (with phase-noise response as seen in Figure D2), the results from the two integration

The examples described in this appendix illustrate the big difference between approximated closed-form integration and numerical integration using measured data points. Ultimately, the most accurate method is deemed to be numerical integration using measured data points of the phase noise.

Appendix E

SNR performance of the AD6644 ADC was recorded, with the ADC being clocked using different clock quality sources (*Fig. E1*). The data-acquisition (DAQ) board, supplied by Analog Devices, is an evaluation board for the company's single-channel digital downconverter (DDC) AD6620. It interfaces with the PC via the parallel port. The PC then downloads either 1, 2, 4, 8, 16, 32, or 64 ksamples from the AD6620 board's FIFO, on which a FFT algorithm calculates the SNR.



E1. This type of test setup is often used to measure an ADC's SNR.

Figures C1 and C2 show the clock sources' phase noise. The encode levels were all kept consistent at 0, 3, 6, 9, 12, and 15dBm at the evaluation board input containing the DUT. The analog input signal was adjusted to -0.5 dBFS for the purpose of keeping a consistent SNR reading. Each of the four HP signal generators were used to clock the ADC to measure SNR *(Figs. E2-E7).* All of the plots had one common trait—SNR improves at higher analog input frequencies for higher encode drive. That's significant when dealing with a high phase-noise clock source, such as the HP8648B and HP81110A generators.

methods begin to deviate from each other. The major slope sections seen in Figure D2 break down into nine different areas. Table D3 lists the parameters for closed-form integration. Overall, closed-form integration yields an rms clock jitter of 29.53 ps, while numerical integration yields 62.52 ps (or $\frac{(29.53-62.52)100\%}{62.53} = -52.8\%$ difference).

Section	Lower	Upper	Lower-side	Higher-side	Slope factor
	frequency	frequency	phase noise	phase noise	$n\left(\frac{1}{1}\right)$
	(Hz)	(Hz)	(dBc/Hz)	(dBc/Hz)	$\prod_{n=1}^{n} \left(\frac{f^n}{f^n} \right)$
А	1	4	-50	-70	3.32
В	4	42	-70	-80	0.98
С	42	200	-80	-76	-0.59
D	200	580	-76	-68	-1.73
Е	580	2,441	-68	-90	3.52
F	2,441	10,000	-90	-96	0.98
G	10,000	50,500	-96	-124	3.98
Н	50,500	318,380	-124	-140	2.00
Ι	318,380	1,000,000	-140	-140	0.00

Table D3: Limits Of Integration For HP81110A Slope Sections

In another example involving a low-cost square-wave quartz crystal oscillator, numerical integration yielded 135.79-ps clock jitter. In comparison, the approximated method yielded 127.88 ps (or $\frac{(127.88-135.79)100\%}{135.79} = -5.8\%$ difference). The oscillator's phase-noise plot indicates the approximated major slope sections (*Fig. D3*).



D3. This phase-noise plot shows the major slope sections of a low-cost square-wave quartz crystal oscillating at 66.6666 MHz.

HP8642B as Clock Source



E2. The HP8642B signal generator was used as a clock source to measure SNR.



E3. In this test, the HP8644B signal generator was used as clock source to measure SNR. No filtering was applied.

HP8648c as Clock Source Without Clock Filtering







HP8648c as Clock Source with Broadband Clock Filtering

E5. Broadband clock-line filtering was applied in this case (with the HP8648C as the clock source) to measure SNR.

8648c as Clock Source with Narrowband 4-pole 62.208 MHz Crystal Filter









Appendix F

With high phase-noise signal generators, two types of filtering help limit the clock line's noise bandwidth, thus improving the ADC's SNR. The first is a broadband lumped element filter (*Fig. F1*). Featuring approximately 50-MHz bandwidth, it limits only the overall noise bandwidth (not close-in noise). The second type of filter limits the close-in noise as well as far-out noise. Shown are results using the four-pole crystal bandpass filter developed by Piezo Technology Inc. (PTI), which contains 20-kHz bandwidth (*Fig. F2*).



F1. Shown is the measured frequency response when using the broadband bandpass clockline filter.



F2. A narrowband bandpass clock-line filter was used to obtain this measured frequency response.

Appendix G

A sampling device's voltage error can be derived from the slew rate of the analog input signal. The incident instantaneous voltage at the converter is expressed as $v(t) = V_0 \sin(2\pi f)$, where V_0 represents the peak amplitude. By looking at the signal's slew rate, one can derive the resultant voltage error for a given rms jitter (t_j) :

$$\frac{d \cdot v(t)}{dt}\Big|_{rms} \cdot t_j = \sqrt{\frac{1}{T} \int_0^T \left(\frac{d \cdot V_0 \sin(2\pi f t)}{dt}\right)^2 dt} \cdot t_j$$
(G1)

Using the trigonometric relationship:

$$\cos^{2}(\theta) = \frac{1}{2} + \frac{1}{2}\cos(2\theta)$$
 (G2)

will obtain:

$$\frac{d \cdot v(t)}{dt}\Big|_{rms} \cdot t_j = \sqrt{\frac{1}{T} \left(V_0 2\pi f\right)^2} \left[\int_0^T \frac{1}{2} dt + \int_0^T \frac{1}{2} \cos\left(2 \cdot 2\pi f\right) dt\right] \cdot t_j$$
(G3)

Since the cosine term is an odd function, it will integrate to zero. Therefore, the equation for error voltage caused by rms clock jitter becomes:

$$v_{e_j itter} = \sqrt{2\pi} f \, V_0 \cdot t_j \tag{G4}$$

If the error voltage created in the sampling circuit is labeled $v_{e-sampler}$, then the SNR expression for the sampler can be expressed as:

$$SNR = 10 \cdot \log_{10} \left(\frac{V^2_{signal,rms}}{(v^2_{e_j itter} + v^2_{e_sampler})}_R \right) = 10 \cdot \log_{10} \left(\frac{(V_0/\sqrt{2})^2}{\left[(\sqrt{2}\pi f V_0 \cdot t_j) + v^2_{e_sampler} \right]} \right)$$
(G5)

where $v_{e-jitter}$ is the error voltage due to clock jitter and V_0 represents the peak voltage of the analog input signal.

When the clock-jitter term is much larger than the sampler circuit's error voltage, and the analog input signal amplitude also is large, Equation G5 becomes:

$$SNR = -20 \cdot \log_{10} \left(2\pi f \cdot t_j \right) \tag{G6}$$

Conversely, when the sampler circuit's error voltage is larger than the jitter-related noise, which is the case for small analog input signals, SNR can be expressed as:

$$SNR = 20 \cdot \log_{10} \left(\frac{V_0}{\sqrt{2} \cdot v_{e_sampler}} \right)$$
(G7)

ARILD KOLSRUD has worked at Lucent/Bell Labs, Qualcomm, and Texas Instruments. He has a bachelor's and master's degree in electrical engineering from Texas A&M University. He also is the author of four technical papers and holds 17 patents.

