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What's the Difference Between VPX and OpenVPX?

Electronic Design
Justin Moll
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In our previous article (see "What's the Difference Between VME and OpenVPX?"), we laid out the differences between VME and OpenVPX. In this edition, we'll go into detail on the differences between VPX and OpenVPX.

The VPX (VITA 46) specification started around 2005 and was ratified in 2007 as the next generation of VME. However, to handle the speed and differential signaling of switch fabrics, a new connector was required—the MultiGig RT2. There are many benefits with VPX/OpenVPX, including:

• Inherent reliability of a fabrics-based approach

• High-speed MultiGig RT2 connector rated to about 10 Gb/s

• Standard SERDES data-rate options of 3.125, 5.000, and 6.250 Gb/s (with 10 Gb/s and beyond becoming more popular)

• Defined areas for control plane, fabric plane, management, etc.

• Options for system management per VITA 46.11

• Fully tested and rugged differential connectors

• Guide pins on the backplane for easy blind-mating

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The architecture is primarily used in defense and aerospace applications, but has found application in some test-and-measurement, research, and other markets. VPX was rapidly adopted by many of the previous users of VME/VME64x architectures. Since it utilizes the same 3U or 6U Eurocard form factor as VME/VME64x, with 160-mm-depth boards, most of the existing mechanics could be employed.

Although most of the 19-in. rackmount chassis and ATRs could be leveraged, the backplane would be completely different. Also, power requirements typically are higher, which in turn often requires more challenging cooling solutions.

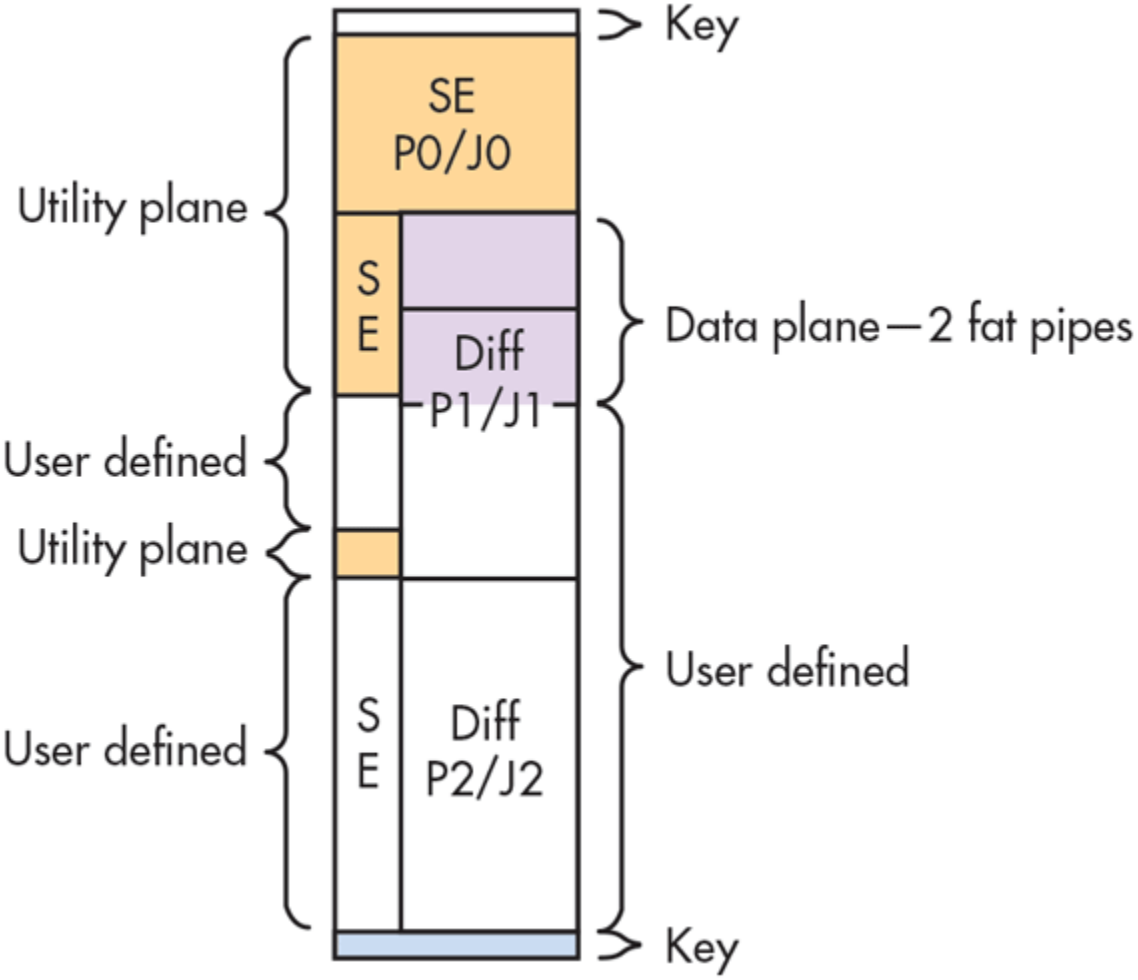
VPX grew, it became clear over time that the flexibility of the specification was less of a virtue than a serious problem. With the variances of signaling (single-ended, x1, x2, and x4, etc.) and the routing options of the various topologies, it was extremely difficult to ensure interoperability across multiple vendors. This feature is a significant aspect of an open-specification solution!

Enter OpenVPX

To address those interoperability issues, the VITA 65 specification for OpenVPX was introduced (ratified in 2009). In short, OpenVPX created profiles (routing classifications) so that vendor A's boards will talk to vendor B's boards in vendor C's backplane/chassis solution.

OpenVPX also defined the "planes" in the specification (control, data, expansion, management, and utility planes) that grouped different types of signals/functions. Then, OpenVPX defined the signal types in "pipe" classes, which include ultra-thin pipe (x1), thin pipe (x2), fat pipe (x4), and double fat pipe (x8) as the principal groups as well as a couple of others.

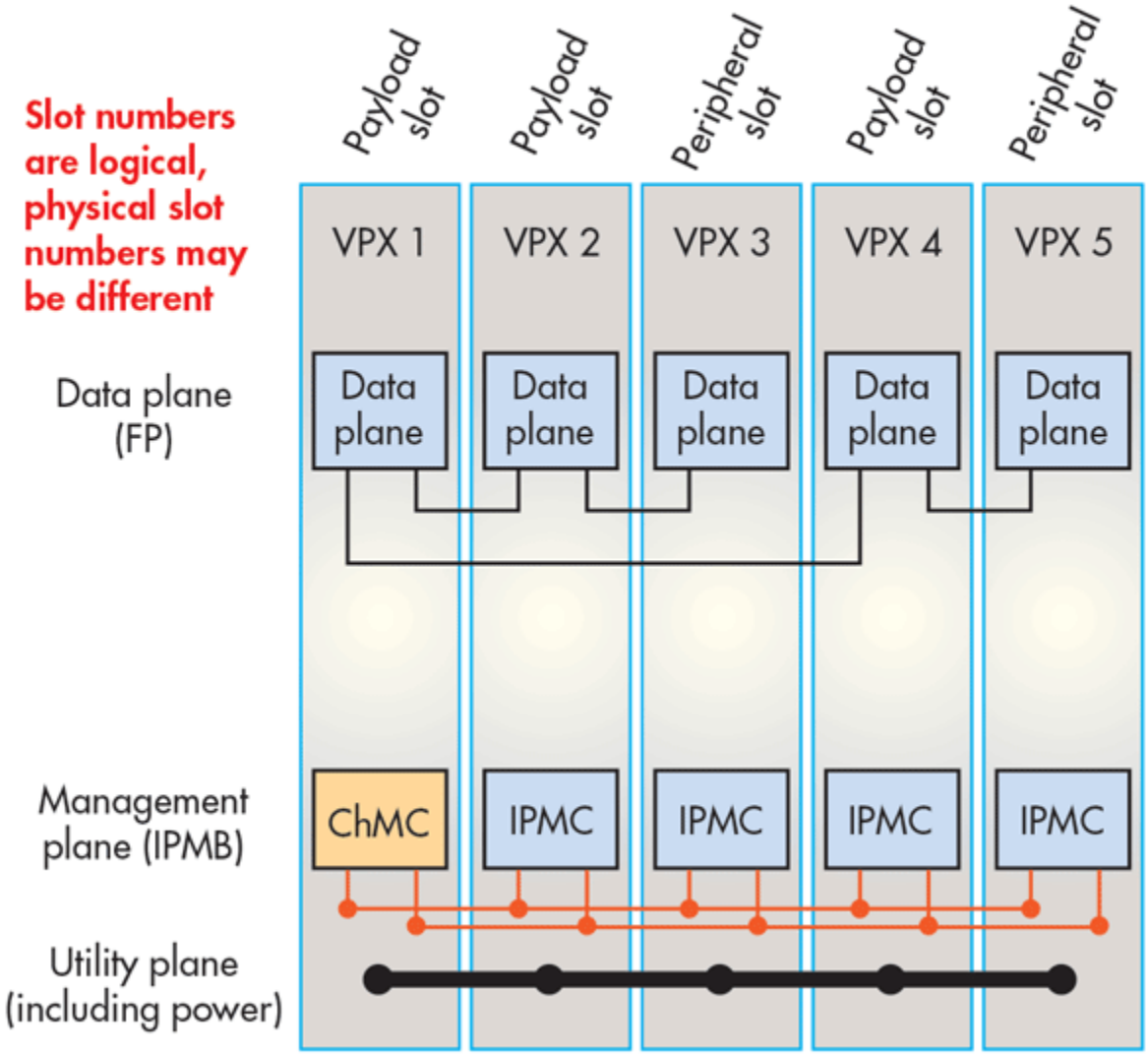
To ensure interoperability, OpenVPX created profiles of 3 categories—the Slot Profile, the Module Profile, and the Backplane Profile.



The *Slot Profile* defines the connector type and provides a physical mapping of ports onto a given slot's backplane connectors. *Figure 1* shows a Slot Profile of a slot in a 3U VPX backplane.

TABLE 1: MODULE PROFILES MOD3-PAY-8U-16.2.9-n	
Profile name	Data plane
	DP01-DP08 ultra-thin pipes
MOD3-PAY-8U-16.2.9-1	PCIe Gen1—2.5 Gbaud per Section 5.3
MOD3-PAY-8U-16.2.9-2	PCIe Gen2—5.0 Gbaud per Section 5.3

The *Module Profile* is a physical mapping of ports onto a given module's backplane connectors. This includes any protocol mapping to the assigned port(s). For example, *Table 1* shows a 3U payload module with eight ultra-thin pipes with options for PCIe Gen 1 or Gen2. The last digits (16.2.9-1 or -2) refer to the location in the specification where there's more detail. The (-1, -2, -3) refers to the speed options, such as 2.5 Gbaud/s, 5.0 Gbaud/s, etc.



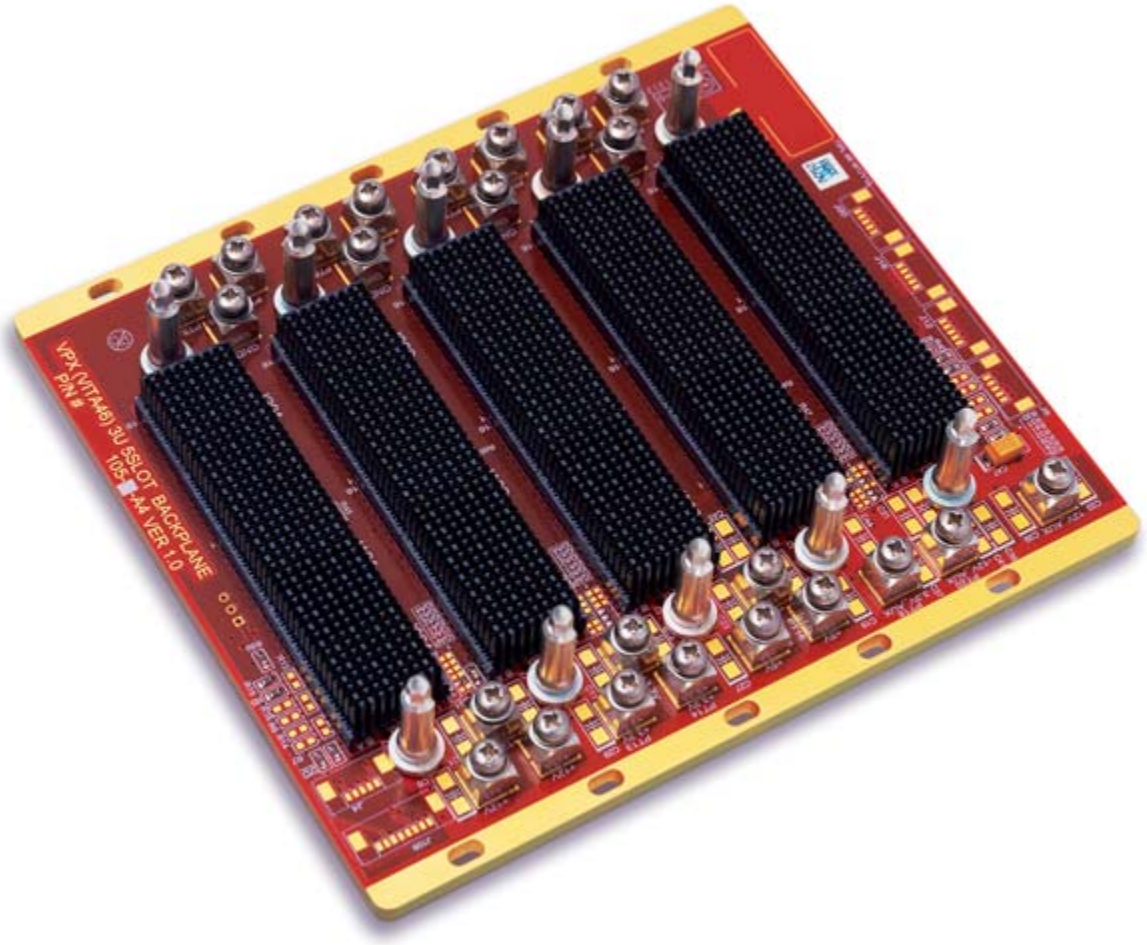
The *Backplane Profile* shows a physical definition of a backplane implementation and the topologies used to

erconnect them. It describes which Slot Profiles are used and the speed options of the backplane. See the kplane profile (BKP3-DIS05-15.2.13-1) in *Figure 2* and *Table 2* (where BKP3 = 3U backplane; DIS05 = distributed topology, 5 slots; 15-2-13 = location of more details in the specification; and-1 = speed of 3.125 Gbaud/s).

TABLE 2: BACKPLANE PROFILES BKP3-DIS05-15.2.13-n

Profile name	Mechanical		Slot profiles and section		Channel Gbaud rate
			VPX 1, 2, and 4	VPX 3 and 5	
	Pitch (in.)	RTM conn	Payload	Payload or peripheral	Data plane
BKP3-DIS05-15.2.13-1	1.0	VITA 46.10	SLT3-PAY-2F-14.2.7	SLT3-PER-1F-14.3.2	2.5
BKP3-DIS05-15.2.13-2	1.0	VITA 46.10	SLT3-PAY-2F-14.2.7	SLT3-PER-1F-14.3.2	5.0
BKP3-DIS05-15.2.13-3	1.0	VITA 46.10	SLT3-PAY-2F-14.2.7	SLT3-PER-1F-14.3.2	6.25

Figure 3 shows a photo of the backplane with the above configuration. The other options for the backplane size is 6U and the topology can be also be CEN for Centralized or HYB for Hybrid. Other standard speeds are 5.0 Gbaud/sec and 6.250 Gbaud/s. Note that the industry is already moving to 10 Gbaud/sec speeds and above. So, putting this all together, we can ensure the right types of signals/protocols are defined for a slot and which Slot Profiles can be accepted by the backplane.



OpenVPX added a couple of other minor changes to the backplane. This includes redefining two reserved P0/J0 signals Aux_Clk (+/-), redefining the Res_Bus signal to GDiscrete, and adding one P1/J1 single-ended utility signal of Maskable Reset. The Aux_Clk and GDiscrete pins were previously bussed anyway, so the change is negligible. The SysCon signal also became configurable with OpenVPX.

VPX, via the 46 specification, provided a new high-speed serial solution to embedded computing design. The specification provided vastly higher performance and reliability COTS capabilities to mil/aero and other applications. However, interoperability became a problem due to the lack of specifics in routing classifications and signal-type definitions. OpenVPX, via VITA 65 specification, provides profile definitions for the modules, slots, and backplanes so that systems will be interoperable.

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