Adding A GPS Chipset To Your Next Design Is Easy

Electronic Design

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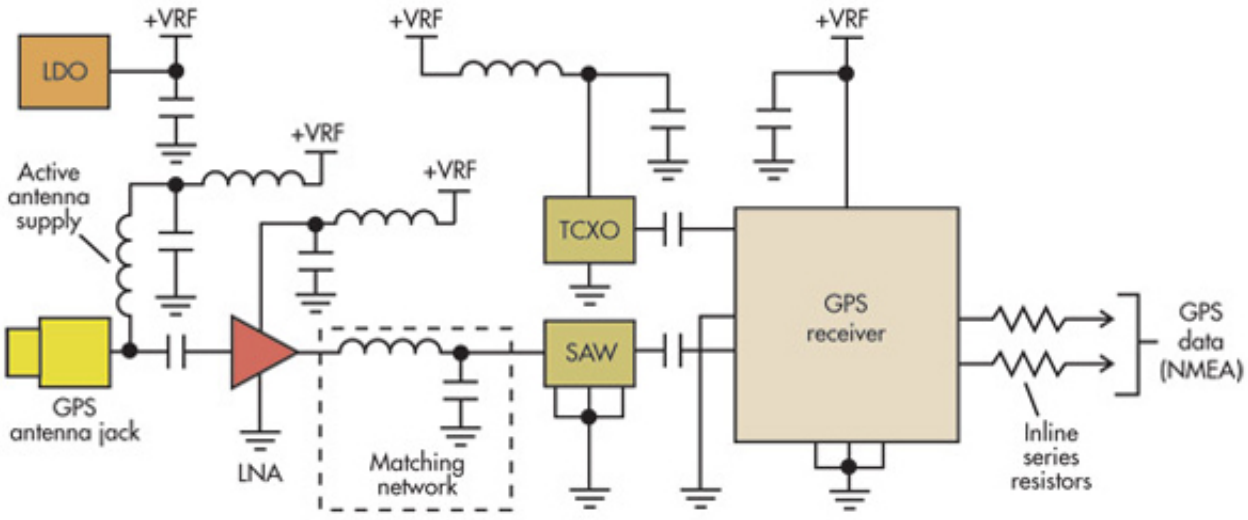

Fig 1. A typical GPS receiver includes several key components, including the RF input, the LNA, a SAW filter, a TCXO, and the GPS RF chip.

GPS modules and chipsets are being designed into many consumer and industrial devices, resulting in an increasing number of engineers being tasked with incorporating GPS subsystems into their designs. And while not all design engineers are going to have GPS design experience (or even RF design experience), several design rules will help average engineers successfully integrate a GPS receiver into their design.

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Of course, the first step in the process is choosing a GPS chipset or module. When considering GPS solutions, there will be a number of factors to consider before the design-in can start.

Can you afford a GPS simulator for testing and production?

Single-channel simulators cost between $10,000 and $15,000. If these costs cannot be accounted for in your product, then an already tested GPS module may be a better choice for your system. You may still need to design 50-Ω RF tracks (more on that later), but the performance of the module comes pre-tested and qualified, albeit at a higher BOM cost.

You may be tempted at this point to "throw an antenna out the window" or use a GPS repeater. Both options will likely result in poor test coverage. A GPS simulator is really your best option for production test.

What are the goals for the GPS antenna, active or passive?

"Active antennas" have a built-in low-noise amplifier (LNA) and will usually connect to your main printed-circuit board (PCB) through a coax cable (either inside your enclosure or outside), while passive antenna designs have no LNA in the antenna element and are commonly mounted directly onto the PCB.

"Passive antenna" designs are more complex and can be susceptible to noise coupling into the antenna ground plane if not correctly isolated from other noise-producing components on the PCB. Testing can also be complicated with passive antenna designs since an RF chamber, re-radiating antenna, and GPS simulator will need to be set up and calibrated for consistent test results.

What type of antenna element do you need? Patch, linear, chip, or something else?

Generally, patch antennas in the 15- to 25-mm size range with at least a 40-mm (on a side) ground plane will give the best performance in portable equipment, but this may be too large for your application. This could force you to look at smaller antenna topologies such as linear or chip antennas.

There's one thing to note when deciding between chip and patch antennas, though. Patch antennas will provide the best signal performance for their size, as they receive signals on all sides of the patch. Linear GPS antennas (chip or dipole) will generally only receive signals along one of their axes. This results in linear antenna designs being at least half as sensitive (i.e., around –3 dB) compared to patch antennas, and most will probably be around 25% as sensitive as a patch (or about –6 dB).

Some newer chip and folded-F designs show some promise in this area. However, it's best to evaluate your GPS sensitivity needs with an evaluation kit from your chosen GPS chipset or module manufacturer using various antenna topologies to determine what best fits your design requirements.

If antenna design is not your forte, consider using an active chip or patch antenna module such as those sold by Taoglas Limited. These units provide a tested antenna module while allowing the designer to implement a simple GPS simulator test interface through a U.FL style connector.

Whichever antenna design you choose, you also will need to evaluate the antenna to case spacing for antenna-detuning effects. The manufacturer can tune patch antennas to account for the detuning effects of a plastic case near the patch antenna, but this will likely add cost to your design. Another option is to choose a wider-bandwidth antenna, which usually means a taller antenna.

So you have finally decided to design-in a GPS chipset solution and have chosen an antenna topology. What's next? First, it may be helpful to have a basic knowledge of GPS signal strength. Signal-wise, the maximum signal

strength of a GPS transmission (at ground level) is around –160 dBW (or –130 dBm), which in most receiver designs is going to be about 20 dB below the receiver's RF noise floor.

Spectrum analyzers and other general RF equipment are not going to detect this signal. In fact, the GPS receiver RF front end will never have an analog signal that can be traced, probed, or captured. The only practical way to detect the presence of the GPS signal is through the correlation process of the GPS receiver itself. As a result, all GPS testing and performance metrics will involve signal data from the GPS receiver, which is an integral part of the test process.

Starting The Design

At this point, you probably have a reference design from your GPS chipset vendor, and you wish to copy its success. The first concept to ingrain in your mental toolbox of design rules is this: the GPS signal is *below* the noise floor! Repeat this over and over again.

A "quiet" design that passes the electromagnetic compatibility (EMC) tests may not be so quiet as far as the GPS receiver is concerned. The world is fraught with digital noise at this level, so the best design strategy at the start is "isolation." It won't guarantee a noise-free design, but it should give you a good start on getting there.

Figure 1 and Figure 2 detail a simplified GPS-receiver schematic and layout including an RF input (including an active antenna supply feed), an LNA, a set of matching components, a surface acoustic wave (SAW) filter, a dc-blocking capacitor, a temperature-controlled crystal oscillator (TCXO), and the GPS RF chip itself, all under the cover of an RF shield can (more on that later).

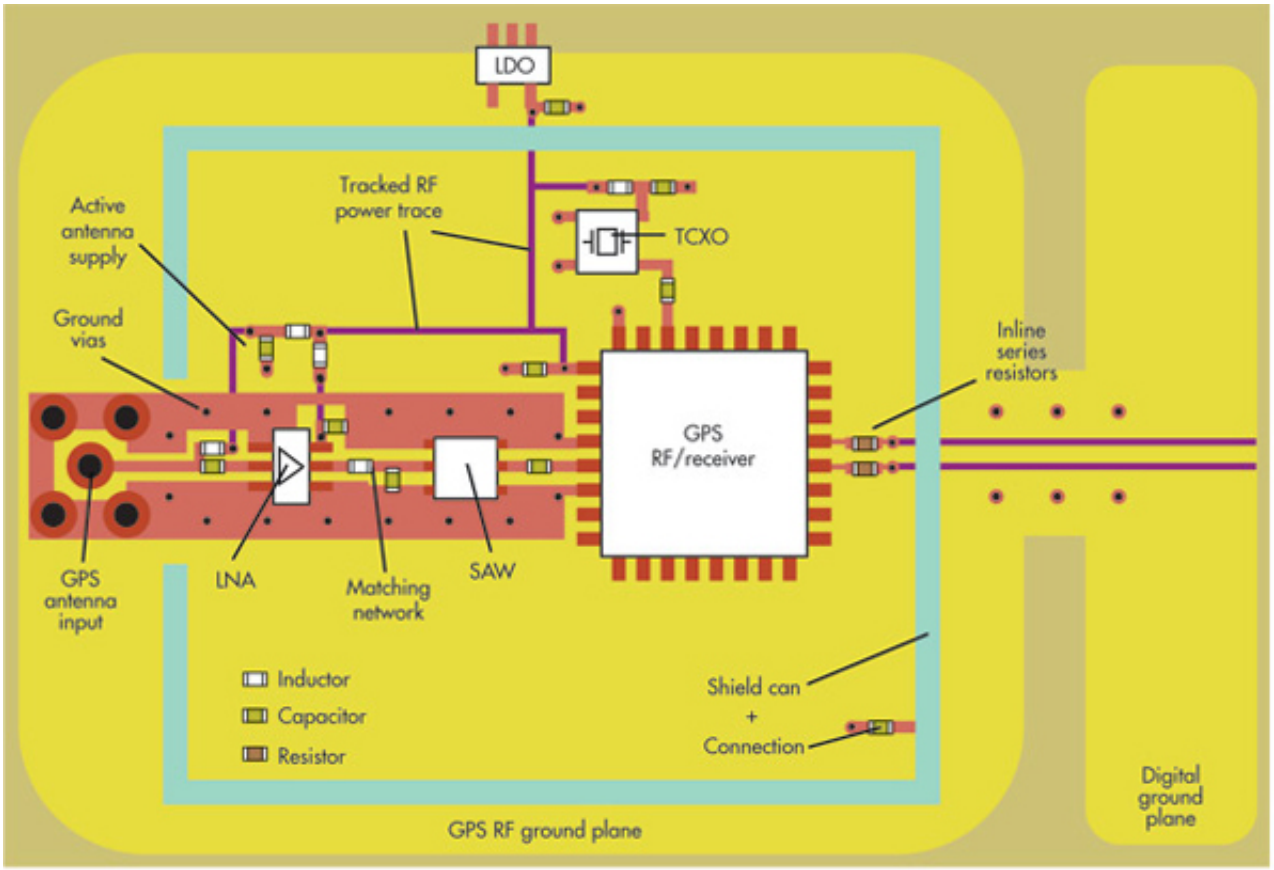


Fig 2. The key components of the GPS receiver should go under the shield can to isolate the TCXO from transient thermal conditions.

For the ground plane layout, you will want to isolate the GPS receiver section (or the GPS RF front end if it is a two-chip solution) to its own RF ground plane, which is connected to the digital section at a single point. This is also the preferred area to connect the clock and data lines. Then, you will need to control current flow into and out of the GPS section.

Usually, in-line resistors inserted in the clock and data paths can control the current flow. The inline resistors minimize the instantaneous current spikes that occur when the signals change state. Another design rule is to remember that the ground connection is a return path for the energy that is being transferred on the signal path. Ground paths should always be present in equal or greater measure to signal paths.

Also, you will need to track in the power supplies to the GPS section on individual traces (not on a power plane). The reason for this rule is that when power and ground planes are placed over each other, they make a plate capacitor with the PCB material acting as the dielectric.

Any noise on the power plane will be coupled directly into the ground plane with noisy results. You may also want to consider using this approach in the rest of your digital design section, as some of the digital noise may find its way up to the GPS RF section through the single-point ground connection.

Strip Line, Via, And Trace Impedance Control

After the component placement is done and your ground planes are defined and isolated, you will need to run your digital, RF, and ground-return traces. For RF signal paths, you will need to set the impedance at 50 Ω. Does this mean you need impedance-controlled PCBs? Not necessarily.

If your PCB manufacturer enables you to set the plane-to-plane spacing (or defines a layer spacing that they will guarantee on a lot-by-lot basis), you can control this yourself. Given an FR4-based PCB material, the necessary trace width can be shown as a function of layer spacing *(see the table)*.

PCB LAYER SPACING FOR 50-Ω IMPEDANCE

PCB layers + thickness	Layer spacing	50-Ω track width
Four layers, 0.062 in. total	0.02 in. or 20 mils	0.03 in. or 30 mils
Four layers, 0.030 in. total	0.01 in. or 10 mils	0.01 in. or 10 mils
Two layers, 0.062 in. total	0.062 in. or 62 mils	0.12 in. or 120 mils!
Two layers, 0.030 in. total	0.030 in. or 30 mils	0.05 in. or 50 mils!

These impedances were calculated using a “typical” Flame Retardant 4 (FR4) permittivity of 4.5. Or you can take the easy route and calculate this with the use of one of the many online impedance calculators, such as the one available at *www.eeweb.com/toolbox/microstrip-impedance*.

You will still need a PCB permittivity value to calculate a trace width. Since FR4 generally runs from about 4.3 to 4.7, a value of 4.5 will work in most cases, but you should verify this with your PCB manufacturer. Trace thickness will generally be about 35 µm for 1-oz copper and 17 µm for 0.5-oz copper (typical for inner layers).

When running your RF traces, you will also need to consider the effects that vias will have on the impedance of the trace. At GPS frequencies, each via acts as a small inductor, with the end result being that each via adds around 10 Ω of impedance to your trace. If you use two vias in an RF path (say, one down to an inner layer and then one up to a component pad), you have added 20 Ω of impedance mismatch.

To avoid this, keep all RF traces on the top layer of the PCB *(Fig. 2)*. RF grounds that are not directly tied into the top-layer ground return path will need multiple vias. (Remember, you reduce inductance when adding inductors in parallel.) Power grounds such as decoupling caps can be implemented with single vias, but decoupling components should be as close as possible to the component with a direct-connection, top-layer

trace if possible.

Another important note at this point is that it only takes a trace length of about 0.9 in. to make an FR4-based 0.25-wave antenna element (at GPS frequencies), so any long ground traces need to be "shorted" with vias every 0.2 in. or so to keep them from resonating at GPS frequencies. You should also try to place all components end to end and avoid track-stubs wherever possible.

Key Components

The LNA, which is the first stage in the GPS receiver, needs a low-noise power supply to properly function. The easiest way to guarantee low noise is to give the RF its own low-dropout regulator (LDO).

The noise rejection on most commonly available LDOs is in the neighborhood of 50 to 70 dB, and the price is generally under 30 cents in volume, so it's well worth the cost. You will also need to add some noise isolation (an inductor and cap) between the LNA and the RF supply if it is not already present in your reference design. This protects the LNA from VCO-induced (voltage-controlled oscillator) noise in the rest of the RF.

SAW filters are also necessary in most environments. Follow the matching components guidelines from the reference design, or ask for matching details from the SAW filter provider. Try to preserve the ground connections through the body of the SAW filter (i.e., don't break the ground underneath the SAW).

A TCXO is a requirement for fast time-to-first-fix (TTFF) and should have an initial tolerance of at least 2.5 ppm. For GPS operation, these oscillators need to be ultra-stable in the 1-Hz time domain—on the order of 1 ppb per second!

Since its short-term stability can be affected by rapid thermal change, the TCXO should be protected from rapidly changing thermal transients. (A shield can be beneficial here; see below.) To meet these requirements, you will need to work with a qualified GPS TCXO provider. A general-purpose TCXO will not do here. Various suppliers are in this market, including Rakon, Kyocera, and ECS.

A shield can, as mentioned above, is necessary for isolating the TCXO from transient thermal conditions. Heat-producing components such as voltage regulators and power transistors should be placed outside of the shield can. Noise-producing components such as switching regulators, high-speed oscillators (other than the GPS TCXO itself), and rapidly switching circuits also should be placed outside of the shield can and away from the RF section in general.

It's common in VHF and UHF RF shielding to connect all points of the shield can to the PCB's ground plane. This can be a mistake at GPS frequencies, since the open-air wavelengths of a GPS signal is so much shorter than UHF. Depending on the size of the shield can, if there is current flow across the can, the shield can will be able to resonate near GPS frequencies resulting in interference or de-tuning of the GPS RF.

The simple way to avoid this is to create a shield "ring" that connects to the shield can and then connect that ring to RF ground through an inductor at a single point. The inductor filters any EMI-induced (electromagnetic interference) current flow while the single-point connection prevents current flow across the shield can (and any resulting resonation).

Noise Control (Elsewhere In Your System)

Designing a clean GPS section is not enough if you happen to have noisy components elsewhere on the board. You will also need to look at the edge rates, clocks, and frequencies that are in use by other components. Certain frequencies just won't work with a GPS receiver on board.

Common interfering frequencies include 4 MHz, usually an IF interferer, and 19.2 MHz. (A multiple falls directly on 1575.42 MHz.) If you have a main-micro running off of a 19.2-MHz oscillator, see if you can change to 24, 25, or 26 MHz, which usually won't interfere. You can also run your main micro off of the GPS clock if it is a suitable frequency.

Lastly, you will need to look for resistor-cap transmission-line terminations, which puts a low-ohm resistor (<100 Ω) in series with a cap to ground to control impedance and reduce transients *(Fig. 3a)*.

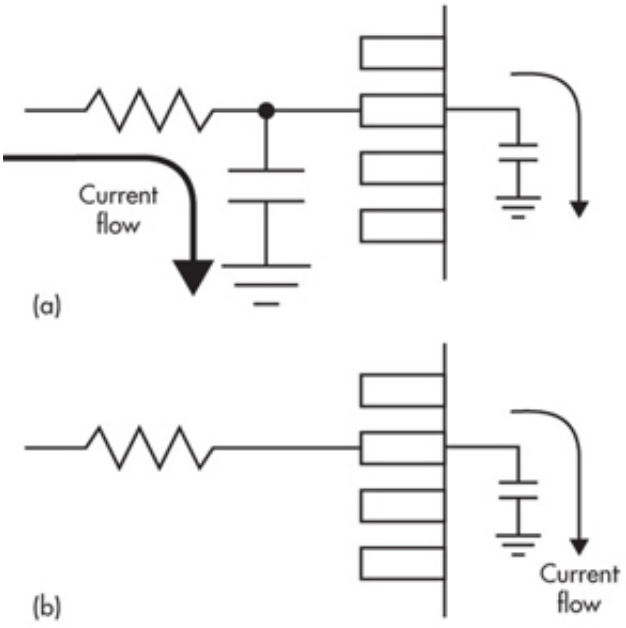
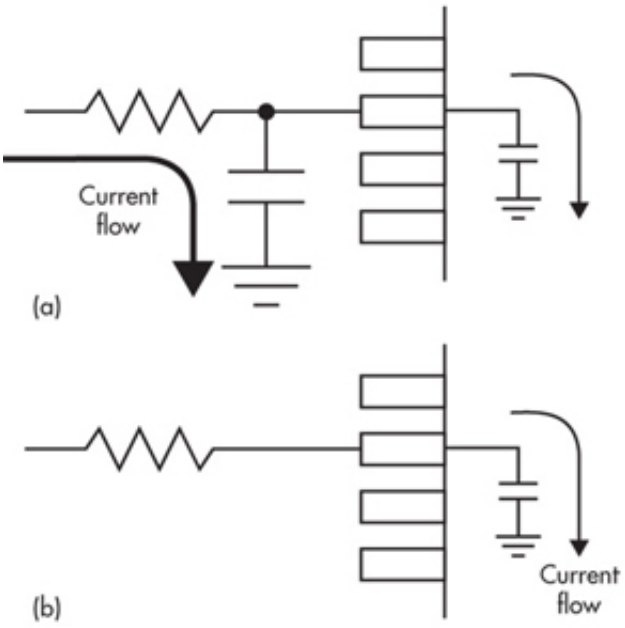


Fig 3. The resistor-cap transmission-line terminations put a low-ohm resistor in series with a cap to control impedance and reduce transients (a). A better approach calculates the capacitance of the inputs on the net in question and then inserts a resistor in series to set the edge rate (b).

The problem with this approach is that the switching energy is dumped through the capacitor directly into the ground plane. These current spikes produce noise on the ground plane and can set up interfering harmonics.

A better approach is to calculate the capacitance of the inputs on the net in question and then insert a resistor in series to set the edge rate *(Fig. 3b)*.



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To calculate the edge rate, you can use R-C charging curves. But to simplify things, I'll present an approximate equation for a 10%/90% switching point:

$R = 3t/C$

As an example, say we need a 10%/90% switching point with 10-ns rise/fall time for a clock line at 10 MHz (100-ns cycle) and a IC input load capacitance of 10 pF. Substituting values we have:

$R = 3t/C$

or:

$R = 3x10^{-8}/1x10^{-11}$

or: 3 kΩ

This may look to be too high a resistance if you're used to standard RC termination methods, but give it a try.

You'll have much quieter boards as a result! So in summary, follow and review these design rules and you'll have a good start on implementing a GPS design in your next project.

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