Fundamentals of Buck Converter Efficiency

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To illustrate the factors that play a role in a buck converter's efficiency, the Table below lists the equations used to *estimate* the most significant power losses. The parameters to minimize for high efficiency can be quickly determined utilizing these equations. The dominant losses in a buck converter design depend on the specific operating conditions of the circuit, and hence, it is important to perform the calculations below for your application. You can click on the table to enlarge it for easy viewing.

	Conduction Losses	Switching Losses
High-Side MOSFET	$P_{COND\_HS} = I_{OUT}^2 \times R_{DS(ON)} \times \frac{V_{OUT}}{V_{IN}}$	$P_{SW\_HS} = \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times (t_{RISE} + t_{FALL}) \times f_{SW}$
Low-Side MOSFET (Synchronous)	$P_{COND\_LS} = \left[I_{OUT}^2 \times R_{DS(ON)} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)\right] + \left[(t_{DT(R)} + t_{DT(F)}) \times V_{BD\_F} \times I_{OUT} \times f_{SW}\right]$	P_{SW_LS} : *negligible*
Power Diode (Non-synchronous)	$P_{COND\_D} = V_F \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$	P_{SW_D} : *negligible* Assuming a Schottky Diode
	DC Losses	**Core Losses**
Inductor	$P_{DC\_L} = I_{OUT}^2 \times DCR$	See Supplier Information or Reference 1

Other Supporting Equations

$$D = \frac{V_{OUT}}{V_{IN}} \qquad t_{RISE} = \frac{Q_{G(SW)}}{I_{DRIVER(RISE)}} \qquad t_{FALL} = \frac{Q_{G(SW)}}{I_{DRIVER(FALL)}} \qquad Q_{G(SW)} \approx Q_{GD} + \frac{Q_{GS}}{2} \qquad t_{DT(R)} + t_{DT(F)} \approx 2 \times t_{DELAY}$$

I_{OUT}	DC Output Current	$t_{DT(R)}$	Time period between when Q_{LS} turns off and Q_{HS} turns on. Also known as the dead time	$I_{DRIVER(RISE)}$	Controller gate drive current during turn on
$R_{DS(ON)}$	MOSFET drain-to-source resistance in the on-state	$t_{DT(F)}$	Time period between when Q_{HS} turns off and Q_{LS} turns on	$I_{DRIVER(FALL)}$	Controller gate drive current during turn off
V_{OUT}	DC Output Voltage	V_{BD_F}	Q_{LS} body diode forward voltage	Q_{GD}	MOSFET gate-to-drain charge
V_{IN}	DC Input Voltage	V_F	Power diode forward voltage	Q_{GS}	MOSFET gate-to-source charge
t_{RISE}	Duration of the turn-on transition	DCR	Inductor DC resistance	t_{DELAY}	Controller dead time delay
t_{FALL}	Duration of the turn-off transition	D	Duty Cycle		
f_{SW}	PWM Switching Frequency	$Q_{G(SW)}$	MOSFET gate charge during the switching period		

Efficiency Parameters

From these equations, the following parameters can be used to improve the efficiency of a buck converter. Keep in mind that typically the output voltage and current are fixed by the load requirement.

Parameters to Minimize for High Efficiency

Switching Frequency, f_{SW}

MOSFET
- On-resistance, $R_{DS(ON)}$
- Gate Charge, Q_G

Inductor
- DC resistance, DCR
- Core Losses

For Synchronous:
Low Side MOSFET
- Body Diode Forward Voltage, V_{BD_F}

For Non-synchronous:
Power Diode
- Forward Voltage, V_F

Switching Frequency (f_{SW})

Decreasing the switching frequency will decrease the losses in the MOSFETs, rectifier and the inductor core. Practical considerations usually limit the switching frequency. As the switching frequency decreases, the inductance and capacitance must increase in order to maintain an acceptable amount of inductor current ripple and output voltage ripple. As a result, the physical size of the inductors and capacitors will increase, and may not be acceptable in some applications.

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At low switching frequencies, the conduction losses will dominate and little is gained by decreasing the switching frequency any further. In the majority of point-of-load applications, an acceptable lower frequency range is approximately 150 to 350 kHz.

Switching frequencies much greater than 350 kHz are possible while maintaining good efficiency as long as care is taken in selecting MOSFETs. Today's MOSFETs allow for reasonable efficiencies at switching frequencies reaching 1.5 MHz without a substantial cost penalty.

High-Side MOSFET

Both conduction and switching losses can be significant in the high-side MOSFET. Conduction losses are proportional to the $R_{DS(ON)}$, whereas switching losses are proportional to the gate charge, Q_G, of the MOSFET. Unfortunately, for a given MOSFET fabrication process, low $R_{DS(ON)}$ devices will tend to have a higher gate charge and vice versa. Deciding which MOSFET parameter is best to optimize depends on the duty cycle and switching frequency. For low duty cycles (< 0.5), switching losses tend to dominate, especially at high frequencies. In this case, it is important to minimize the gate charge. For high duty cycles, conduction losses play a larger role, and it is important to minimize the $R_{DS(ON)}$.

Low-Side MOSFET

Unlike the high-side MOSFET, the voltage across the drain-to-source of the low-side MOSFET is much lower

during turn-on and turn-off transitions due to the conduction of its body diode during the dead time. As a result, switching losses in the low side are often negligible. This is fortunate since the calculations for the low-side switching losses are much more complex (see Reference 2). It is most beneficial to select a low-side MOSFET that has the lowest achievable $R_{DS(ON)}$. Low $R_{DS(ON)}$ MOSFETs require larger die area, and as result, can be expected to be in a larger IC package and be relatively more expensive.

To ensure the contribution of the body diode is minimal, a low forward voltage Schottky diode should be placed externally across Q_{LS} or select an integrated MOSFET + Schottky device.

Power Diode

The power lost in the diode is largely determined by the forward voltage, V_F. A Schottky diode should be used whenever possible since it has a very low forward voltage (~ 0.3V) and minimal reverse recovery time.

Synchronous versus Non-Synchronous

In most applications, especially those that operate at low duty cycles and near the full load current, a synchronous buck will be more efficient than a non-synchronous buck. Non-synchronous bucks can sometimes deliver a higher efficiency when operating at lighter loads or at very high duty cycles. For more details see Reference 3.

Inductor

Inductor power losses are mainly a result of the DC resistance of the winding, DCR, and hysteresis within the core magnetic material. To decrease the DC conduction losses for a given inductance, a larger diameter wire for the coil should be used. To minimize the core losses a lower switching frequency should be selected. Both of these will result in a physically larger inductor that may be more costly but will achieve better efficiency. For more details on inductor power losses see Reference 1.

To identify an inductor with a low DCR rating, look for one with a current specification that is higher than is required for the buck design.

Other Losses

The methods described thus far can provide large efficiency gains if appropriate design practices are utilized. There are many additional losses throughout a real switching buck converter circuit that can also be reduced with some detailed analysis. Reducing these may only provide little return; however, they should be considered if the operating conditions are atypical or to achieve maximum efficiency.

Additional Power Losses in a Buck Converter

● PCB trace copper losses ●Charging HS MOSFET's output capacitor

●Controller quiescent current ●Charging external Schottky diode's capacitance

●Gate drive losses ●Reverse recovery losses of body diode

●Input and output capacitor ESR losses

References

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3. Nowakowski, Rich and Tang, Ning. “Efficiency of Synchronous versus Nonsynchronous Buck Converters”, TI Analog Applications Journal, 4Q 2009.

4. Application Note 4266, “An Efficiency Primer for Switch-Mode, DC-DC Converter Power Supplies”, Maxim Integrated Products, Dec. 2008.

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