Q&A: Embedding FPGAs into Custom SoC Designs

Electronic Design
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FPGAs have proven to be extremely useful in building high-performance, custom designs that can be easily changed. It's possible to implement soft processor cores in most FPGAs, but hard-core processors are more efficient. It's not surprising that major FPGA vendors like Microsemi, Altera, and Xilinx have implemented FPGAs with hard-core CPUs *(see "FPGA Packs In Dual Cortex-A9 Micro")*.

So why not incorporate an FPGA into a custom system-on-chip (SoC)? That's the question Menta, a fabless semiconductor company, answers with its eFPGA.

I was able to talk with Jean-Louis Brelet, Director of Business Development for Menta, about the eFPGA and how it can be incorporated into custom silicon designs.

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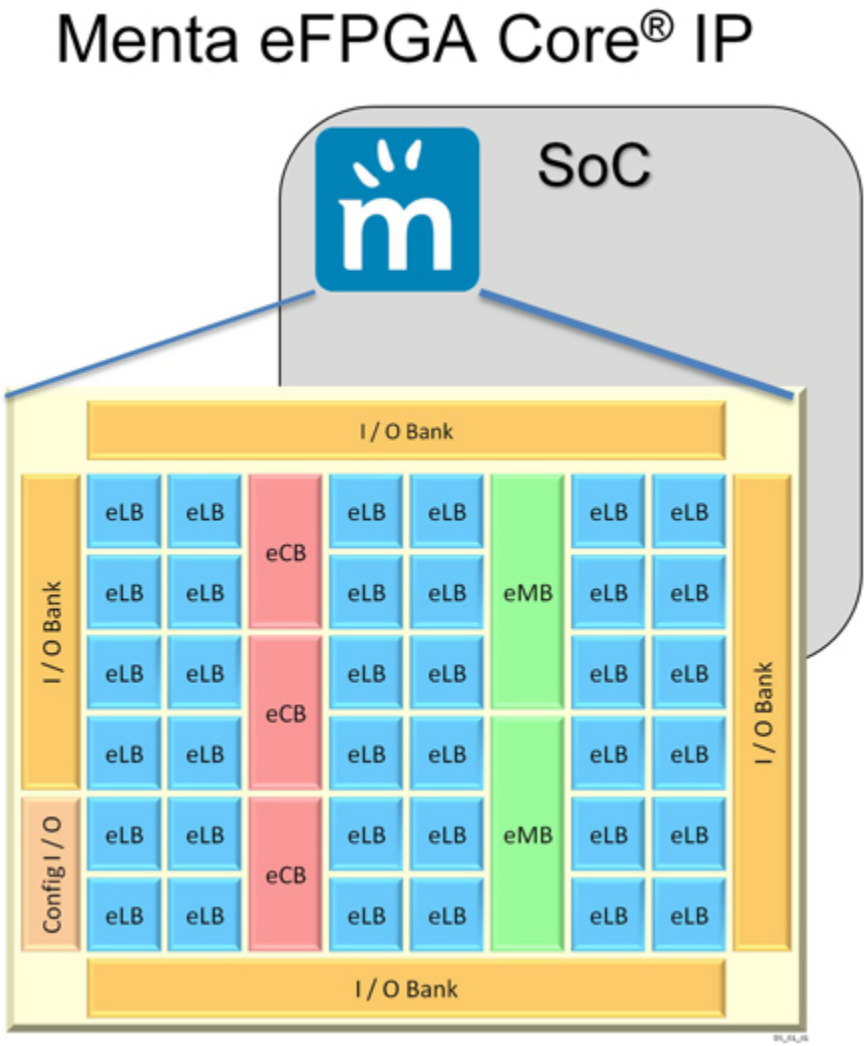
Wong: What is an eFPGA?

Brelet: An eFPGA is a field-programmable gate array that is embedded into a system-on-chip as an IP block *(Fig. 1)* alongside hardwired or fixed logic. The exact function of the eFPGA can be defined after fabrication. This allows semiconductor designers and equipment manufacturers to update the silicon at will post-production, thereby eliminating the cost and time associated with re-spinning silicon.



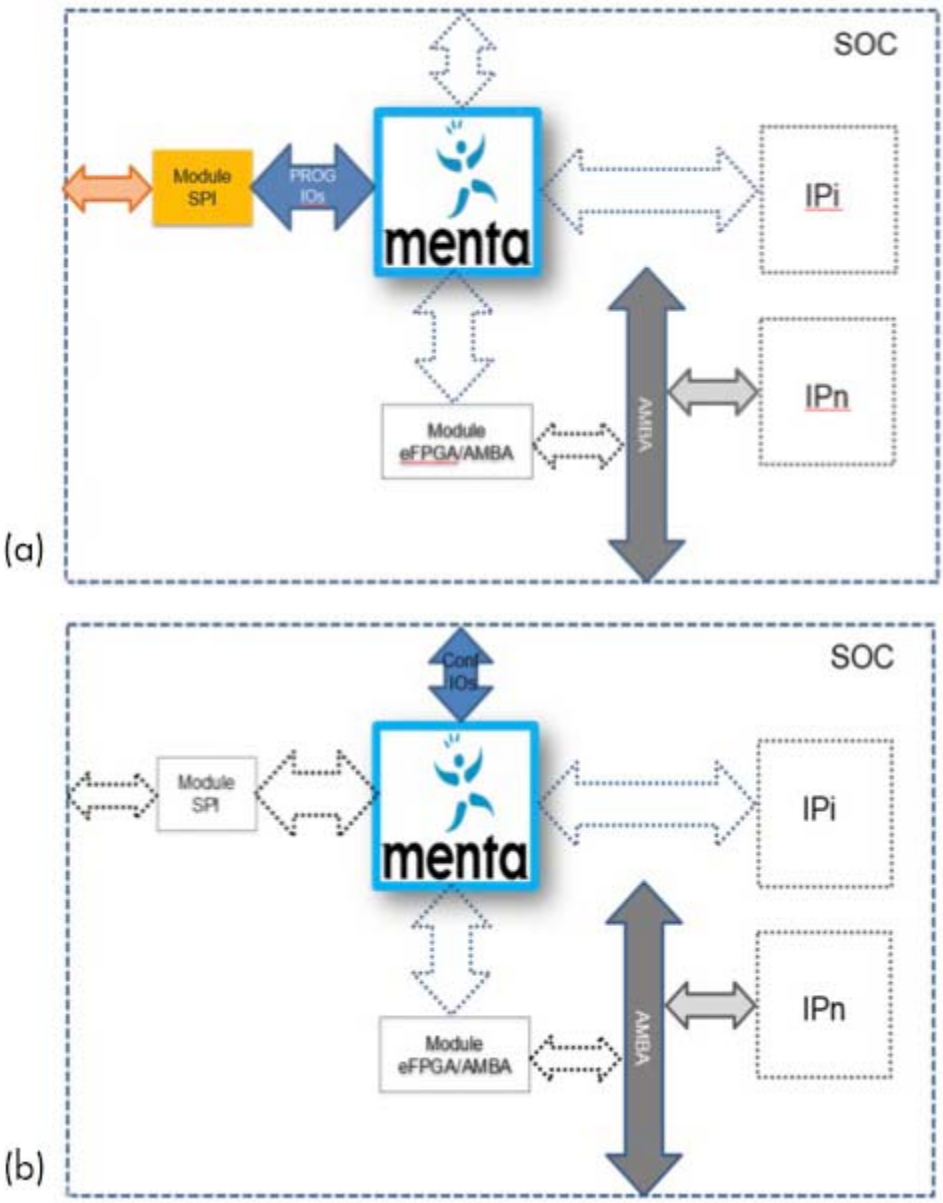
Wong: Why use an eFPGA if you are already designing a custom chip?

Brelet: Using an eFPGA offers programmability, allowing hardware modifications of a SoC over time. From a development standpoint, embedding programmability allows design reuse with the ability to quickly customize the same SoC to address different product, application, or market requirements. This saves cost and allows designers to get to market more quickly.

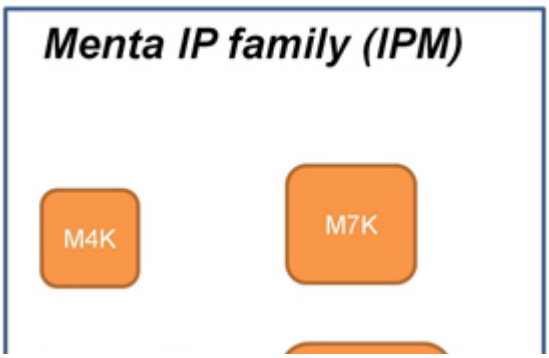
This approach also allows the device to be manufactured before all of the functions are finalized. For example, implementation of specific standards or security features (cryptographic protocols) in the eFPGA can be done post-production. Also along those lines, as protocols change over time, a designer can simply make updates to the SoC instead of starting from scratch.

Wong: How is the IP configured and how small/large can the eFPGA be?

Brelet: Designers can implement the eFPGA to support either on-chip programmability or off-chip programmability. For off-chip programmability, a serial interface with SPI protocol can be used *(Fig. 2a)*. Or, a parallel interface can be used to reduce configuration time, although this increases the number of needed pads *(Fig. 2b)*. On-chip programming could be made either directly or via a bus.



In theory, the size of an eFPGA can be as small or large as needed. However, choosing a block that is too small or too large may compromise capability or performance. Menta's new family of IP cores *(Fig. 3)* includes six off-the-shelf eFPGA options that have from 4k-60k equivalent ASIC gates, plus DSP blocks. The IP cores are delivered as hard macros with optimized array sizes for the embedded logic blocks (eLBs), embedded custom blocks (eCBs), and embedded memory blocks (eMBs), each of which are customizable in type, number, and size to address various markets and applications. Custom sizes can be developed as well.



Wong: What types of tools are available to program the eFPGA?

Brelet: Menta has developed its own programming tool called Origami programmer. This tool supports design from HDL to bitstream with synthesis, mapping, and place and route. The Origami tool chain, includes synthesis to allow RTL applications in VHDL, Verilog, or SystemVerilog, as well as new SDC support for application design constraints. Additionally, new timing-analysis tools enhance engineer

experience and facilitate designs.

Wong: How is the eFPGA configured and can it be programmed by an on-chip processor?

Brelet: As referenced in question 2, an on-chip processor can be used for programming. In this configuration, the processor can interface to the eFPGA either directly or via bus, such as an AMBA interface.

Wong: What are some of the applications areas for eFPGAs?

Brelet: eFPGAs are particularly well-suited for applications requiring parallel or co-processing, such as rad-hard solutions in aerospace and defense systems, or video processing. In addition, the ability to make updates to the silicon post-production or in the field make eFPGAs ideal for SOCs used for encryption or standards-compliant systems in automotive, industrial, or consumer applications.

Wong: Can you tell us more about Menta?

Brelet: Menta is a privately held company based in Montpellier, France. The company provides both custom and off-the-shelf eFPGA technology for system-on-chip, ASIC, or system-in-package (SiP) designs. Our programmable logic is based on scalable, customizable, and easily programmable architecture created to enable flexibility in customization for next-generation ASIC design.

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