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Q&A: A New Extraction Architecture Takes on Advanced-IC Challenges

Electronic Design
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Advanced IC processes require orders of magnitude improvements in extraction tools to meet the latest performance and accuracy demands. I talked with Mentor Graphics' Carey Robertson, Director of Product Marketing, LVS and Extraction about the new Calibre xACT product.

Wong: What product are you announcing?

Robertson: We've developed a new extraction product, called Calibre xACT, for IC designers working at advanced nodes. It's based on a new architecture that incorporates multiple extraction technologies to make it very fast, accurate and flexible *(Fig. 1)*.

Wong: What type of developers will want to use Calibre xACT?

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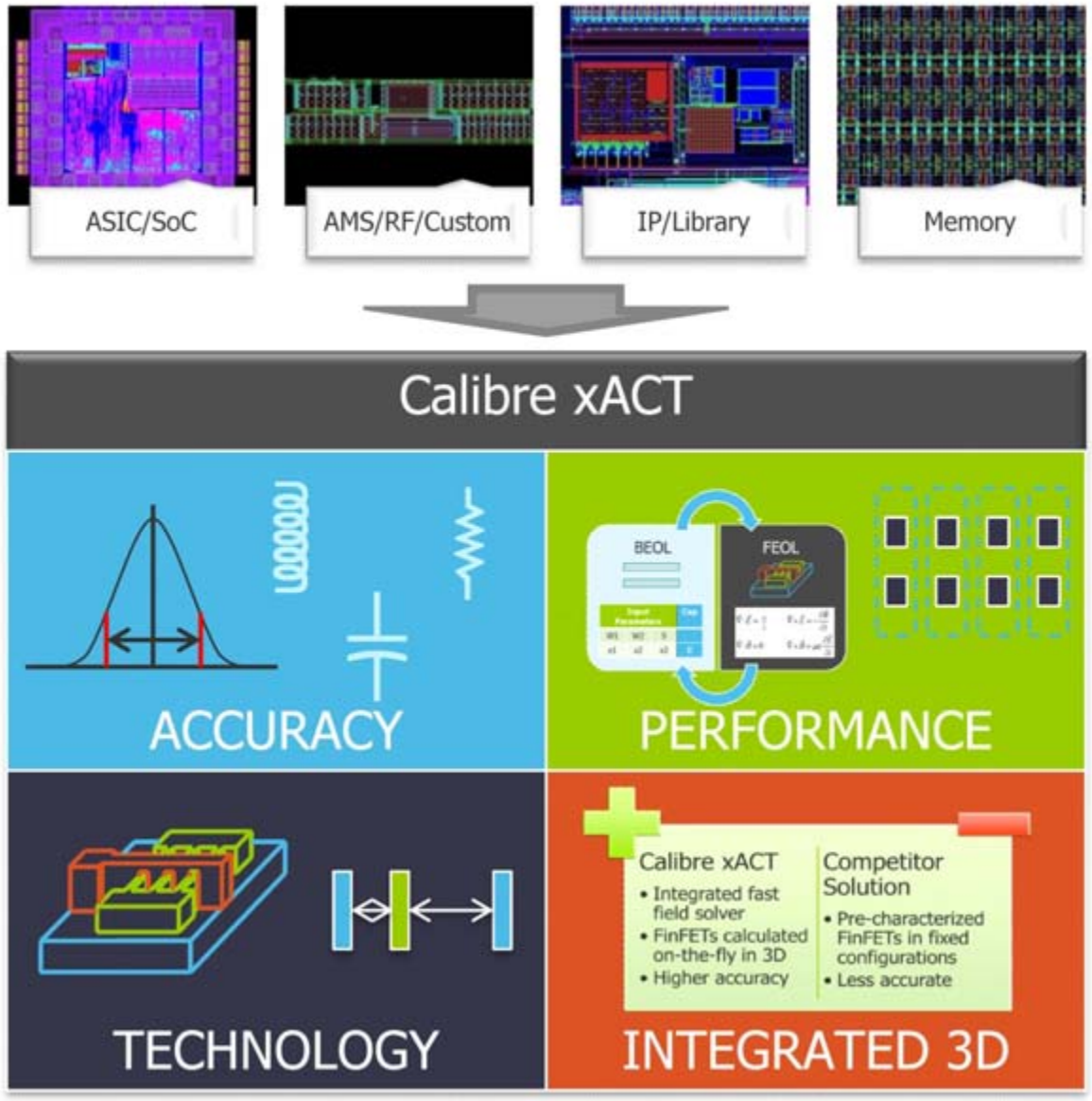
Robertson: IC designers need to extract the detailed electrical properties of an IC after it has been committed to a specific physical layout so that the device can be simulated to ensure it functions properly and meets critical performance requirements. We've created this new technology for IC design teams working at advanced IC process nodes on digital, custom, or analog ICs; cell libraries; or large mixed-signal SoCs.



Wong: What has changed in the market that requires tools like Calibre xACT?

Robertson: Newer process technologies are creating a lot of challenges for IC designers in the area of extraction. Beyond the usual scaling, which means exponentially more devices and interconnects, new nodes require higher accuracy, and FinFET devices add much more complexity to the extraction task. As a result, it is becoming very difficult for designers to get the extraction accuracy they need while maintaining the desired turnaround time.

Wong: What is the significance of this product?

Robertson: Calibre xACT provides IC designers with a combination of characteristics that are critical to success at advanced nodes. This includes reference-quality accuracy and repeatability, the ability to handle FinFET devices, quick turnaround time, and efficient scaling across many CPUs.

In addition to the need for increased accuracy and performance, versatility was a specific design goal because designers don't want to waste time dealing with multiple tools or reconfiguring tools to address their different extraction needs. Calibre xACT has the ability to automatically employ the optimum extraction technology for the application without complicated user setup tasks. For example, Calibre xACT handles the high-accuracy

uirements of FinFETs by automatically extracting with more precision in areas around devices where higher uracy is required, while using different techniques that provide the required accuracy and faster execution for upper metal layers. It can also optimize for individual cell library blocks, analog circuits, and full-chip digital extraction.

Wong: What challenges is Calibre xACT designed to address?

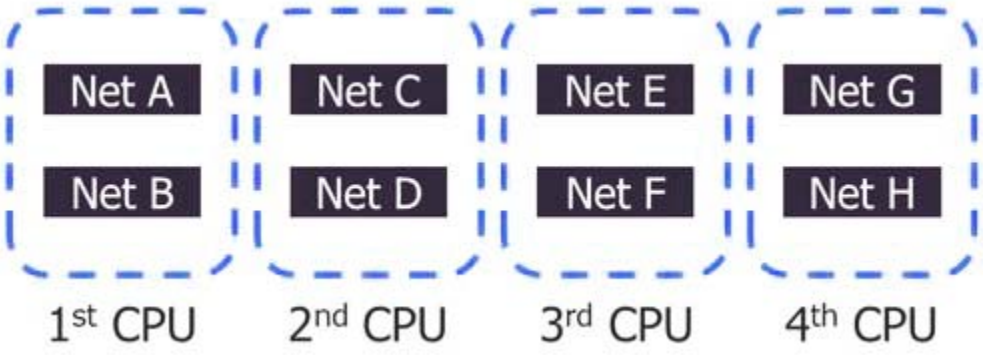
Robertson: Besides the accuracy and performance requirements I've already mentioned, static timing analysis is a significant bottleneck for tapeout of digital designs. With the expanding combinations of process and temperature variability that must be checked to ensure that ICs meet their target specifications, designers need to perform extraction for many more corners.

Double pattering exacerbates the problem because any misalignment of masks during manufacturing impacts the predictability of parasitic capacitance by increasing or decreasing the distance between features on multi-patterning layers. Consequently, designers need to characterize potential misalignment by performing simulations with multi-patterning corners. In practice this often means a combination of more than 10 process, temperature, and double-patterning (DP) corners.

The time spent on a big, full-chip design to extract all of the necessary corners could easily exceed an overnight run with traditional tools. Designers are often forced to limit their timing analysis runs to a few well-chosen corners, increasing the risk of missing a critical corner combination.

So we built in the ability to perform simultaneous multi-corner processing, which enables designers to generate additional netlists and validate their assumptions about corner scaling, with minimal execution time overhead. We use a technique that provides stable, deterministic results with only a 15% to 20% runtime increase for each additional corner, and no loss in accuracy. We specifically rejected stochastic (Monte Carlo) methods because they are slow and suffer from accuracy drift between multi-corner and single-corner results. Our goal was to make it possible to turn around multi-million-instance full chip designs with multiple-process, double-patterning, and temperature corners in a single workday.

Wong: What does this product do that is new or unique?



Robertson: Calibre xACT features a massively parallel architecture and unique computation techniques to achieve nearly ideal linear scaling. Rather than the typical tiling method, which breaks up nets into many pieces that are processed separately, our product keeps each net intact and processes each entire net on a dedicated CPU. This "net-based parallelism" approach eliminates boundary and halo effects on accuracy, and provides better scalability than tiling, especially on symmetric-multiprocessing (SMP) machines *(Fig. 2)*. Net-based parallelism also eliminates variance in the accuracy of results that occurs with tiling when the number of CPUs changes.

ng: What is Calibre xACT's performance relative to competing tools?

Robertson: Working with our customers has shown that we can perform extraction about three times faster than other extraction tools while delivering equivalent or better accuracy. That's about four to eight million nets per hour using eight CPUs. The great thing is that the tool scales nearly linearly, so users can get better turnaround time by provisioning more CPUs.

Wong: How accurate is Calibre xACT?

Robertson: Our product is delivering the accuracy required by the foundries themselves. In fact, our tool compares favorably to the reference field-solver tools the foundries use to qualify their processes.

Wong: How were you able to achieve these improvements?

Robertson: Traditionally, fast production extraction tools have used a simple table-lookup approach to determining the parasitics associated with physical transistors and interconnects. Such an approach provides an approximation to the actual parasitic values, depending on the accuracy of the parameterized model. In contrast, a field solver actually solves Maxwell's differential field equations in three dimensions to determine parasitics value based on the actual physics of the layout shapes. Consequently, field solvers are inherently very accurate, but they are usually very slow.

One innovation in our product is the computational methods used in our field solver, which are both inherently efficient and very scalable across many CPUs. This is one reason why Calibre xACT can be both fast and accurate.

Adding to this fundamental advantage, we built our tool with intelligence to know when to switch between field solver and other techniques to achieve the required accuracy for different extraction tasks, while delivering the best overall performance.

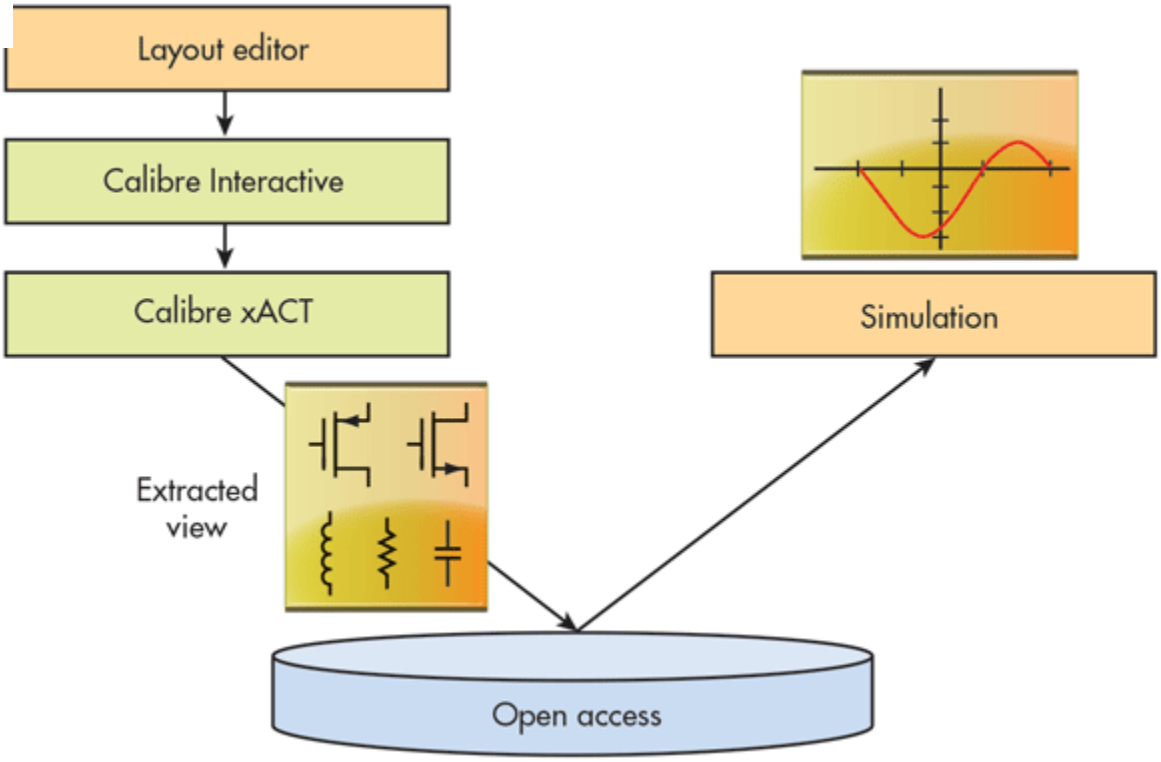
Wong: What is the development history of this product? Does it incorporate IP from non-Mentor sources?

Robertson: In 2008, we purchased a company called Pextra. That acquisition brought over the core field-solver technology leveraged by Calibre xACT. Also, the Olympus acquisition brought technologies for table-based and multi-corner methodologies that we also leverage for sign-off extraction. That being said, the technology needed to be integrated into the overall Calibre platform. We also needed to enhance the accuracy to meet foundry criteria, as well as develop the netlisting features, interfaces, etc., to allow the new technology to be used within Calibre and with design environments from both Mentor and third-party providers.

Wong: What processes can it be used with? Which foundries? Which design tools?

Robertson: Because of its flexibility, Calibre xACT can be used for a wide variety of extraction applications, including digital, analog, mixed-signal, and custom designs. While it addresses the critical needs of advanced nodes, especially at 16 nm and beyond, it is also suitable for established nodes. This means that designers can standardize on one extraction tool that uses foundry-qualified rule decks and reduce the overhead of dealing with multiple tools, or reconfiguring tools for different extraction tasks.

Wong: How does this product relate to other Mentor products?



Robertson: Calibre xACT is fully integrated with the Calibre platform, uses the Calibre syntax, works with the Calibre viewing environment, and shares the same internal data formats *(Fig. 3)*. Designers working with a Calibre verification flow will have no difficulty adopting this product. It is also interoperable with third-party design and simulation tools, using standard data-exchange formats so that it can fit in virtually any overall design flow.

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