Avoid Clipping in Emitter Follower with AC-Coupled Resistive Load

Electronic Design
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An engineer asked me for help when he encountered what appeared to be strange phenomenon while testing a prototype circuit in the system. He saw “mysterious” clipping distortion of the signal at the output of his emitter follower. He told me that he checked this follower with a much-heavier (smaller-value) resistive load than the actual load, but did not see any visible distortions. However, when he connected his prototyping board to the system, there was significant clipping of the signal at the bottom.

Looking at the schematic, I saw that the resistive input of the next device is decoupled from his follower by a large capacitor. I explained to him the reason for the problem. I also realized that, unlike with a resistive load when the possibility of clipping is fairly obvious, the problem with a capacitively coupled resistive load can be easily overlooked during the design.

A one-transistor emitter follower can source as much current to the load as the load needs, within its transistor’s limits. However, the transistor cannot sink current. This may cause clipping distortions of the output signal when the follower is ac-coupled to a resistive load, for reasons which are sometimes not obvious.

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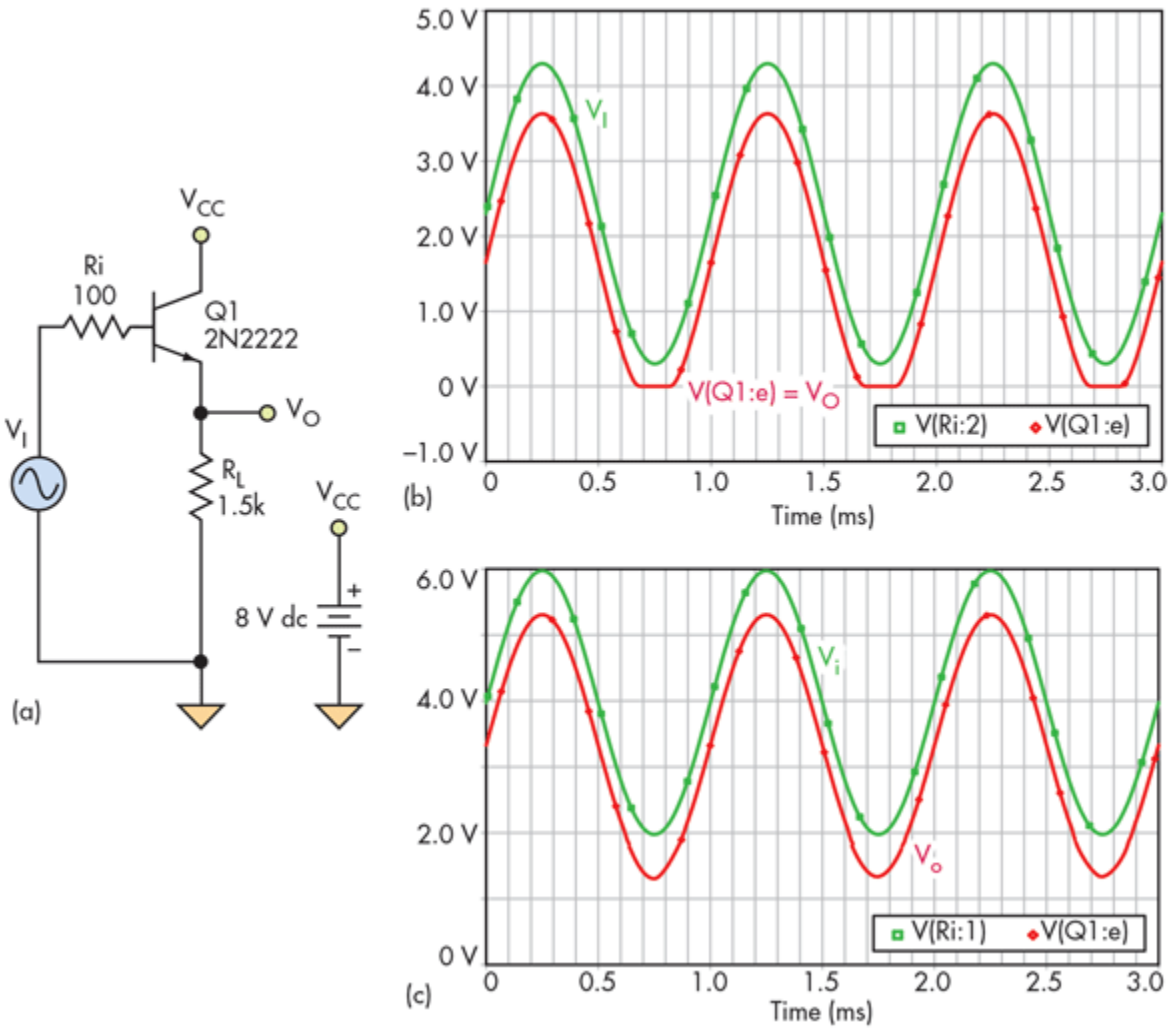
First, look at the simple NPN emitter follower *(Fig. 1a)* and its possible obvious clipping distortions. Positive clipping to V_{CC} on the output will occur if a large input signal exceeds V_{CC} by about 0.7 V, turning on the base-collector junction of the transistor Q1 (here, a common 2N2222). That junction works like a diode above the clipping point, shunting the input signal to V_{CC}. If this diode's current is not limited by an appropriate value of input resistor R_I, the transistor may be damaged.



Negative clipping occurs during the negative swing of the input signal if the input level at the base of the transistor becomes less than about 0.7 V (the V_{BE} of the transistor). In this case, the base-emitter junction of the transistor becomes reverse-biased, its emitter current (I_E) drops down to zero, and the transistor turns off. This causes clipping of the output signal to zero at its bottom until the input signal returns the transistor to the normal mode.

Close to the clipping point, emitter current I_E is low, and the follower increases its total harmonic distortion (THD) level. In the case of a sinusoidal input signal, to prevent this obvious clipping:

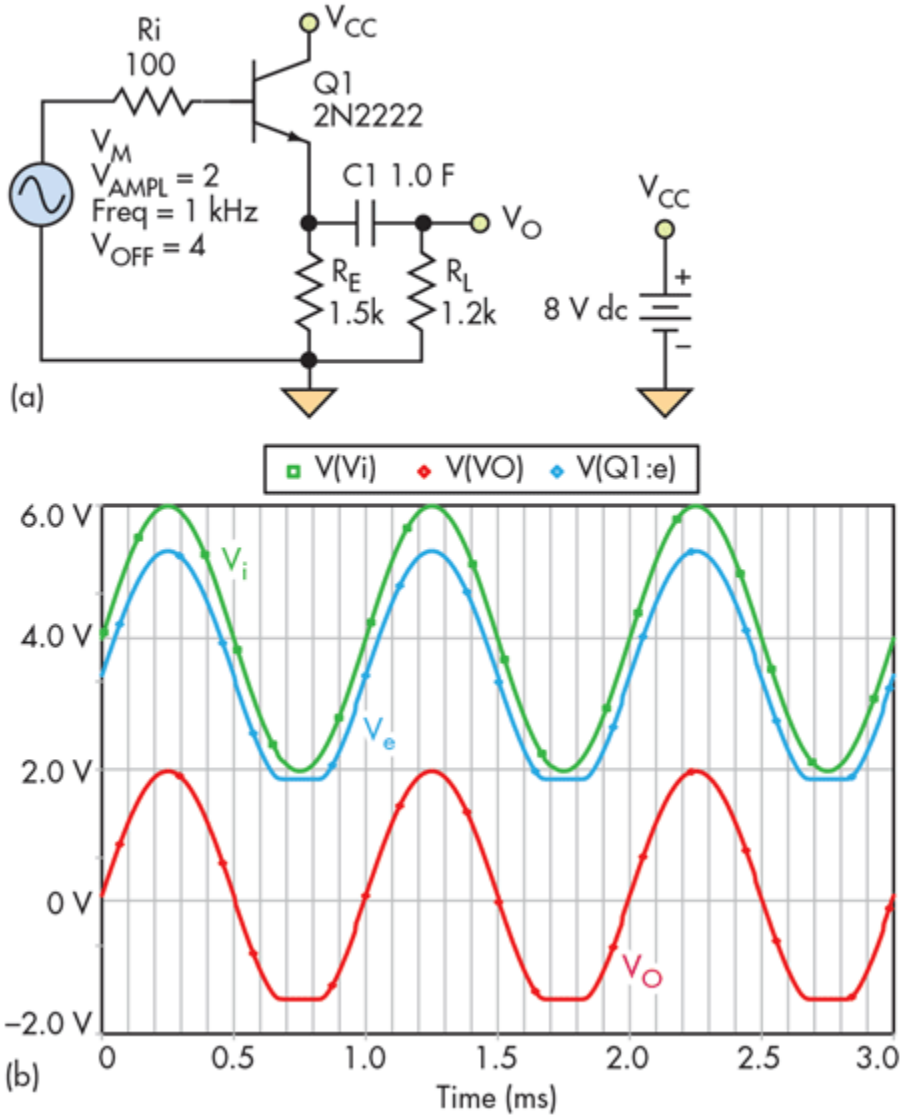
$$V_{OFF} - V_{AMPL} - V_{BE} > 0 \quad (1)$$

where V_{AMPL} is the peak amplitude and V_{OFF} is the dc offset voltage of the sine-wave input source.

The described clipping is illustrated using PSpice transient analysis of the circuit, with the ac input source set for V_{AMPL} = 2 V, V_{OFF} = 2.3 V and frequency of 1 kHz. In this case, V_{I_MIN} = 0.3 V and the transient analysis shows a clipping at the bottom of the output signal *(Fig. 1b)*.

Figure 1c shows results of the same circuit simulation with V_{OFF} = 4 V, which gives a 1.3-V margin above the clipping level. Now the transient analysis doesn't show clipping and other noticeable distortions of the output signal. Also, the Fourier analysis in the simulation profile shows THD of 0.143% in the output file.

reasing the follower's load produces a similar result. For example, even with R_E = 0.5 kΩ in the circuit of ure 2a (which is one third of the R_E used in the simulation), there aren't any noticeable changes in the graph and only slightly increases of THD to 0.145% from 0.143%.



Next, connect the ac-coupled load resistor R_L to the follower. The value of the decoupling capacitor C1 is chosen as large enough (1.0 F) so as to not contribute to possible distortions of the output signal at the end of the transient process. At first glance, you would expect the same result of the simulation as for the circuit in Figure 1, but without a dc component on R_L. However, the transient analysis *(Fig. 2b)* shows a significant clipping of the output signal and on the emitter of the transistor.

There's a simple explanation for this non- obvious result. In the steady state, C1 is charged to the dc level of Q1's emitter. During the positive half-cycle of V_{IN}, Q1's emitter current splits and goes to R_E and R_L (I_{RE} and I_{RL}, respectively). The maximum level of the emitter current I_{E_MAX} is:

$$I_{E\_MAX} = [(V_{AMPL} + V_{OFF} - V_{BE})/R_E] + (V_{AMPL}/R_L)$$

However, during the negative half-cycle of V_{IN}, while I_{RE} is still directed out of transistor Q1, thus decreasing its value, I_{RL} is directed back to Q1 and is subtracted from I_{Re}.

$_{MIN} = [(V_{OFF} - V_{AMPL} - V_{BE})/R_E] - (V_{AMPL}/R_L)$

If the result of this subtraction is negative, I_{E_MIN} drops to zero and the output signal suffers from clipping.

The reason I_{RL} is directed back to Q1 also isn't obvious. In the steady state, C1 is fully charged. The dc voltage on its left side is V_E, which is higher than the absolute voltage at minimum AC signal (V_{AC_AMPL} = 2 V) and in this case is equivalent to 4 – 0.7 = 3.3 V. The capacitor's dc level on the right side is zero.

Consequently, during the negative cycle of the ac signal, the voltage across R_E follows the negative wave of the input signal, but is always positive because of the bias. The R_E component in the combined current equals the voltage at the emitter of Q1/R_E > 0. Output voltage V_O on the top of R_L also follows the negative wave of the input signal, but it has zero dc bias. It's also negative for the negative wave. In this region, it changes from zero to negative V_{AMPL}, which causes the current through R_L to go in the opposite direction. I_{RL} is always less than 0.

To prevent the clipping problem, I_{E_MIN} should be always greater than zero:

$$I_{E\_MIN} = [(V_{OFF} - V_{AMPL} - 0.7)/R_E] - (V_{AMPL}/R_L) > 0$$

or

$$[(V_{OFF} - V_{AMPL} - 0.7)/R_E] > V_{AMPL}/R_L \quad (2)$$

Thus, to avoid clipping in the one-transistor emitter follower with an ac-coupled resistive load, the three variables of Equation 2 should comply with the following constraints:

$$V_{AMPL\_MAX} = (V_{OFF} - 0.7) \times [R_L/(R_L + R_E)]$$

or

$$V_{OFF\_MIN} = V_{AMPL}[(R_E/R_L) + 1] + 0.7$$

or

$$R_{L\_MIN} = [V_{AMPL}/(V_{OFF} - V_{AMPL} - 0.7)] \times R_E$$

and also, from Equation 1:

$$V_{OFF} - V_{AMPL} - 0.7 > 0.$$

References:

1. Alan B. Grebene, *Bipolar and MOS analog integrated circuit design*, Wiley - Interscience Publications, John Wiley & Sons.

2. Douglas Self, *Small Signal Audio Design*, Focal Press, 2010.

3. P. Horwitz, Winfield Hill; *The Art of Electronics*, Second Edition, Cambridge University Press, 1989.

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