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FRAMs Fit Wearable Electronics Like a Glove

Electronic Design
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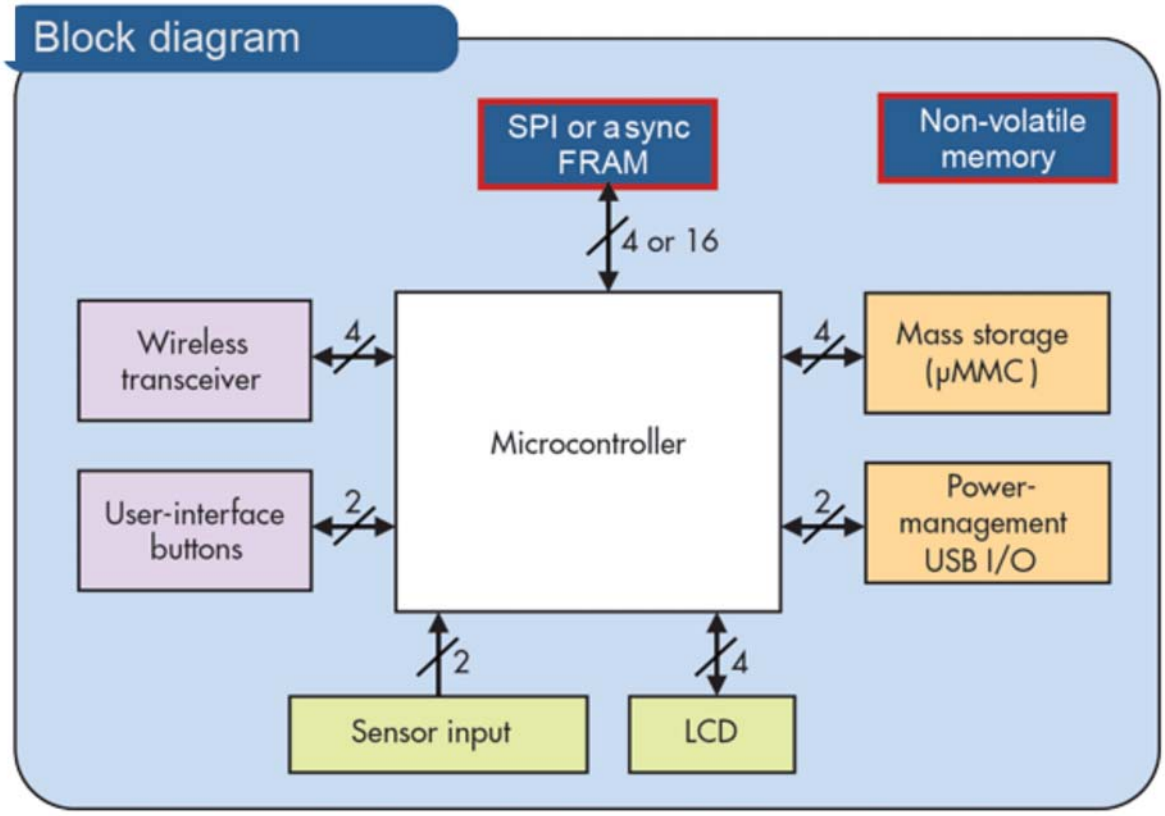
Ferroelectric-RAM (FRAM) memory is widely used in industrial control systems, industrial automation, mission-critical space applications, high-reliability military, and various automotive applications. The characteristics of FRAM that suit it for these applications also make FRAM a viable technology for wearable applications because of additional inherent attributes—low power and high endurance *(Fig. 1)*.

A major consideration for electronic wearable designs revolves around reducing total power consumption while increasing reliability. Designers must add functionality while simultaneously shrinking the system's power budget to achieve longer battery life. At the same time, though, embedded software is becoming larger and more complex, requiring more memory and thus further stressing the power budget.

Most of today's MCUs come equipped with two common types of memories: flash and SRAM. Flash is relatively slow and supports a limited number of write cycles. However, it's non-volatile and therefore is used to hold slow-changing data, such as application code. By comparison, SRAM is fast and has unlimited write cycle endurance. Its volatile nature means it can only hold temporary data.

Choosing an MCU can become complex when trying to accurately determine how little flash and SRAM will be required for an application. As system complexity increases and designers need to introduce external memory, often the first option that comes to mind is to add more flash or an EEPROM and, in certain rare instances, external SRAM.



Wearable-Design Considerations

Energy consumption, form factor, high endurance, and cost are key design parameters:

• High demand for data assimilation drives demand for memories.

• Memories increasingly impact component selection and bill of materials (BOM).

• Saving battery life and reducing recharge times are now critical differentiating parameters in the market.

Typically, as a design becomes more complex through high code complexity and execution of multiple mathematical functions, designers may look at augmenting on-chip resources with an external memory. A low-power external parallel-interface memory would be the first logical option, typically a SRAM-type memory with extremely low active currents and, ideally, zero standby current *(Table 1)*.

TABLE 1: PARALLEL VOLATILE/NON-VOLATILE MEMORY COMPARISON

Features	Cypress 4-Mb FRAM	4-Mb MRAM	4-Mb SRAM	4-Mb NOR flash
Operating voltage	2.0 to 3.6 V	2.7 to 3.6 V	2.5 to 3.6 V	2.7 to 3.6 V
Access speed	110 ns	35 ns	35 ns	45 ns
Energy (µJ)—full chip write	699	4634	585	2,831,798
Bandwidth (KB/s)	9000	28,000	28,000	5
Write endurance (cycles)	1014	105	Unlimited	105
Lifetime at 5-ms write frequency	15,855 years	Unlimited	Unlimited	8.3 minutes
Number of writes with 3-V, 220-mAh battery	3,398,895	512,695	4,060,547	839
Non-volatile retention	100 years	20 years	0	20 years
Active write current	12 mA at 110 ns	165 mA at 35 ns	25 mA at 35 ns	20 mA at 45 ns

A parallel-interface FRAM could also be a candidate for this application. FRAM has densities up to 4 Mb and offers high-speed performance (90-ns access time) with very low active write and read currents. Since FRAMs are inherently non-volatile, they can be power-gated (off) when not in use or when the MCU goes into sleep mode.

TABLE 2: SERIAL NON-VOLATILE MEMORY COMPARISON

Features	Cypress 2-Mb FRAM	2-Mb EEPROM	2-Mb NOR flash	4-Mb MRAM
Operating voltage	2.0 to 3.6 V	1.8 to 5.5 V	2.7 to 3.6 V	3.0 to 3.6 V
SPI speed	40 MHz	5 MHz	75 MHz	50 MHz
Energy (µJ)—1-byte write	314	63,996	10,611,178	6606
Bandwidth (KB/s)	5000	25	11	5000
Write endurance (cycles)	1014	1.2 x106	105	Unlimited
Lifetime at 5-ms write frequency	15,855 years	100 minutes	8.3 minutes	Unlimited
Number of writes with 3-V, 220-mAh battery	7,552,985	37,127	2,239	359,666
Non-volatile retention	100 years	100 years	20 years	20 years
Active write current	3 mA at 40 MHz	3 mA at 5 MHz	15 mA at 75 MHz	46.5 mA at 50 MHz

imilar problem arises for data storage, typically implemented in a serial flash *(Table 2)*. Flash is the prevalent rage memory, mainly attributed to the low cost per megabit and larger densities available. However, flash has a major drawback in terms of energy consumption when writing—it drains batteries faster. Many developers try to partition flash and use an EEPROM that consumes less energy (i.e., write infrequently to flash and use EEPROM as a front-end for heavy writes). EEPROM standby and active modes consume lower currents than flash.

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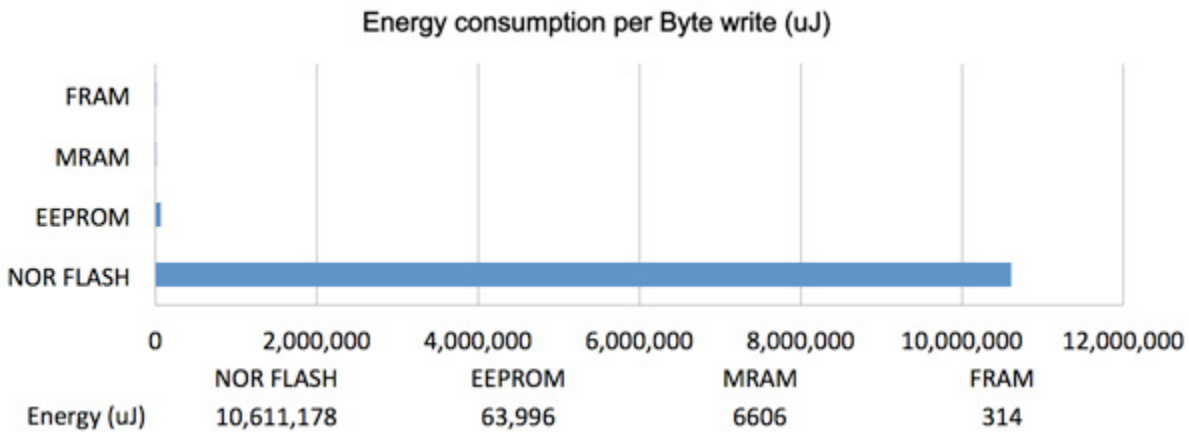
Another approach for such scenarios is an external serial interface FRAM with addressing capabilities, high speeds (40-MHz SPI), low active energy consumption (typically less than 100 µA/MHz) and densities up to 4 Mb. There are two principal advantages of serial FRAMs over MRAM, EEPROM, and flash-based memories *(Fig. 2)*. First, when writing to FRAM, power consumption is multiple orders of magnitude better than other non-volatile memories. Second, its write endurance is near infinite. Simplifying the decision is the fact that FRAMs are usually available in packages similar to those of EEPROMs and flash.

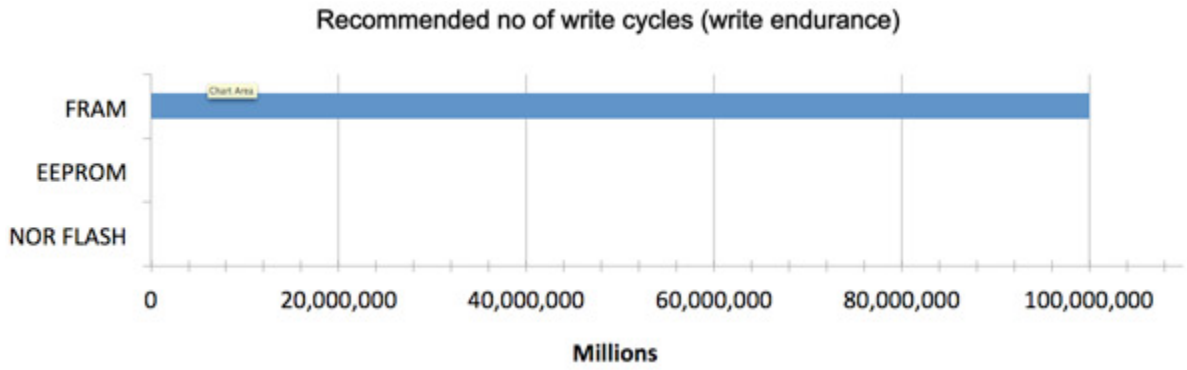


Write Endurance Comparisons

Wearable electronic devices try to conserve energy to maximize battery life. Such applications rely on small bursts of energy that provide power in short time intervals. As a result, the MCU is usually very tight in terms of how many lines of code can be executed before power is lost.

Flash-based applications pay a premium in power, not only because of higher average power while accessing the flash, but also because of higher peak power during flash write events. This peak power is mainly due to the usage of a charge pump, which causes values to climb up to 7 mA, making non-volatile writes virtually taboo in the wearable electronics world.

FRAM has no charge pump; therefore, it doesn't have high-current writes *(Fig. 3)*. The average power when writing to FRAM is the same as when reading from, or executing out of, FRAM. There's no penalty for non-volatile writes, making FRAM a truly flexible option for energy-saving applications.



Combine RAM and ROM in a Single Memory

Design engineers working on embedded systems usually select memories based on what they intended to store in it. Typical executable code is stored in nonvolatile memory, while data is stored in volatile memory (except for archival purposes). Most embedded systems, however, still maintain the traditional mix of memory technologies with applications.

Applications for memory technologies generally split between executable code and data tasks. ROM-based technologies, including mask ROM, OTP-EPROM, and NOR flash, are non-volatile. Thus, they're oriented toward code storage applications.

Other derivatives of ROM technology, including NAND flash and EEPROM, can serve as a non-volatile data memory. These come at a compromise, since they perform both code and data storage with low performance relative to alternatives. Flash's main virtue for data is its low cost, rather than ease of use or performance for data storage.

RAM-based technologies such as SRAM serve as data memory and as working space for code execution when flash is too slow. RAM provides an excellent blend of code and data functionality, but ordinary RAM offers only temporary storage.

Space-constrained applications require maximum functionality in a few devices. Even in applications with adequate board space, the design engineer may be unwilling to use three different memory types in the system. Ideally, a single memory technology could serve for code and data. Since it must be non-volatile, ordinary RAM is omitted from consideration. This leaves the ROM family of technologies, which offer poor performance as data storage media, undesirable battery-backed SRAM, or FRAM.

FRAM can lower system cost, increase system efficiency and reduce complexity while being significantly lower power than flash, EEPROM, SRAM, and other comparable technologies. If your existing flash/EEPROM-based application has energy, write speed, endurance, or power-fail backup constraints, it may be time to make the switch to FRAM.

References:

2Mb FRAM datasheet

SPI Guide to FRAMs

FRAM SPI Read and Write, Data Protection during Power Cycles

FRAM Endurance

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