

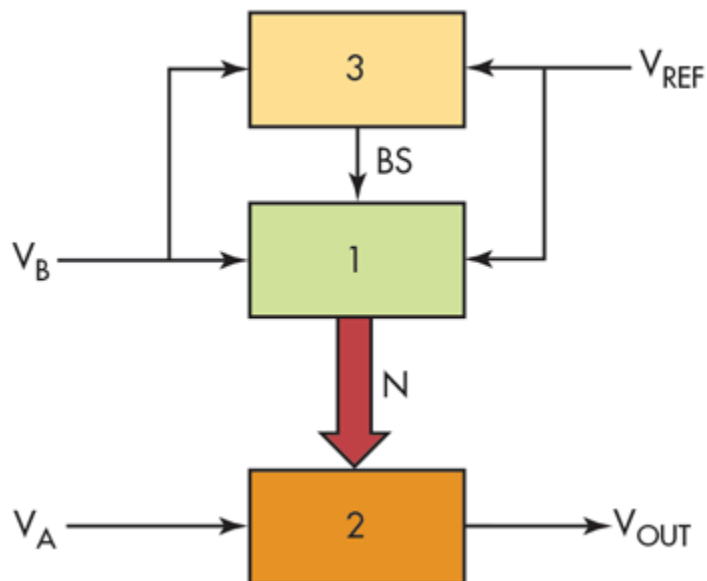
Simple Components Increase Precision of Analog-Division Circuit

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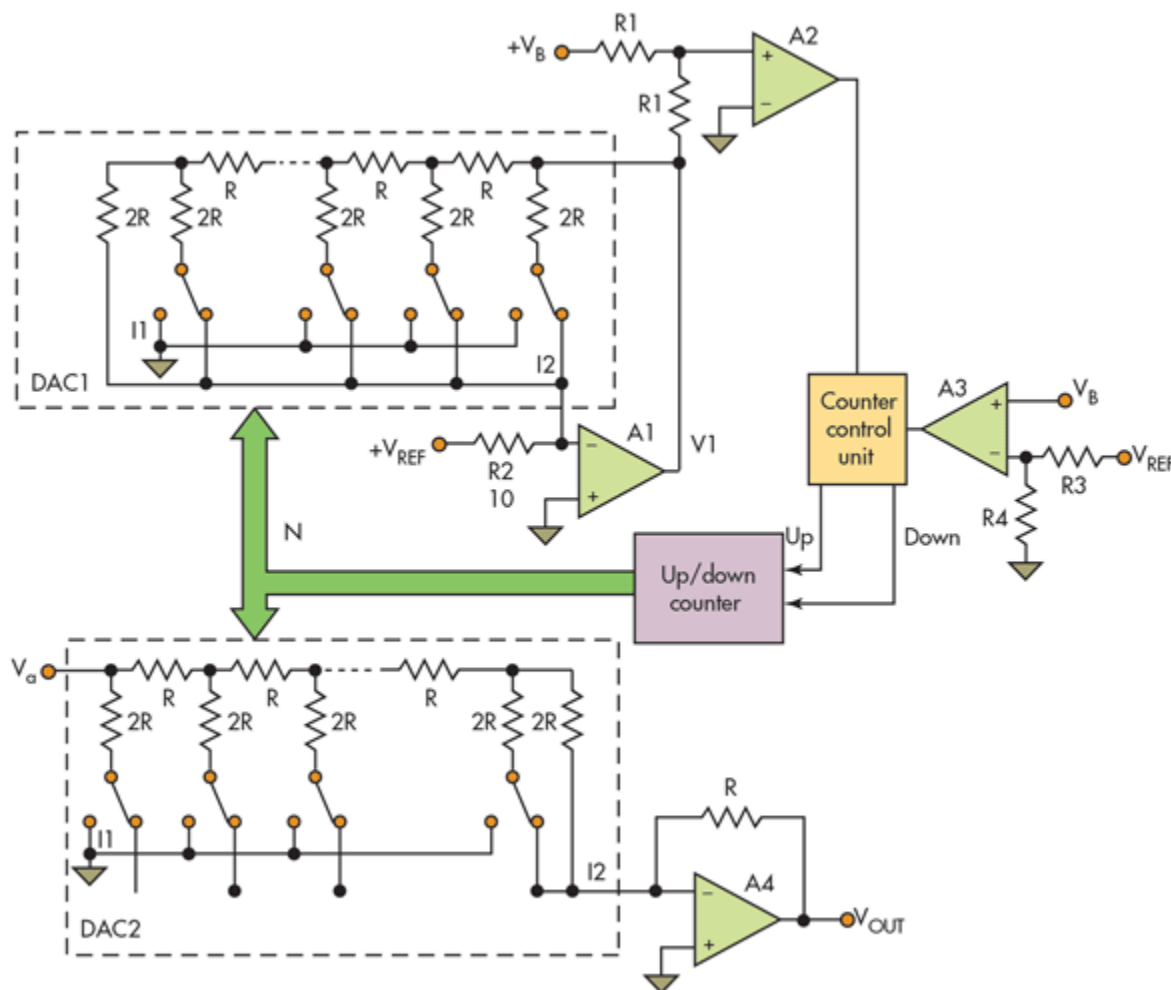
[Yakov Velikson](#)

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Despite the availability of FPGAs and microcontrollers, the historical use of analog circuitry to implement some arithmetic functions is still a viable and cost-effective technique. For the division of voltages, commonly used analog devices combine operational amplifiers with different multipliers for feedback.¹ The maximum precision of the multiplier used is based on the accuracy of the transfer function of logarithmic and antilogarithmic functions of its diodes and transistors; the minimum error achievable using these multipliers is around $\pm 0.1\%$.



To achieve much greater precision, the proposed approach uses a modified analog-to-digital converter (ADC) and two digital-to-analog converters (DACs) to do the division, with the precision determined by the number of bits in each DAC. In the circuit structure of the division device (*Fig. 1*), Block 1 is an ADC with a special compensating circuit, consisting of an op amp with DAC1 as feedback. The ADC converts the voltage of the divisor to digital code N . Block 2 is another DAC (DAC2), which yields the output voltage resulting from the division. Block 3 is a comparator that interrupts the conversion if the divisor voltage drops below the minimum possible value.



"The DACs shown here are 4-bit implementations, but DACs with more bits can be used if desired and beneficial."

In the detailed example of a division circuit (*Fig. 2*), and using a simplification of realized dependencies, define N as:

$$N = Z / (Z_{max} + 1)$$

where Z and Z_{max} are present and maximum sums of least significant bits (LSBs).² The sums of the LSBs depend on the code resolution.

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The proposed ADC differs from the usual ADC implementation in its connection to DAC1, which provides feedback via its position between the input and output of amplifier A1.³ Output I2 of DAC1 connects to the input of A1, and output I1 connects to ground. The connection of amplifier A1 determines the feedback resistance as equal to R when $N = 0$. The equivalent resistance (DAC1) to output current I2 is $R / (1 - N)$. The input resistor ($R2$) of amplifier A1 is $10R$, when the reference-voltage source V_{REF} is $+10$ V. The output voltage of amplifier A1 is:

$$\propto 1/(1 - N)$$

Input voltages V_B of ADC and V_1 connect to the comparator A2. With $V_{REF} = 10$ V, the range of voltage V_B is $+1$ V $\leq V_B \leq 10$ V. The range of code N is $0 \leq N \leq 0.9$ for the range V_B . The ADC is balanced when $V_B - V_1 = 0$. Then,

$$V_1 = V_{REF} \times 1/[10(1 - N)] \text{ or } (1 - N) = V_{REF}/10V_B$$

The output section consists of DAC2 and amplifier A4. DAC2 connects to the input of amplifier A4 by output current I_2 . Therefore, code N is the information component of V_B only.

$$V_{OUT} = \pm V_A(1 - N), \text{ or } V_{OUT} = \pm V_A \times V_{REF}/10V_B$$

The third part of the device is the comparator A3, which creates a blocking signal BS for controlling the counter. Voltage V_B is compared with $V_{REF} \times [R_4/(R_3 + R_4)]$. If V_B becomes less than 1.0 V, then the output signal BS of A3 changes to stop the counter. The output voltage of the division circuit changes polarity depending on the polarity of V_A .

The example circuit provided here reduces the error to less than $\pm 0.02\%$, based on the resolution of both DACs. You can increase precision further by increasing the number of bits, with the resistors connected in series within each DAC.

References:

1. Ulrich Tietze, Christoph Schenk, & Eberhard Gamm; *Electronic Circuits*, 2nd ed., Springer 2008, p. 762.
2. Ibid, p. 960.
3. Ibid, p. 953.

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