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Get Ready to Hit 10 nm Out of the Park

This sure is a fun and exciting industry we work in! Despite all the naysayers, each year, the focus is on the next up-and-coming IC technology. A couple of years ago, attention was on 20 nm. This year it is 16/14 nm. Behind closed doors, there are already early peeks as to what 10 nm could be.

Here in the United States, we're in the middle of the baseball season, which provides the perfect metaphor. The batter at home plate is actively involved in the game, facing a variety of 90-mph-plus pitches and trying to get on base and score runs, while the next batter in line is "on deck," warming up and watching the pitcher to analyze what might be coming. When he steps up to the plate, he wants to be as prepared as he can be, so he isn't surprised by anything the pitcher might throw at him. So in our baseball game, where are we in the technology node lifecycle?

THE BATTING ORDER

Just a couple of years ago, all the hype was about the move to 20 nm and the challenges of double patterning. Now, 20 nm is "on base" and in volume production. Many customers have released 20-nm designs to production, with more on the way.

This year, 16/14 nm is at the plate and looking to make some hits. As you recall, 16 and 14 nm are essentially two names for the same process, which is a 20-nm back end of line (BEOL) with FinFET transistors. It is still an emerging technology node, in early production and likely to remain so through the remainder of this year, but with dozens of test chips and early production chips coming off the line.

On deck, 10 nm awaits. It is in the midst of final process development tweaks, with early intellectual property (IP) development now in full engagement across the early process node adopters and the ecosystems. The node should see its very first customer test chips starting now and growing in the second half of 2014, with far more following in 2015.

So, what are the curveballs and fastballs that each of these nodes must face?

The greatest impact of these nodes falls on the designers. The designer's job of creating circuitry and layout that comply with the fabs' design rules has always become more challenging node over node as new and more complex design rules were introduced. But at 20 nm and below, it has become dramatically more difficult.

The 20-nm node introduced double patterning, which significantly increased the designer's need to understand the ramifications of how designs are manufactured. Requiring designers to design and verify layouts that could be accurately split between two masks meant familiarizing them with a host of new design concepts and rules. Also, 20 nm saw a change from minimizing fill to intelligently maximizing fill.

The 16/14-nm node added on a new transistor design (FinFET), while maintaining the rest of the 20-nm BEOL. The FinFET design offers clear IC performance and power benefits. But with this new transistor design comes the need for far more accurate parasitic extraction (PEX) models, additional convoluted fill requirements, and, as always, more complex design rule checks (DRC).

The 10-nm node will face even more exciting challenges. If early indications are correct, it puts us back on the 30%+ node-over-node increase in DRC checks that we have been slogging through since the 40-nm node. At 20 nm, some double patterning layout coloring was supported/required. At 10 nm, designers can expect to see significantly more requirements to color layouts before tapeout.

Additionally, although fill was subject to double patterning coloring requirements at the 20- and 16/14-nm nodes, fill analysis, insertion, and balancing will be significantly more "interesting" at 10 nm. We are also seeing significantly more interest in modeling and controlling sensitive net parasitics to maximize performance, control variability, and other factors.

One of the toughest 90-mph pitches that designers will need to hit at 10 nm is multi-patterning (MP). Because extreme ultraviolet lithography (EUV) continues to slip out, critical layer layouts must be divided across even more masks to resolve the structures we need. Designers are still making final adjustments to their processes, but expect to see, in addition to double patterning, the introduction of triple patterning (TP), quadruple patterning (QP), and various forms of spacer-assisted double patterning (SADP).

AT THE PLATE

The foundries have been working on 10-nm process development and enablement for some time. Their preparation includes creating test layouts and DRC/MP decks, then undertaking

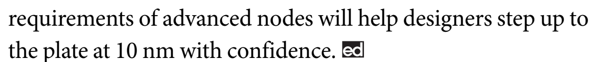
process exploration to determine what patterns/structures are manufacturable with what design rules. This exploration is an iterative process in which the foundries continually refine the layout decks and design rules, based on test results.

Once a foundry begins to converge on a process, decks, and design rules that look to be manufacturable, it begins creating a standard library and other key IP. In conjunction with this process, the foundries and their primary EDA suppliers partner closely to ensure that their preferred EDA tools have the necessary functionality and performance for the new node. Major foundry ecosystems are in the midst of this development effort to get ready for 10 nm.

Also, fabless customers are (or should be) building designs at 20 and 16/14 nm. Each of these technology nodes introduces new types of verification and analysis that help designers transition from one node to the next. A jump from, say, 28 nm directly to 10 nm would be challenging, requiring designers to adopt all these new methodologies simultaneously while also trying to intercept a market window on schedule. To attempt this, one would be swinging for the fences—a very tall order indeed.

Working closely with your foundry to understand the flows, decks, and EDA tools it is using internally is especially critical during the first few years of a node ramping into production, given all the changes that occur in the process, decks, and elsewhere. Common approaches and preferred solutions ensure you are in synch and help avoid delays in getting updated decks and flows. The introduction of MP at 10 nm means new ways of making and verifying coloring assignments. Critical to your success is partnering with your key EDA supplier and foundry early to understand the design methodology changes and flow changes that MP brings, so you can train and prepare your team.

All in all, while a lot of new pitches are being thrown at 10 nm, the old adage of "You play like you practice" still applies. Using 20- and 16/14-nm process nodes to become acquainted with the expanding complexity and new manufacturing requirements of advanced nodes will help designers step up to the plate at 10 nm with confidence.



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